

CURRENT SENSE LATCH

DESCRIPTION

This monolithic integrated circuit is an analog latch device with digital reset. It was specifically designed to provide pulse-by-pulse current limiting for switch-mode power supply systems, but many other application are also feasible. Its function is to provide a latching switch action upon sensing an input threshold voltage, with reset accomplished by an external clock signal. This device can be interfaced directly with many kinds of pulse width modulating control IC's, including the SG1524, SG1525A and SG1527A.

The input threshold for the latch circuit is 100mV, which can be referenced either to ground or to a wide-ranging positive voltage. There are high and low-going output signals available, and both the supply voltage and clock signal can be taken directly from an associated PWM control chip.

With delays in the range of 200 nanoseconds, this latch circuit is ideal for fast reaction sensing to provide overall current limiting, short circuit protection, or transformer saturation control.

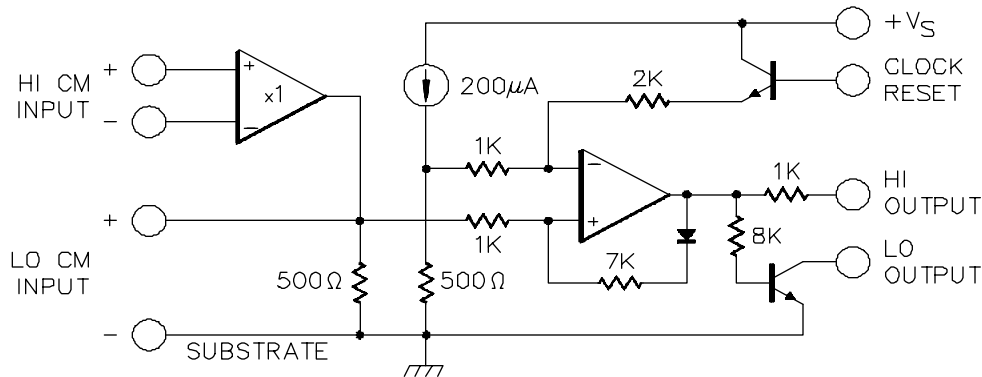
FEATURES

- Current sensing with 100mV threshold
- Common-mode input at ground or to 40V
- Complementary outputs
- Automatic reset from PWM clock
- 180ns delay
- Interface direct to SG1524, SG1525A, SG1527A

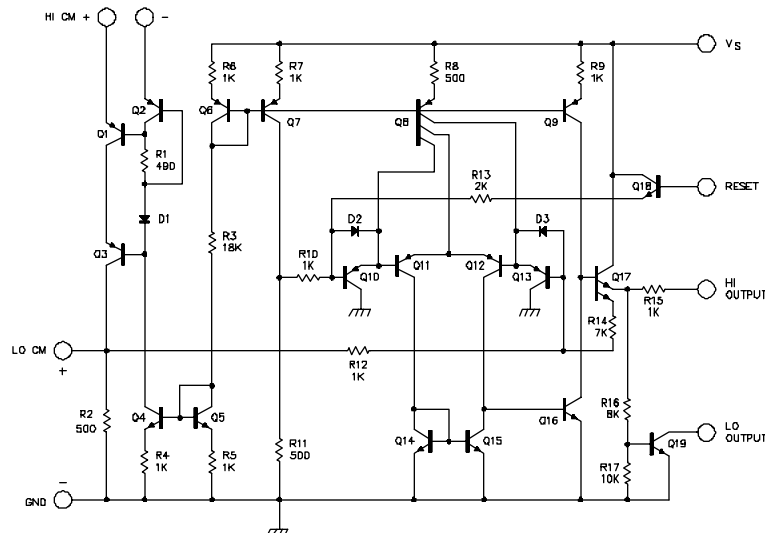
HIGH RELIABILITY FEATURES - SG1549

- ◆ Available to MIL-STD-883
- ◆ LMI level "S" processing available
- ◆ Radiation data available

BLOCK DIAGRAM



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, V_S	25V
HI CM Input Voltage	40V
LO Output "off" Voltage	40V
LO Output "on" current	25mA

Operating Junction Temperature	
Hermetic (Y Package)	150°C
Plastic (N Package)	150°C
Storage Temperature Range	-65°C to 150°C

Note 1. Values beyond which damage may occur.

THERMAL DATA

Y Package:

Thermal Resistance-Junction to Case, θ_{JC}	50°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	130°C/W

M Package:

Thermal Resistance-Junction to Case, θ_{JC}	60°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	95°C/W

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.

Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Supply Voltage, V_S	5.0V
HI CM Input Voltage	2V to 40V
LO Output "off" Voltage	5V to 40V
LO Output "on" Current	0 to 10mA
Reset LO Voltage	0V to 0.8V

Reset HI Voltage	2.5V to 5.0V
Operating Ambient Temperature Range	
SG1549Y	-55°C to 125°C
SG2549Y or M	-25°C to 85°C
SG3549Y or M	0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1549 with $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, SG2549 with $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, SG3549 with $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, and $V_S = 5\text{V}$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1549/2549			SG3549			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Section								
Supply Current	$V_{PIN8} = 5\text{V}$		2	3		2	5	mA
	$V_{PIN6} = 20\text{V}$		10	15		10	15	mA
LO CM Input Section (Note 3)								
Threshold Voltage	Pin 1 & 2 shorted, $T_A = 25^\circ\text{C}$	80	100	120	80	100	120	mV
	pin 1 & 2 shorted	70	100	130	70	100	130	mV
Input Impedance	$V_{PIN3} = 50\text{mV}$, $T_A = 25^\circ\text{C}$	400	500	600	400	500	600	Ω
	$V_{PIN3} = 50\text{mV}$	300	500	700	300	500	700	Ω
HI CM Input Section (Note 3)								
Threshold Voltage	$V_{CM} = 2\text{V}$, Pin 3 open, $T_A = 25^\circ\text{C}$	80	100	120	80	100	120	mV
	$V_{CM} = 40\text{V}$, Pin 3 open, $T_A = 25^\circ\text{C}$	80	100	120	80	100	120	mV
	$V_{CM} = 2\text{V}$, Pin 3 open	70	100	130	70	100	130	mV
	$V_{CM} = 40\text{V}$, Pin 3 open	70	100	130	70	100	130	mV
Input Current	$V_{PIN1} = V_{PIN2} = 40\text{V}$		200	300		200	300	μA
Clock Reset Section								
Min. Trigger Voltage			2.0	2.5		2.0	2.5	V
Input Current	$V_{PIN7} = 4\text{V}$		20	40		20	40	μA

Note 3. Input threshold voltages and supply current are directly proportional to supply voltage, V_S .

ELECTRICAL CHARACTERISTICS

($V_S = 5V$, and over recommended operating temperature, unless otherwise specified.)

Parameter	Test Conditions	SG1549/2549			SG3549			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
HI Output Section								
Off Voltage			0	0.1		0	0.1	V
On Voltage	$I_L = 1mA$	2.8	3.2		2.8	3.2		V
LO Output								
Off Leakage	$V_{PIN5} = 40V$.01	1.0		.01	1.0	μA
On Voltage	$I_L = 5mA$.3	0.5		.3	0.5	V

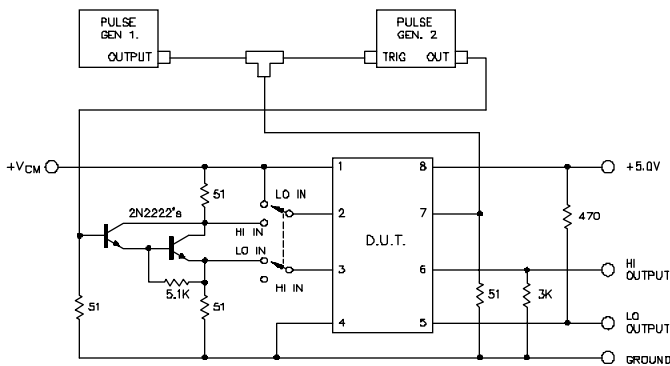
TYPICAL SWITCHING CHARACTERISTICS (Note 4)

($V_S = 5V$, $T_A = 25^\circ C$)

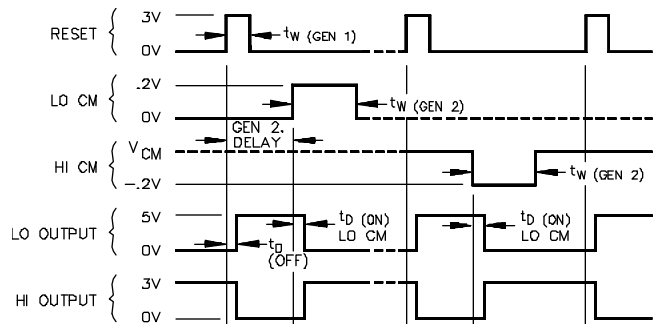
Parameter	Test Conditions	SG1549 Series			Units
		Min.	Typ.	Max.	
Reset Minimum Pulse Width (T_{W1})	Amplitude = 3.0V		150	300	ns
Delay from Reset to LO Output ($T_{D(OFF)}$)	$R_L = 470\Omega$ to V_S		300	600	ns
LO Input Minimum Pulse Width (T_{W2})	LO CM Amplitude = 200mV		50	300	ns
Delay from LO Input to LO Output ($T_{D(ON)}$)	LO CM Amplitude = 200mV, $R_L = 470\Omega$ to V_S		180	360	ns
Delay from HI Input to LO Output ($T_{D(ON)}$)	Amplitude = 200mV, $V_{CM} = 5V$		300	900	ns
Delay from HI Output to LO Output	LO CM Input = 200mV		30	60	ns

Note 4: These parameters, although guaranteed, are not tested in production.

DYNAMIC TEST CIRCUIT



SWITCHING WAVEFORMS



APPLICATION NOTES

HIGH LINE SENSING - The SG1549 will provide current sensing in the positive supply line in the typical SG1524 single-ended switching regulator application shown in Figure 1. The HI CM sense circuitry can be used with input voltages between 2 and 40 volts.

A value for R_{SC} is determined by dividing the 100mV input threshold by the peak current desired. High-frequency noise, or switching transients, can usually be eliminated by a small capacitor between pins 3 and 4. Current control may be accomplished by either the HI OUTPUT pin connected to the SG1524's Shutdown pin, or the LO OUTPUT pin connected directly to the Compensation Terminal. In either case, activation of the current sense latch will tend to discharge the compensation capacitor, C_C , which may cause slow recovery from pulse limiting. If this feature is desired, the LO OUTPUT pin may be used to discharge a soft-start network instead of coupling directly to the SG1524. If it is not desired, the use of a small value of C_C , and perhaps a diode across R_C , will enhance recovery.

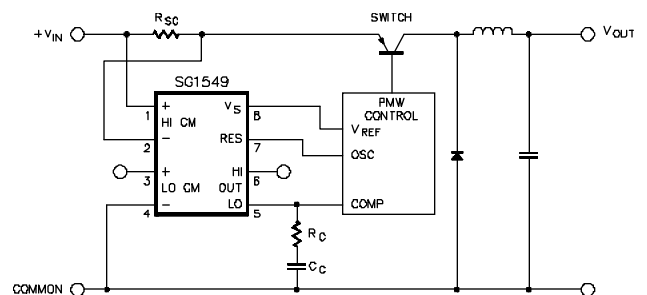


FIGURE 1 — HIGH LINE SENSING WITH THE SG1549 IN CONJUNCTION WITH AN SG1524 PWM CONTROL IC

