MBM29LV160TM/BM 90

Data Sheet *(Retired Product)*

This product has been retired and is not recommended for new designs. Availability of this document is retained for reference and historical purposes only.

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary.

For More Information

Please contact your local sales office for additional information about Spansion memory solutions.

Publication Number MBM29LV160TM/BM **Revision** DS05-20906-4E **Issue Date** July 31, 2007

This page left intentionally blank.

SPANSION™ Flash Memory

Data Sheet

September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.

AMD

FUJITSU

FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20906-4E

FLASH MEMORY

CMOS

16 M (2M × 8/1M × 16) BIT

MirrorFlash™*

MBM29LV160TM/BM 90

■ DESCRIPTION

The MBM29LV160TM/BM is a 32M-bit, 3.0 V-only Flash memory organized as 4M bytes by 8 bits or 2M words by 16 bits. The MBM29LV160TM/BM is offered in 48-pin TSOP(1) and 48-ball FBGA. The device is designed to be programmed in-system with the standard 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for program or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

The standard MBM29LV160TM/BM offers access times of 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices have separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

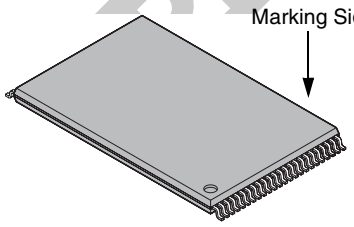
(Continued)

■ PRODUCT LINE UP

Part No.	MBM29LV160TM/BM
	90
V_{CC}	3.0 V to 3.6 V
Max Address Access Time	90 ns
Max $\overline{CE}$ Access Time	90 ns
Max $\overline{OE}$ Access Time	25 ns

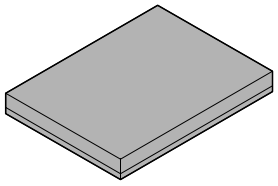
■ PACKAGES

48-pin plastic TSOP (1)



(FPT-48P-M19)

48-ball plastic FBGA



(BGA-48P-M20)

* : MirrorFlash™ is a trademark of Fujitsu Limited.

Notes : • Programming in bytemode (× 8) is prohibited.
• Programming to the address that already contains data is prohibited (It is mandatory to erase data prior to overprogram on the same address) .

FUJITSU

(Continued)

The MBM29LV160TM/BM supports command set compatible with JEDEC single-power-supply EEPROMS standard. Commands are written into the command register. The register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29LV160TM/BM is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm™ which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm™ which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. All sectors are erased when shipped from the factory.

The device features single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6. Once the end of a program or erase cycle has been completed, the devices internally return to the read mode.

Fujitsu Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The devices electrically erase all bits within a sector simultaneously via hot-hole assisted erase. The bytes/words are programmed one bytes/words at a time using the EPROM programming mechanism of hot electron injection.

■ FEATURES

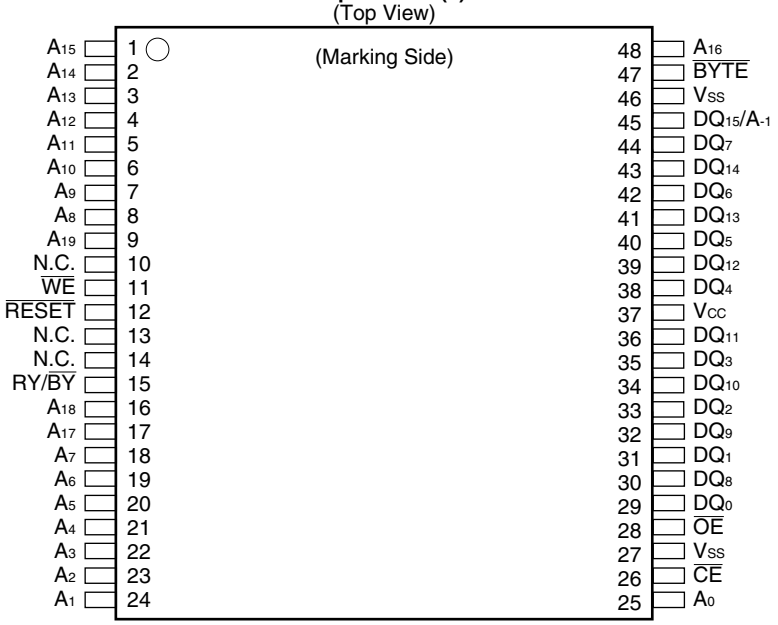
- **0.23 μm Process Technology**
- **Single 3.0 V read, program and erase**
  Minimizes system level power requirements
- **Industry-standard pinouts**
  48-pin TSOP (1) (Package suffix: TN - Normal Bend Type)
  48-ball FBGA (Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance**
  90 ns maximum access time
- **Sector erase architecture**
  One 16K bytes, two 8K bytes, one 32K bytes, and thirty-one 64K bytes sectors in byte mode
  One 8K words, two 4K words, one 16K words, and thirty-one 32K words sectors in word mode
  Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Embedded Erase™* Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™* Algorithms**
  Automatically program and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switches themselves to low power mode
- **Program Suspend/Resume**
  Suspends the program operation to allow a read in another address
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Sector Protection**
  Hardware method disables any combination of sectors from program or erase operations
- **Sector Protection Set function by Extended sector protect command**
- **Fast Programming Function by Extended Command**
- **Temporary sector unprotection**
  Temporary sector unprotection via the $\overline{\text{RESET}}$ pin
  This feature allows code changes in previously locked sectors
- **In accordance with CFI (Common Flash Memory Interface)**

* : Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

Retired Product DS05-20906-4E_July 31, 2007

■ PIN ASSIGNMENTS

48 pin TSOP(1)
(Top View)



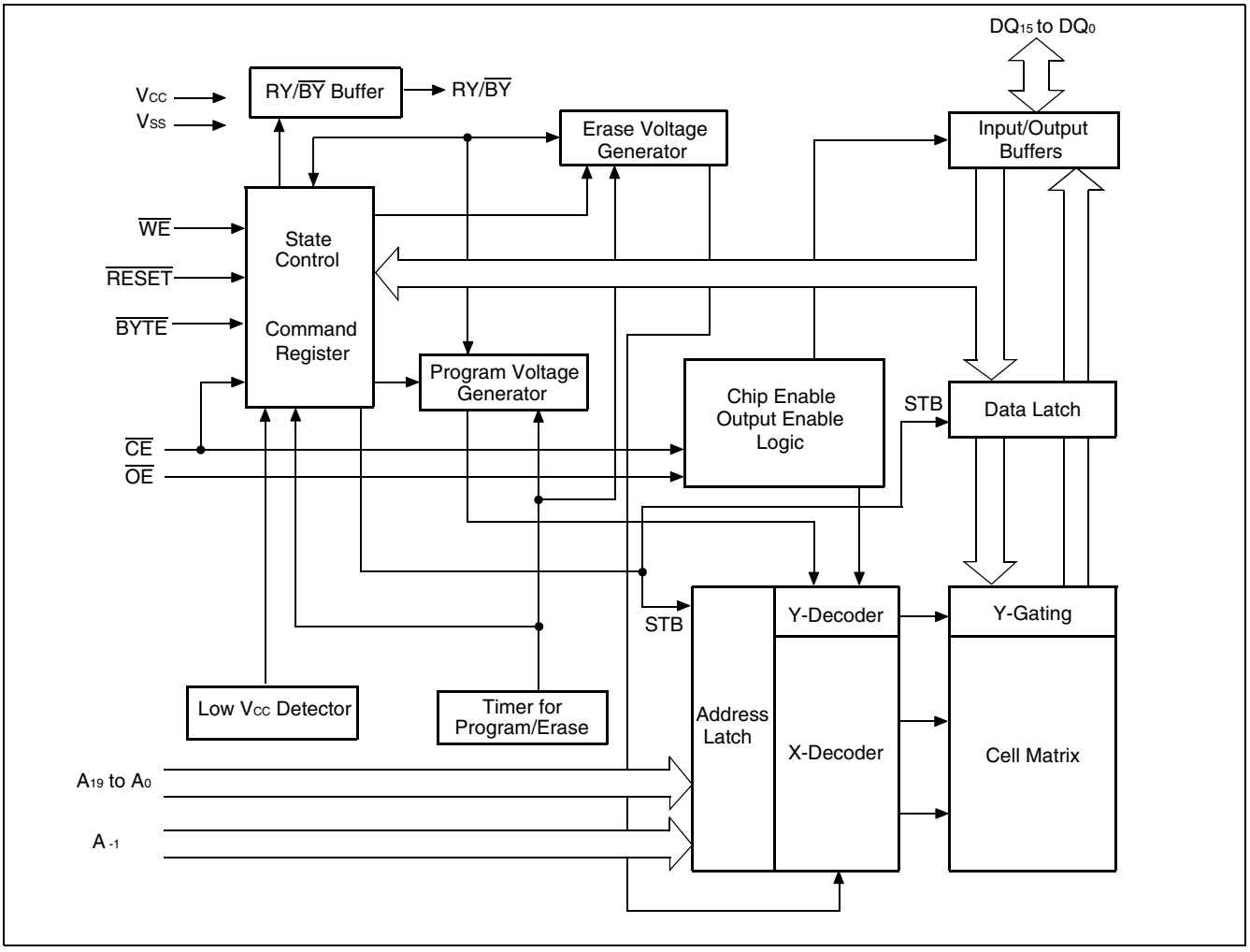
FPT-48P-M19

■ PIN DESCRIPTIONS

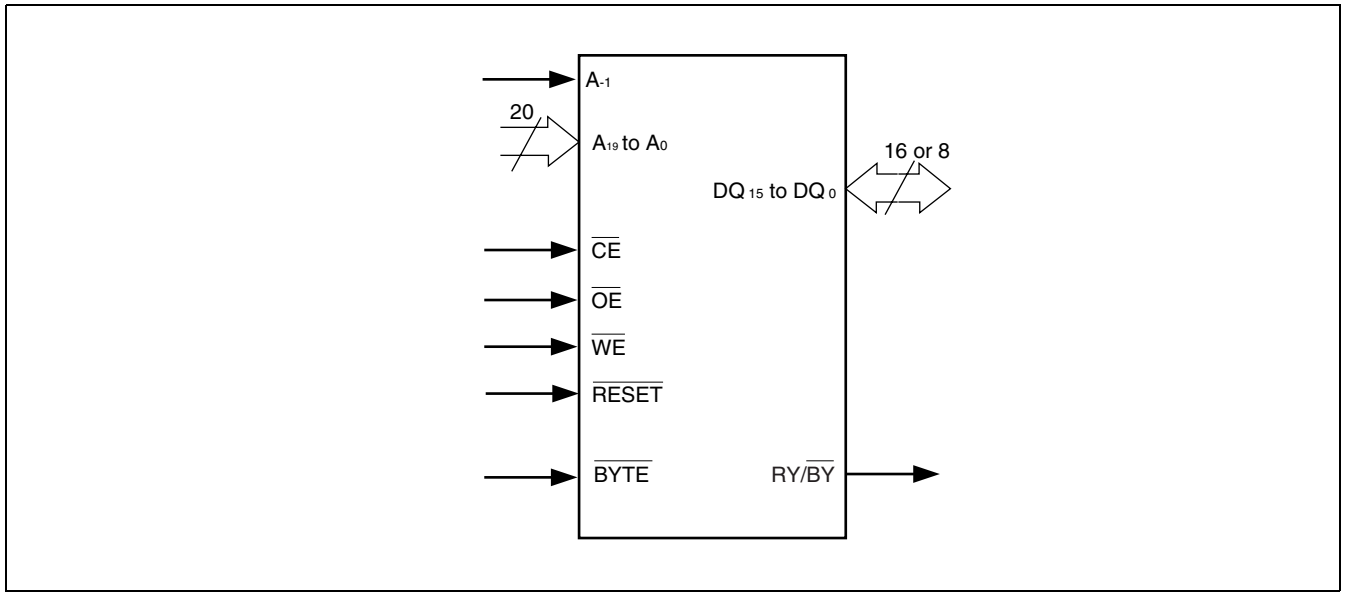
MBM29LV160TM/BM Pin Configuration

Pin	Function
A_{19} to A_0, A_{-1}	Address Inputs
DQ_{15} to DQ_0	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$	Hardware Reset Pin/Temporary Sector Unprotection
$\overline{BYTE}$	Select Byte or Word mode
RY/$\overline{BY}$	Ready/Busy Output
V_{CC}	Device Power Supply
V_{SS}	Device Ground
N.C.	No Internal Connection

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

MBM29LV160TM/BM User Bus Operations (Word Mode : $\overline{BYTE}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_{15} to DQ_0	$\overline{RESET}$
Standby	H	X	X	X	X	X	X	Hi-Z	H
Autoselect Manufacture Code *1	L	L	H	L	L	L	V_{ID}	Code	H
Autoselect Device Code *1	L	L	H	H	L	L	V_{ID}	Code	H
Read	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H
Output Disable	L	H	H	X	X	X	X	Hi-Z	H
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	*3	H
Enable Sector Protection *2	L	H	L	L	H	L	X	*3	V_{ID}
Temporary Sector Unprotection	X	X	X	X	X	X	X	*3	V_{ID}
Reset (Hardware)	X	X	X	X	X	X	X	Hi-Z	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See “1. DC Characteristics” in ■ELECTRICAL CHARACTERISTICS for voltage levels.
Hi-Z = High-Z, V_{ID} = 11.5 V to 12.5 V

*1 : Manufacturer and device codes may also be accessed via a command register write sequence. See “MBM29LV160TM/BM Standard Command Definitions”.

*2 : Refer to “Sector Protection” in ■FUNCTIIONAL DESCRIPTION.

*3 : D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm.

Retired Product DS05-20906-4E_July 31, 2007

MBM29LV160TM/BM User Bus Operations (Byte Mode : $\overline{BYTE}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_{15}/A_{-1}	A_0	A_1	A_6	A_9	DQ_7 to DQ_0	$\overline{RESET}$
Standby	H	X	X	X	X	X	X	X	Hi-Z	H
Autoselect Manufacture Code *1	L	L	H	L	L	L	L	V_{ID}	Code	H
Autoselect Device Code *1	L	L	H	L	H	L	L	V_{ID}	Code	H
Read	L	L	H	A_{-1}	A_0	A_1	A_6	A_9	D_{OUT}	H
Output Disable	L	H	H	X	X	X	X	X	Hi-Z	H
Write (Program/Erase)	L	H	L	A_{-1}	A_0	A_1	A_6	A_9	*3	H
Enable Sector Protection *2	L	H	L	L	L	H	L	X	*3	V_{ID}
Temporary Sector Unprotection	X	X	X	X	X	X	X	X	*3	V_{ID}
Reset (Hardware)	X	X	X	X	X	X	X	X	Hi-Z	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See “1. DC Characteristics” in ■ELECTRICAL CHARACTERISTICS for voltage levels.
Hi-Z = High-Z, V_{ID} = 11.5 V to 12.5V

*1 : Manufacturer and device codes may also be accessed via a command register write sequence. See “MBM29LV160TM/BM Standard Command Definitions”.

*2 : Refer to “Sector Protection” in ■FUNCTIIONAL DESCRIPTION.

*3 : D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm.

MBM29LV160TM/BM Standard Command Definitions*1

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset *2	Word /Byte	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Reset *2	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA*10	RD *10	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect(Device ID)	Word	3	555h	AAh	2AAh	55h	555h	90h	00h *10	04h *10	—	—	—	—
	Byte		AAAh		555h		AAAh							
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Program/Erase Suspend *3		1	XXXh	B0h	—	—	—	—	—	—	—	—	—	—
Program/Erase Resume *3		1	XXXh	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode *4	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Fast Program*4	Word /Byte	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode *5	Word /Byte	2	XXXh	90h	XXXh	00h *9	—	—	—	—	—	—	—	—
Extended Sector Protection*6,*7	Word	4	XXXh	60h	SA	60h	SA	40h	SA*10	SD *10	—	—	—	—
	Byte													
Query*8	Word	1	55h	98h	—	—	—	—	—	—	—	—	—	—
	Byte		AAh											

(Continued)

(Continued)

Legend : Address bits A_{19} to A_{12} = X = "H" or "L" for all address commands except for Program Address (PA), Sector Address (SA).
Bus operations are defined in "MBM29LV160TM/BM User Bus Operations (Word Mode: $\overline{BYTE}$ = V_{IH})" and "MBM29LV160TM/BM User Bus Operations (Byte Mode : $\overline{BYTE}$ = V_{IL})".
RA = Address of the memory location to be read.
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector to be programmed / erased. The combination of A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12} will uniquely select any sector. See "Sector Address Table (MBM29LV160TM)" and "Sector Address Table (MBM29LV160BM)".
SD = Sector protection verify data. Output 01h at protected sector addresses and output 00h at unprotected sector addresses.
RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.

*1 : The command combinations not described in "MBM29LV160TM/BM Standard Command Definitions" are illegal.

*2 : Both of these reset commands are equivalent.

*3 : The Erase Suspend and Erase Resume command are valid only during a sector erase operation.

*4 : The Set to Fast Mode command is required prior to the Fast Program command.

*5 : The Reset from Fast Mode command is required to return to the read mode when the device is in fast mode.

*6 : This command is valid while $\overline{RESET}$ = V_{ID}.

*7 : Sector Address (SA) with A_6 = 0, A_1 = 1, and A_0 = 0

*8 : The valid address are A_6 to A_0.

*9 : The data "F0h" is also acceptable.

*10 : Indicates read cycle.

Sector Protection Verify Autoselect Codes

Type			A_{19} to A_{12}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacturer's Code			X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	MBM29LV160TM	Word	X	V_{IL}	V_{IL}	V_{IH}	X	22C4h
		Byte					V_{IL}	C4h
	MBM29LV160BM	Word	X	V_{IL}	V_{IL}	V_{IH}	X	2249h
		Byte					V_{IL}	49h
Sector Protection			Sector Addresses	V_{IL}	V_{IH}	V_{IL}	V_{IL}	*2

*1 : A_{-1} is for Byte mode.

*2 : Outputs 01h at protected sector addresses and outputs 00h at unprotected sector addresses.

Sector Address Table (MBM29LV160TM)

Sector Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sector Size (Kbytes/ Kwords)	Address Range (x 8)	Address Range (x 16)
SA0	0	0	0	0	0	X	X	X	64/32	00000h to 0FFFFh	000000h to 007FFFh
SA1	0	0	0	0	1	X	X	X	64/32	10000h to 1FFFFh	008000h to 00FFFFh
SA2	0	0	0	1	0	X	X	X	64/32	20000h to 2FFFFh	010000h to 017FFFh
SA3	0	0	0	1	1	X	X	X	64/32	30000h to 3FFFFh	018000h to 01FFFFh
SA4	0	0	1	0	0	X	X	X	64/32	40000h to 4FFFFh	020000h to 027FFFh
SA5	0	0	1	0	1	X	X	X	64/32	50000h to 5FFFFh	028000h to 02FFFFh
SA6	0	0	1	1	0	X	X	X	64/32	60000h to 6FFFFh	030000h to 037FFFh
SA7	0	0	1	1	1	X	X	X	64/32	70000h to 7FFFFh	038000h to 03FFFFh
SA8	0	1	0	0	0	X	X	X	64/32	80000h to 8FFFFh	040000h to 047FFFh
SA9	0	1	0	0	1	X	X	X	64/32	90000h to 9FFFFh	048000h to 04FFFFh
SA10	0	1	0	1	0	X	X	X	64/32	A0000h to AFFFFh	050000h to 057FFFh
SA11	0	1	0	1	1	X	X	X	64/32	B0000h to BFFFFh	058000h to 05FFFFh
SA12	0	1	1	0	0	X	X	X	64/32	C0000h to CFFFFh	060000h to 067FFFh
SA13	0	1	1	0	1	X	X	X	64/32	D0000h to DFFFFh	068000h to 06FFFFh
SA14	0	1	1	1	0	X	X	X	64/32	E0000h to EFFFFh	070000h to 077FFFh
SA15	0	1	1	1	1	X	X	X	64/32	F0000h to FFFFFh	078000h to 07FFFFh
SA16	1	0	0	0	0	X	X	X	64/32	100000h to 10FFFFh	080000h to 087FFFh
SA17	1	0	0	0	1	X	X	X	64/32	110000h to 11FFFFh	088000h to 08FFFFh
SA18	1	0	0	1	0	X	X	X	64/32	120000h to 12FFFFh	090000h to 097FFFh
SA19	1	0	0	1	1	X	X	X	64/32	130000h to 13FFFFh	098000h to 09FFFFh
SA20	1	0	1	0	0	X	X	X	64/32	140000h to 14FFFFh	0A0000h to 0A7FFFh
SA21	1	0	1	0	1	X	X	X	64/32	150000h to 15FFFFh	0A8000h to 0AFFFFh
SA22	1	0	1	1	0	X	X	X	64/32	160000h to 16FFFFh	0B0000h to 0B7FFFh
SA23	1	0	1	1	1	X	X	X	64/32	170000h to 17FFFFh	0B8000h to B0FFFFh
SA24	1	1	0	0	0	X	X	X	64/32	180000h to 18FFFFh	0C0000h to 0C7FFFh
SA25	1	1	0	0	1	X	X	X	64/32	190000h to 19FFFFh	0C8000h to 0CFFFFh
SA26	1	1	0	1	0	X	X	X	64/32	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
SA27	1	1	0	1	1	X	X	X	64/32	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
SA28	1	1	1	0	0	X	X	X	64/32	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
SA29	1	1	1	0	1	X	X	X	64/32	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
SA30	1	1	1	1	0	X	X	X	64/32	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
SA31	1	1	1	1	1	0	X	X	32/16	1F0000h to 1F7FFFh	0F8000h to 0FBFFFh
SA32	1	1	1	1	1	1	0	0	8/4	1F8000h to 1F9FFFh	0FC000h to 0FCFFFh
SA33	1	1	1	1	1	1	0	1	8/4	1FA000h to 1FBFFFh	0FD000h to 0FDFFFh
SA34	1	1	1	1	1	1	1	X	16/8	1FC000h to 1FFFFFh	0FE000h to 0FEFFFh

Sector Address Table (MBM29LV160BM)

Sector Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sector Size (Kbytes/ Kwords)	Address Range (x 8)	Address Range (x 16)
SA0	0	0	0	0	0	0	0	X	16/8	00000h to 03FFFh	000000h to 001FFFh
SA1	0	0	0	0	0	0	1	0	8/4	04000h to 05FFFh	002000h to 002FFFh
SA2	0	0	0	0	0	0	1	1	8/4	06000h to 07FFFh	003000h to 003FFFh
SA3	0	0	0	0	0	1	0	X	32/16	08000h to 0FFFFh	004000h to 007FFFh
SA4	0	0	0	0	1	X	X	X	64/32	10000h to 1FFFFh	008000h to 00FFFFh
SA5	0	0	0	1	0	X	X	X	64/32	20000h to 2FFFFh	010000h to 017FFFh
SA6	0	0	0	1	1	X	X	X	64/32	30000h to 3FFFFh	018000h to 01FFFFh
SA7	0	0	1	0	0	X	X	X	64/32	40000h to 4FFFFh	020000h to 027FFFh
SA8	0	0	1	0	1	X	X	X	64/32	50000h to 5FFFFh	028000h to 02FFFFh
SA9	0	0	1	1	0	X	X	X	64/32	60000h to 6FFFFh	030000h to 037FFFh
SA10	0	0	1	1	1	X	X	X	64/32	70000h to 7FFFFh	038000h to 03FFFFh
SA11	0	1	0	0	0	X	X	X	64/32	80000h to 8FFFFh	040000h to 047FFFh
SA12	0	1	0	0	1	X	X	X	64/32	90000h to 9FFFFh	048000h to 04FFFFh
SA13	0	1	0	1	0	X	X	X	64/32	A0000h to AFFFFh	050000h to 057FFFh
SA14	0	1	0	1	1	X	X	X	64/32	B0000h to BFFFFh	058000h to 05FFFFh
SA15	0	1	1	0	0	X	X	X	64/32	C0000h to CFFFFh	060000h to 067FFFh
SA16	0	1	1	0	1	X	X	X	64/32	D0000h to DFFFFh	068000h to 06FFFFh
SA17	0	1	1	1	0	X	X	X	64/32	E0000h to EFFFFh	070000h to 077FFFh
SA18	0	1	1	1	1	X	X	X	64/32	F0000h to FFFFFh	078000h to 07FFFFh
SA19	1	0	0	0	0	X	X	X	64/32	100000h to 1FFFFFh	080000h to 087FFFh
SA20	1	0	0	0	1	X	X	X	64/32	110000h to 11FFFFh	088000h to 08FFFFh
SA21	1	0	0	1	0	X	X	X	64/32	120000h to 12FFFFh	090000h to 097FFFh
SA22	1	0	0	1	1	X	X	X	64/32	130000h to 13FFFFh	098000h to 09FFFFh
SA23	1	0	1	0	0	X	X	X	64/32	140000h to 14FFFFh	0A0000h to 0A7FFFh
SA24	1	0	1	0	1	X	X	X	64/32	150000h to 15FFFFh	0A8000h to 08FFFFh
SA25	1	0	1	1	0	X	X	X	64/32	160000h to 16FFFFh	0B0000h to 0B7FFFh
SA26	1	0	1	1	1	X	X	X	64/32	170000h to 17FFFFh	0B8000h to 0BFFFFh
SA27	1	1	0	0	0	X	X	X	64/32	180000h to 18FFFFh	0C0000h to 0C7FFFh
SA28	1	1	0	0	1	X	X	X	64/32	190000h to 19FFFFh	0C8000h to 0CFFFFh
SA29	1	1	0	1	0	X	X	X	64/32	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
SA30	1	1	0	1	1	X	X	X	64/32	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
SA31	1	1	1	0	0	X	X	X	64/32	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
SA32	1	1	1	0	1	X	X	X	64/32	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
SA33	1	1	1	1	0	X	X	X	64/32	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
SA34	1	1	1	1	1	X	X	X	64/32	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh

Common Flash Memory Interface Code

A_0 to A_6	DQ_{15} to DQ_0	Description
10h 11h 12h	0051h 0052h 0059h	Query-unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set (02h = Fujitsu standard)
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = not applicable)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = not applicable)
1Bh	0027h	V_{CC} Min (write/erase) DQ_7 to DQ_4: 1V/bit, DQ_3 to DQ_0: 100 mV/bit
1Ch	0036h	V_{CC} Max (write/erase) DQ_7 to DQ_4: 1V/bit, DQ_3 to DQ_0: 100 mV/bit
1Dh	0000h	V_{PP} Min voltage (00h = no V_{pp} pin)
1Eh	0000h	V_{PP} Max voltage (00h =no V_{pp} pin)
1Fh	0007h	Typical timeout per single write 2^N μs
20h	0000h	Typical timeout for Min size buffer write 2^N μs
21h	000Ah	Typical timeout per individual sector erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms
23h	0001h	Max timeout for write 2^N times typical
24h	0000h	Max timeout for buffer write 2^N times typical
25h	0004h	Max timeout per individual sector erase 2^N times typical
26h	0000h	Max timeout for full chip erase 2^N times typical
27h	0015h	Device Size = 2^N byte
28h 29h	0002h 0000h	Flash Device Interface description
2Ah 2Bh	0000h 0000h	Max number of byte in multi-byte write = 2^N
2Ch	0004h	Number of Erase Block Regions within device (01h = uniform)
2Dh 2Eh 2Fh 30h	0000h 0000h 0040h 0000h	Erase Block Region 1 Information

(Continued)

(Continued)

A_0 to A_6	DQ_{15} to DQ_0	Description
31h 32h 33h 34h	0001h 0000h 0020h 0000h	Erase Block Region 2 Information
35h 36h 37h 38h	0000h 0000h 0080h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	001Eh 0000h 0000h 0001h	Erase Block Region 4 Information
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0000h	Address Sensitive Unlock Required
46h	0002h	Erase Suspend (02h = To Read & Write)
47h	0001h	Number of sectors in per group
48h	0001h	Sector Temporary Unprotection (01h = Supported)
49h	0004h	Sector Protection Algorithm
4Ah	0000h	Dual Operation (00h = Not Supported)
4Bh	0000h	Burst Mode Type (00h = Not Supported)
4Ch	0000h	Page Mode Type (00h = Not Supported)
50h	0001h	Program Suspend (01h = Supported)

■ FUNCTIONAL DESCRIPTION

Standby Mode

There are two ways to implement the standby mode on the device, one using both the $\overline{CE}$ and $\overline{RESET}$ pins, and the other via the $\overline{RESET}$ pin only.

When using both pins, CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ input held at V_{CC} ±0.3 V. Under this condition the current consumed is less than 5 µA Max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even when $\overline{CE}$ = "H". The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, CMOS standby mode is achieved with $\overline{RESET}$ input held at V_{SS} ±0.3 V ($\overline{CE}$ = "H" or "L") . Under this condition the current consumed is less than 5 µA Max. Once the $\overline{RESET}$ pin is set high, the device requires t_{RH} as a wake-up time for output to be valid for read access.

During standby mode, the output is in the high impedance state, regardless of $\overline{OE}$ input.

Automatic Sleep Mode

Automatic sleep mode works to restrain power consumption during read-out of device data. It can be useful in applications such as handy terminal, which requires low power consumption.

To activate this mode, the device automatically switch themselves to low power mode when the device addresses remain stable after t_{ACC}+30 ns from data valid. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ in this mode. The current consumed is typically 1 µA (CMOS Level).

Since the data are latched during this mode, the data are continuously read out. When the addresses are changed, the mode is automatically canceled and the device read-out the data for changed addresses.

Autoselect

The Autoselect mode allows reading out of a binary code and identifies its manufacturer and type.It is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9. Two identifier bytes may then be sequenced from the devices outputs by toggling A_0. All addresses can be either High or Low except A_6, A_1 and A_0. See "MBM29LV160TM/BM User Bus Operations (Word Mode: $\overline{BYTE}$ = V_{IH})" and "MBM29LV160TM/BM User Bus Operations (Byte Mode : $\overline{BYTE}$ = V_{IL})" in ■DEVICE BUS OPERATION.

The manufacturer and device codes may also be read via the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in "MBM29LV160TM/BM Standard Command Definitions" in ■DEVICE BUS OPERATION.Refer to "Autoselect Command" in ■COMMAND DEFINITIONS.

In Word mode, a read cycle from address 00h returns the manufacturer's code (Fujitsu = 04h) . A read cycle at address 01h outputs device code(MBM29LV160TM: 22C4h; MBM29LV160BM: 2249h). Notice that the above applies to Word mode. The addresses and codes differ from those of Byte mode. Refer to "Sector Protection Verify Autoselect Codes" in ■DEVICE BUS OPERATION.

Read Mode

The device has two control functions required to obtain data at the outputs. $\overline{CE}$ is the power control and used for a device selection. $\overline{OE}$ is the output control and used to gate data to the output pins.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least t_{ACC}-t_{OE} time.) When reading out a data without changing addresses after power-up, input hardware reset or to change $\overline{CE}$ pin from "H" or "L".

Output Disable

With the $\overline{OE}$ input at logic high level (V_{IH}), output from the devices are disabled. This may cause the output pins to be in a high impedance state.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the device function.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever starts later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever starts first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and “Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram” in ■SWITCHING WAVEFORMS for specific timing parameters.

Sector Protection

The device features hardware sector protection. This feature will disable both program and erase operations in any combination of 35 sectors of memory. The user‘s side can use the sector protection using programming equipment. The device is shipped with all sectors that are unprotected.

To activate it, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, $\overline{CE}$ = V_{IL} and $A_6 = A_0 = V_{IL}$, $A_1 = V_{IH}$. The sector addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. “Sector Address Table (MBM29LV160TM)” and “Sector Address Table (MBM29LV160BM)” in ■DEVICE BUS OPERATION defines the sector address for each of the thirty-five (35) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See “Sector Protection Timing Diagram” in ■SWITCHING WAVEFORMS and “Sector Protection Algorithm” in ■FLOW CHART for sector protection timing diagram and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical “1” code at device output DQ_0 for a protected sector. Otherwise the device will produce “0” for unprotected sectors. In this mode, the lower order addresses, except for A_0, A_1, and A_6 can be either High or Low. Address locations with $A_1 = V_{IL}$ are reserved for Autoselect manufacturer and device codes. A_{-1} requires applying to V_{IL} on Byte mode.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) are the desired sector address will produce a logical “1” at DQ_0 for a protected sector. See “Sector Protection Verify Autoselect Codes” in ■DEVICE BUS OPERATION for Autoselect codes.

Temporary Sector Unprotection

This feature allows temporary unprotection of previously protected sectors of the devices in order to change data. The Sector Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (V_{ID}). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the V_{ID} is taken away from the $\overline{RESET}$ pin, all the previously protected sectors will be protected again. Refer to “Temporary Sector Unprotection Timing Diagram” in ■SWITCHING WAVEFORMS and “Temporary Sector Unprotection Algorithm” in ■FLOW CHART.

Hardware Reset

The devices may be reset by driving the $\overline{RESET}$ pin to V_{IL} from V_{IH}. The $\overline{RESET}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least “t_{RP}” in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode “t_{READY}” after the $\overline{RESET}$ pin is driven low. Furthermore, once the $\overline{RESET}$ pin goes high, the devices require an additional “t_{RH}” before it will allow read access. When the $\overline{RESET}$ pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. "MBM29LV160TM/BM Standard Command Definitions" in ■DEVICE BUS OPERATION shows the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Also the Program Suspend (B0h) and Program Resume (30h) commands are valid only while the Program operation is in progress.Moreover Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands must be asserted to DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored.

Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to Read mode, the Reset operation is initiated by writing the Reset command sequence into the command register. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically be in the reset state after power-up. In this case, a command sequence is not required in order to read data.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. Therefore, manufacture and device codes must be accessible while the devices reside in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However applying high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated first by writing two unlock cycles. This is followed by a third write cycle that contains the address and the Autoselect command. Then the manufacture and device codes can be read from the address, and an actual data of memory cell can be read from the another address.

Following the command write, a read cycle from address 00h returns the manufactures's code (Fujitsu = 04h). A read cycle at address 01h outputs device code (MBM29LV160TM : C4h in byte mode and 22C4h in word mode ; MBM29LV160BM : 49h in byte mode and 2249h in word mode). Refer to "Sector Protection Verify Autoselect Codes" in ■DEVICE BUS OPERATION.

To terminate the operation, it is necessary to write the Reset command into the register. To execute the Autoselect command during the operation, Reset command must be written before the Autoselect command.

Programming

The devices are programmed on a word-by-word (or byte-by-byte) basis. Programming is a four bus cycle operation. There are 2 "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) starts programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The system can determine the status of the program operation by using DQ_7 ($\overline{Data}$ Polling), DQ_6 (Toggle Bit) or RY/$\overline{BY}$. The $\overline{Data}$ Polling and Toggle Bit are automatically performed at the memory location being programmed.

The programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which the devices return to the read mode and plogram addresses are no longer latched. Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance. Hence $\overline{Data}$ Polling requires the same address which is being programmed.

If hardware reset occurs during the programming operation, the data being written is not guaranteed.

Programming is allowed in any address sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may result in either failure condition or an apparent success

according to the data polling algorithm. But a read from Reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

Note that attempting to program a “1” over a “0” will result in programming failure. This precaution is the same with Fujitsu standard NOR devices. “Embedded Program™ Algorithm” in ■FLOW CHART illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Program Suspend/Resume

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any address. Writing the Program Suspend command (B0h) during Embedded Program operation immediately suspends the programming. Refer to "Erase Suspend/Resume" for the detail.

When the Program Suspend command is written during a programming process, the device halts the program operation within 1us and updates the status bits.After the program operation has been suspended, the system can read data from any address. The data at program-suspended address is not valid. Normal read timing and command definitions apply.

After the Program Resume command (30h) is written, the device reverts to programming. The system can determine the status of the program operation using the DQ_7 or DQ_6 status bits, just as in the standard program operation. See "Write Operation Status" for more information. When issuing program suspend command in 4 μs after issuing program command, determine the status of program operation by reading status bit at more 4 μs after issuing program resume command.

The system also writes the Autoselect command sequence in the Program Suspend mode. The device allows reading Autoselect codes at the addresses within programming sectors, since the codes are not stored in the memory. When the device exits the Autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See "Autoselect Command" for more information.

The system must write the Program Resume command to exit from the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device resumes programming.

Do not read CFI code after HiddenROM Entry and Exit in program suspend mode.

Chip Erase

Chip erase is a six bus cycle operation. It begins 2 “unlock” write cycles followed by writing the “set-up” command, and 2 “unlock” write cycles followed by the chip erase command which invokes the Embedded Erase Algorithm.

The device does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm the devices automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase (Preprogram function). The system is not required to provide any controls or timings during these operations.

The system can determine the erase operation status by using DQ_7 ($\overline{\text{Data}}$ Polling), DQ_6 (Toggle Bit I) and DQ_2 (Toggle Bit II) or RY/$\overline{\text{BY}}$ output signal. The chip erase begins on the rising edge of the last $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first from last command sequence and completes when the data on DQ_7 is “1” (See “Write Operation Status”.) at which time the device returns to read mode.

Sector Erase

Sector erase is a six bus cycle operation. There are 2 “unlock” write cycles. These are followed by writing the “set-up” command. 2 more “unlock” write cycles are then followed by the Sector Erase command.

Multiple sectors may be erased concurrently by writing the same six bus cycle operations. This sequence is followed by writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than Erase Time-out time(t_{TOW}). Otherwise that command will not be accepted and erasure will not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can reoccur after the last Sector Erase command is written. A time-out of “t_{TOW}” from the rising edge of last $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first, will initiate the execution of the Sector Erase command(s). If another falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first occurs within the “t_{TOW}” time-out window the timer is reset (monitor DQ_3 to determine if the sector erase timer window is still open, see section

"DQ_3", Sector Erase Timer). Resetting the devices once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete (refer to "Write Operation Status"). Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 34).

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector(s) to be erased prior to electrical erase using the Embedded Erase Algorithm. When erasing a sector, the remaining unselected sectors remain unaffected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data}}$ Polling), DQ_6 (Toggle Bit) or RY/$\overline{\text{BY}}$.

The sector erase begins after the "t_{TOW}" time-out from the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ whichever happens first for the last sector erase command pulse and completes when the data on DQ_7 is "1" (see "Write Operation Status"), at which the devices return to the read mode. $\overline{\text{Data}}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt Sector Erase operation and then perform read to a sector not being erased. This command is applicable ONLY during the Sector Erase operation within the time-out period for sector erase. Writting the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the "Erase Resume" command (30h) resumes the erase operation.

When the "Erase Suspend" command is written during the Sector Erase operation, the device takes maximum of "t_{SPD}" to suspend the erase operation. When the devices enter the erase-suspended mode, the RY/$\overline{\text{BY}}$ output pin will be at Hi-Z and the DQ_7 bit will be at logic "1" and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation is suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode, except that the data must be read from sectors that have not been erase-suspended. Reading successively from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. see the section on DQ_2.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Do not issuing program command after entering erase-suspend-read mode.

Fast Mode Set/Reset

The device has Fast Mode function. It dispenses with the initial two unclock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming consists of two cycles instead of four bus cycles in standard program command. During the Fast mode, do not write any commands other than the Fast program/Fast mode reset command. The read operation is also executed after exiting this mode. To exit from this mode, write Fast Mode Reset command into the command register. (Refer to the "Embedded Program™ Algorithm for Fast Mode" in ■FLOW CHART.) The V_{CC} active current is required even $\overline{\text{CE}}$ = V_{IH} during Fast Mode.

Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). See “Embedded Program™ Algorithm for Fast Mode” in ■FLOW CHART.

Extended Sector Protection

In addition to normal sector protection, the device has Extended Sector Protection as extended function. This function enables protection of the sector by forcing V_{ID} on $\overline{RESET}$ pin and writes a command sequence. Unlike conventional procedures, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector protection in this mode. The extended sector protection requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60h) into the command register. Then the sector addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 0, 1, 0) should be set to the sector to be protected (set V_{IL} for the other addresses pins is recommended), and write extended sector protection command (60h). A sector is typically protected in 250 μs. To verify programming of the protection circuitry, the sector addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40h). Following the command write, a logical “1” at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical “0”, write the extended sector protection command (60h) again. To terminate the operation, set $\overline{RESET}$ pin to V_{IH}. (Refer to the “Extended Sector Protection Timing Diagram” in ■SWITCHING WAVEFORMS and “Extended Sector Protection Algorithm” in ■FLOW CHART.)

Query Command (CFI : Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98h) into the command register. Following the command write, a read cycle from specific address retrieves device information. Please note that output data of upper byte (DQ_{15} to DQ_8) is “0”. Refer to “Common Flash Memory Interface Code” in ■DEVICE BUS OPERATION. To terminate operation, it is necessary to write the Reset command sequence into the register. (See “Common Flash Memory Interface Code” in ■DEVICE BUS OPERATION.)

Write Operation Status

Detailed in “Hardware Sequence Flags” are all the status flags which can determine the status of the device for current mode operation. When checking Hardware Sequence Flags during program operations, it should be checked 4 μs after issuing program command. During sector erase, the part provides the status flags automatically to the I/O ports. The information on DQ_2 is address sensitive. If an address from an erasing sector is consecutively read, then the DQ_2 bit will toggle. However DQ_2 will not toggle if an address from a non-erasing sector is consecutively read. This allows the user to determine which sectors are erasing.

Once erase suspend is entered address sensitivity still applies. If the address of a non-erasing sector (one available for read) is provided, then stored data can be read from the device. If the address of an erasing sector (one unavailable for read) is applied, the device will output its status bits.

Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle*1
	Program Suspend Mode	Program-Suspend-Read (Program Suspended Sector)	Data	Data	Data	Data	Data
		Program-Suspend-Read (Non-Program Suspended Sector)	Data	Data	Data	Data	Data
	Erase Suspend Mode	Erase-Suspend-Read (Erase Suspended Sector)	1	1	0	0	Toggle*1
		Erase-Suspend-Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase-Suspend-Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	0	0	1*2
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspend Mode	Erase-Suspend-Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

*1 : Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle.

*2 : Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

DQ_7
$\overline{\text{Data}}$ Polling

The device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read devices will produce reverse data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ_7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read device will produce a “1” at the DQ_7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in “$\overline{\text{Data}}$ Polling Algorithm” in ■FLOW CHART.

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector addresses of sectors being erased, not protected sectors. Otherwise, the status may become invalid.

If a program address falls within a protected sector, $\overline{\text{Data}}$ polling on DQ_7 is active for approximately 1 μs, then the device returns to read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on DQ_7 is active for approximately 100 μs, then the device returns to read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

Once the Embedded Algorithm operation is close to being completed, the device data pins (DQ_7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that the device is driving status information on DQ_7 at one instant of time, and then that byte’s valid data the next. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device completes the Embedded

Algorithm operation and DQ_7 has a valid data, the data outputs on DQ_6 to DQ_0 may still be invalid. The valid data on DQ_7 to DQ_0 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspend mode or sector erase time-out.

See "$\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram" in ■SWITCHING WAVEFORMS for the $\overline{\text{Data}}$ Polling timing specifications and diagram.

DQ_6
Toggle Bit I

The device also features the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling) data from the devices will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequences. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequences. The Toggle Bit I is active during the sector time out.

In programm operation, if the sector being written to is protected, the Toggle bit will toggle for about 1 μs and then stop toggling with the data unchanged. In erase, the device will erase all the selected sectors except for the protected ones. If all selected sectors are protected, the chip will toggle the Toggle bit for about 100 μs and then drop back into read mode, having data kept remained.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ_6 to toggle. See "Toggle Bit I Timing Diagram during Embedded Algorithm Operations" in ■SWITCHING WAVEFORMS for the Toggle Bit I timing specifications and diagram.

DQ_5
Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ_5 will produce a "1". This is a failure condition indicating that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions. The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in "MBM29LV160TM/BM User Bus Operations (Word Mode : $\overline{\text{BYTE}}$ = V_{IH})" and "MBM29LV160TM/BM User Bus Operations (Byte Mode : $\overline{\text{BYTE}}$ = V_{IL})" in ■DEVICE BUS OPERATION.

The DQ_5 failure condition may also appear if a user tries to program a non blank location without pre-erase. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ_7 bit and DQ_6 never stop toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a "1". Note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device with command sequence.

DQ_3
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ_3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates a valid erase command has been written, DQ_3 may be used to determine whether the sector erase timer window is still open. If DQ_3 is "1" the internally controlled erase cycle has begun. If DQ_3 is "0", the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

See "Hardware Sequence Flags".

DQ_2
Toggle Bit II

This Toggle bit II, along with DQ_6, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the non-erase suspended sector will indicate a logic "1" at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows:

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also "Hardware Sequence Flags" and "DQ_2 vs. DQ_6" in ■SWITCHING WAVEFORMS.

Furthermore, DQ_2 can also be used to determine which sector is being erased. At the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

Reading Toggle Bits DQ_6 / DQ_2

Whenever the system initially begins reading Toggle bit status, it must read DQ_7 to DQ_0 at least twice in a row to determine whether a Toggle bit is toggling. Typically a system would note and store the value of the Toggle bit after the first read. After the second read, the system would compare the new value of the Toggle bit with the first. If the Toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ_7 to DQ_0 on the following read cycle.

However, if, after the initial two read cycles, the system determines that the Toggle bit is still toggling, the system also should note whether the value of DQ_5 is high (see the section on "DQ_5") . If it is, the system should then determine again whether the Toggle bit is toggling, since the Toggle bit may have stopped toggling just as DQ_5 went high. If the Toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the Toggle bit is toggling and DQ_5 has not gone high. The system may continue to monitor the Toggle bit and DQ_5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. (Refer to "Toggle Bit Algorithm" in ■FLOW CHART.)

Toggle Bit Status

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle*1
Erase-Suspend-Read (Erase-Suspended Sector)	1	1	Toggle*1
Erase-Suspend-Program	$\overline{DQ_7}$	Toggle	1*2

*1 : Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle.

*2 : Reading from the non-erase suspend sector address will indicate logic "1" at the DQ_2 bit.

RY/$\overline{BY}$

Ready/Busy

The device provides a RY/$\overline{BY}$ open-drain output pin to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. If the device is placed in an Erase Suspend mode, the RY/$\overline{BY}$ output will be high, by means of connecting with a pull-up resister to V_{CC}.

During programming, the RY/$\overline{BY}$ pin is driven low after the rising edge of the fourth $\overline{WE}$ pulse. During an erase operation, the RY/$\overline{BY}$ pin is driven low after the rising edge of the sixth $\overline{WE}$ pulse. The RY/$\overline{BY}$ pin will indicate a busy condition during the $\overline{RESET}$ pulse. See "RY/$\overline{BY}$ Timing Diagram during Program/Erase Operation Timing Diagram", "$\overline{RESET}$ Timing Diagram (Not during Embedded Algorithms)" and "$\overline{RESET}$ Timing Diagram (During Embedded Algorithms)" in ■SWITCHING WAVEFORMS for a detailed timing diagram. The RY/$\overline{BY}$ pin is pulled high in standby mode.

Since this is an open-drain output, RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to V_{CC}.

Word/Byte Configuration

$\overline{BYTE}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the device. When this pin is driven high, the device operates in the word (16-bit) mode. Data is read and programmed at DQ_{15} to DQ_0. When this pin is driven low, the device operates in byte (8-bit) mode. In this mode, DQ_{15}/A_{-1} pin becomes the lowest address bit, and DQ_{14} to DQ_8 bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored.

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically reset the internal state machine in Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

(1) Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO}. If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO}.

If Embedded Erase Algorithm is interrupted, the intervened erasing sector(s) is(are) not valid.

(2) Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

(3) Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

(4) Power-up Write Inhibit

Power-up of the devices with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to read mode on power-up.

(5) Sector Protection

Device user is able to protect each sector group individually to store and protect data. Protection circuit voids both write and erase commands that are addressed to protected sectors.
Any commands to write or erase addressed to protected sector are ignored .

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–20	+70	°C
Voltage with Respect to Ground All Pins Except A_9, $\overline{OE}$, and $\overline{RESET}$ *1,*2	V_{IN}, V_{OUT}	–0.5	V_{CC} + 0.5	V
Power Supply Voltage *1	V_{CC}	–0.5	+4.0	V
A_9, $\overline{OE}$, and $\overline{RESET}$ *1,*3	V_{IN}	–0.5	+12.5	V

*1 : Voltage is defined on the basis of VSS = GND = 0V.

*2 : Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –0.2 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

*3 : Minimum DC input voltage is –0.5V. During voltage transitions, these pins may undershoot V_{SS} to –0.2 V for periods of up to 20 ns.Voltage difference between input and supply voltage (V_{IN}–V_{CC}) dose not exceed to +9.0 V. Maximum DC input voltage is +12.5 V which may overshoot to +14.0 V for periods of up to 20 ns .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS*1

Parameter	Symbol	Value		Unit
		Min	Max	
Ambient Temperature	T_A	–20	+70	°C
V_{CC} Supply Voltage *2	V_{CC}	+3.0	+3.6	V

*1 : Operating ranges define those limits between which the functionality of the device is guaranteed.

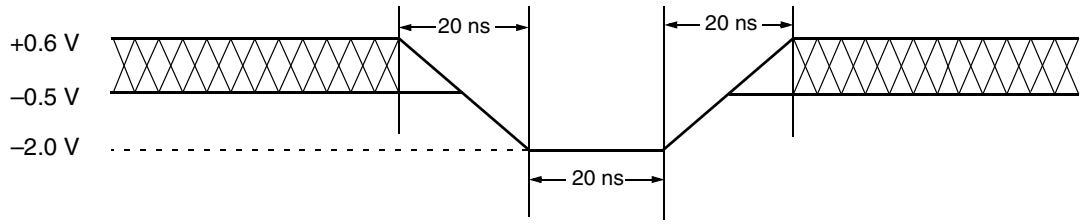
*2 : Voltage is defined on the basis of V_{SS} = GND = 0V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

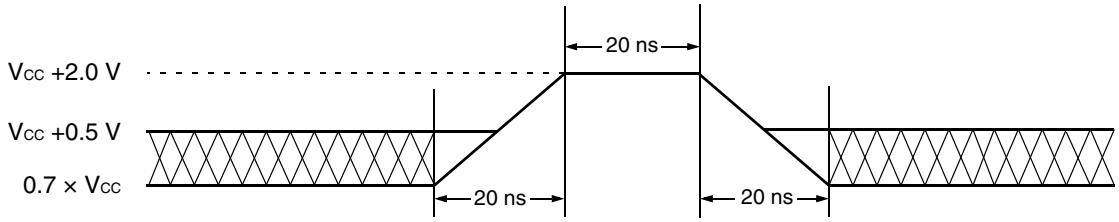
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

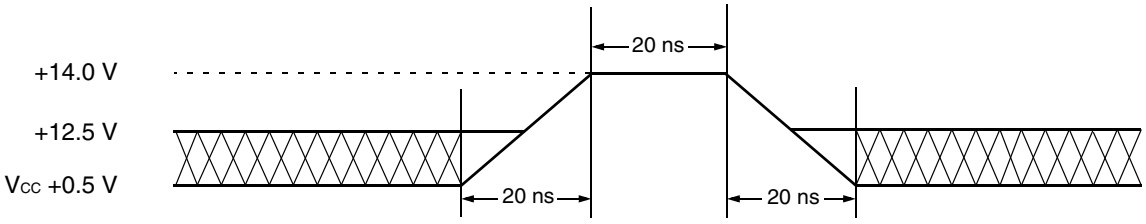
■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT



Maximum Undershoot Waveform



Maximum Overshoot Waveform 1



Note: This waveform is applied for A_9, $\overline{OE}$, and $\overline{RESET}$.

Maximum Overshoot Waveform 2

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max		–1.0	—	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max		–1.0	—	+1.0	µA
A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	I_{LIT}	V_{CC} = V_{CC} Max, A_9, $\overline{OE}$, $\overline{RESET}$ = 12.5 V		—	—	35	µA
V_{CC} Active Current (Read) *1,*2	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5 MHz	Word	—	18	20	mA
			Byte	—	16	20	
		$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 10 MHz	Word	—	35	50	
			Byte	—	35	50	
V_{CC} Active Current (Program / Erase) *2,*3	I_{CC3}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	50	60	mA
V_{CC} Standby Current *2	I_{CC4}	$\overline{CE}$ = V_{CC} ±0.3 V, $\overline{RESET}$ = V_{CC} ±0.3 V, $\overline{OE}$ = V_{IH}		—	1	5	µA
V_{CC} Reset Current *2	I_{CC5}	$\overline{RESET}$ = V_{CC} ±0.3 V		—	1	5	µA
V_{CC} Automatic Sleep Current *4	I_{CC6}	$\overline{CE}$ = V_{SS} ±0.3 V, $\overline{RESET}$ = V_{CC} ±0.3 V, V_{IN} = V_{CC} ±0.3V or V_{ss} ±0.3V		—	1	5	µA
V_{CC} Active Current (Erase-Suspend-Program) *2	I_{CC7}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	50	60	mA
Input Low Level	V_{IL}	—		–0.5	—	0.6	V
Input High Level	V_{IH}	—		0.7×V_{CC}	—	V_{CC} + 0.3	V
Voltage for Autoselect, and Temporary Sector Unprotected	V_{ID}	V_{CC} = 3.0 V to 3.6 V		11.5	12.0	12.5	V
Output Low Voltage Level	V_{OL}	I_{OL} = 4.0 mA, V_{CC} = V_{CC} Min		—	—	0.45	V
Output High Voltage Level	V_{OH}	I_{OH} = –2.0 mA, V_{CC} = V_{CC} Min		0.85×V_{CC}	—	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—		2.3	—	2.5	V

*1 : The I_{CC} current listed includes both the DC operating current and the frequency dependent comnent.

*2 : Maximum I_{CC} values are tested with V_{CC} = V_{CC} Max.

*3 : I_{CC} active while Embedded Erase or Embedded Program is in progress.

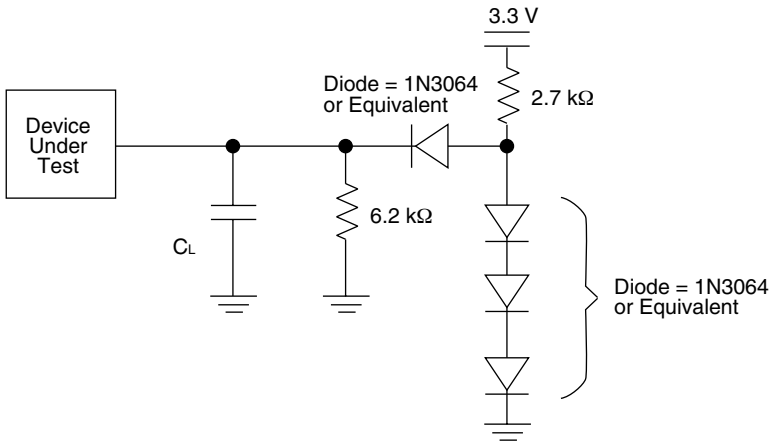
*4 : Automatic sleep mode enables the low power mode when address remain stable for t_{ACC} + 30 ns.

2. AC Characteristics

- **Read Only Operations Characteristics**

Parameter		Symbol		Condition	Value*		Unit
		JEDEC	Standard		Min	Max	
Read Cycle Time		t_{AVAV}	t_{RC}	—	90	—	ns
Address to Output Delay		t_{AVQV}	t_{ACC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}	—	90	ns
Chip Enable to Output Delay		t_{ELQV}	t_{CE}	$\overline{OE}$ = V_{IL}	—	90	ns
Output Enable to Output Delay		t_{GLQV}	t_{OE}	—	—	25	ns
Chip Enable to Output High-Z		t_{EHQZ}	t_{DF}	—	—	25	ns
Output Enable Hold Time	Read	—	t_{OEH}	—	0	—	ns
	Toggle and $\overline{Data}$ Polling			—	10	—	ns
Output Enable to Output High-Z		t_{GHQZ}	t_{DF}	—	—	25	ns
Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		t_{AXQX}	t_{OH}	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode		—	t_{READY}	—	—	20	µs

* : Test Conditions : Output Load : 1 TTL gate and 30 pF
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V or V_{CC}
Timing measurement reference level
Input : V_{CC} / 2
Output : V_{CC} / 2



Test Conditions

- **Write (Erase/Program) Operations**

Parameter		Symbol		Value			Unit
		JEDEC	Standard	Min	Typ	Max	
Write Cycle Time		t_{AVAV}	t_{WC}	90	—	—	ns
Address Setup Time		t_{AVWL}	t_{AS}	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling		—	t_{ASO}	15	—	—	ns
Address Hold Time		t_{WLAX}	t_{AH}	45	—	—	ns
Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling		—	t_{AHT}	0	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	35	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	ns
Output Enable Setup Time		—	t_{OES}	0	—	—	ns
$\overline{CE}$ High During Toggle Bit Polling		—	t_{CEPH}	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling		—	t_{OEPH}	20	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		t_{GHWL}	t_{GHWL}	0	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{CE}$ Low)		t_{GHEL}	t_{GHEL}	0	—	—	ns
$\overline{CE}$ Setup Time		t_{ELWL}	t_{CS}	0	—	—	ns
$\overline{WE}$ Setup Time		t_{WLEL}	t_{WS}	0	—	—	ns
$\overline{CE}$ Hold Time		t_{WHEH}	t_{CH}	0	—	—	ns
$\overline{WE}$ Hold Time		t_{EHWH}	t_{WH}	0	—	—	ns
$\overline{CE}$ Pulse Width		t_{ELEH}	t_{CP}	35	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	35	—	—	ns
$\overline{CE}$ Pulse Width High		t_{EHEL}	t_{CPH}	25	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	30	—	—	ns
Programming Time	Word	t_{WHWH1}	t_{WHWH1}	—	25	—	µs
	Byte			—	25	—	
Sector Erase Operation *1		t_{WHWH2}	t_{WHWH2}	—	1.0	—	s
V_{CC} Setup Time		—	t_{VCS}	50	—	—	µs
Recovery Time From RY/$\overline{BY}$		—	t_{RB}	0	—	—	ns

(Continued)

(Continued)

Parameter	Symbol		Value			Unit
	JEDEC	Standard	Min	Typ	Max	
Erase/Program Valid to RY/$\overline{BY}$ Delay	—	t_{BUSY}	—	—	90	ns
Rise Time to V_{ID} *2	—	t_{VIDR}	500	—	—	ns
Voltage Transition Time *2	—	t_{VLHT}	4	—	—	µs
Write Pulse Width*2	—	t_{WPP}	100	—	—	µs
$\overline{OE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{OESP}	4	—	—	µs
$\overline{CE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{CSP}	4	—	—	µs
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	—	ns
$\overline{RESET}$ High Time Before Read	—	t_{RH}	100	—	—	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	90	ns
Erase Time-out Time	—	t_{TOW}	50	—	—	µs
Erase Suspend Transition Time	—	t_{SPD}	—	—	20	µs

*1 : This does not include the preprogramming time.

*2 : This timing is for Sector Protection operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector Erase Time	—	1	15	s	Excludes programming time prior to erasure
Programming Time	—	25	1000	µs	Excludes system-level overhead
Chip Programming Time	—	—	100	s	
Erase/Program Cycle	100,000	—	—	cycle	

■ TSOP (1) PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	8	10	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	8.5	12	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	8	10	pF
$\overline{OE}$ Pin and $\overline{RESET}$ Pin Capacitance	C_{IN3}	V_{IN} = 0	20	25	pF

Note : Test conditions T_A = +25°C, f = 1.0 MHz

■ FBGA PIN CAPACITANCE

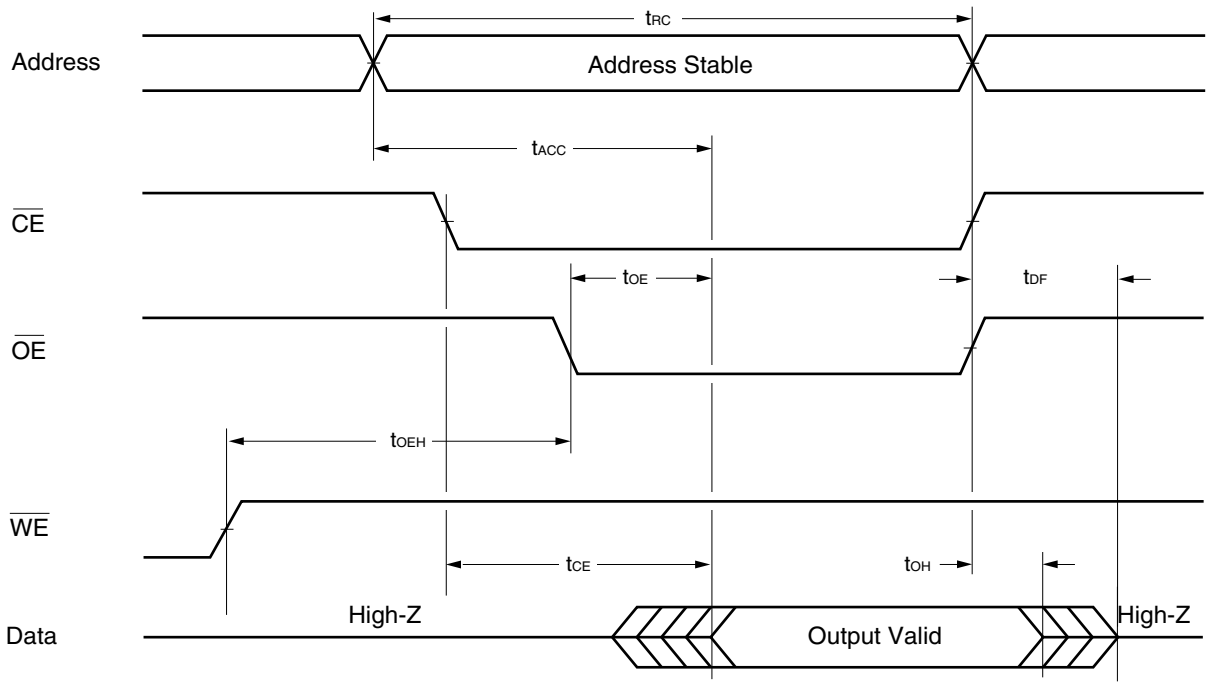
Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	8	10	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	8.5	12	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	8	10	pF
$\overline{OE}$ Pin and $\overline{RESET}$ Pin Capacitance	C_{IN3}	V_{IN} = 0	15	20	pF

Note : Test conditions T_A = +25°C, f = 1.0 MHz

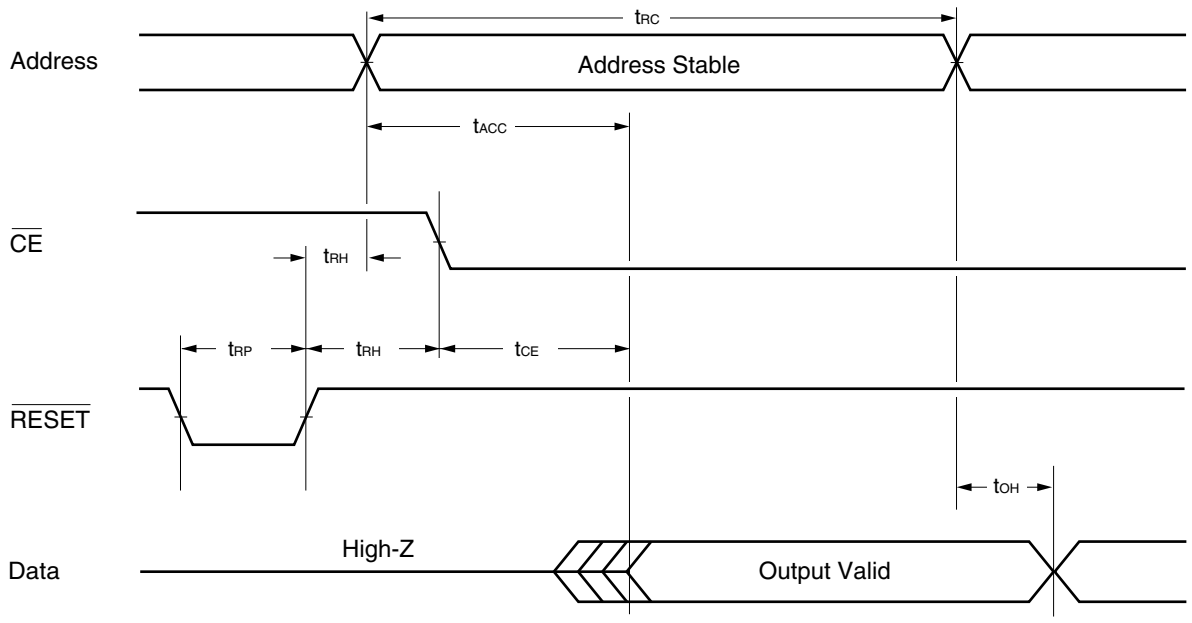
■ SWITCHING WAVEFORMS

- **Key to Switching Waveforms**

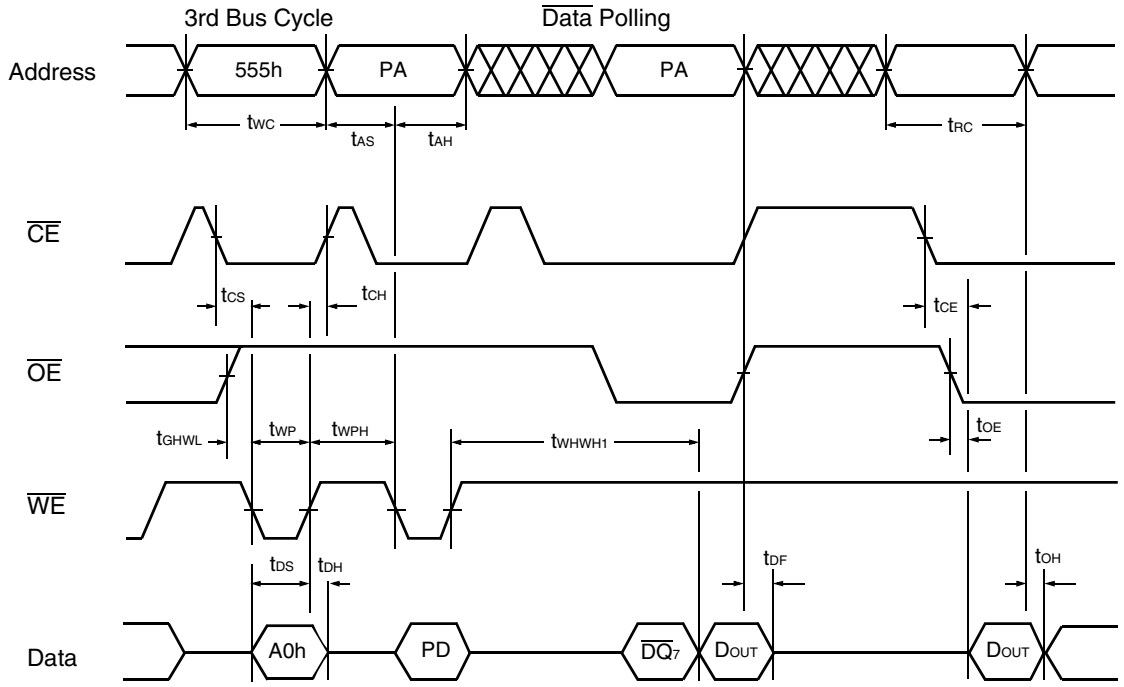
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	"H" or "L" Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State



Read Operation Timing Diagram

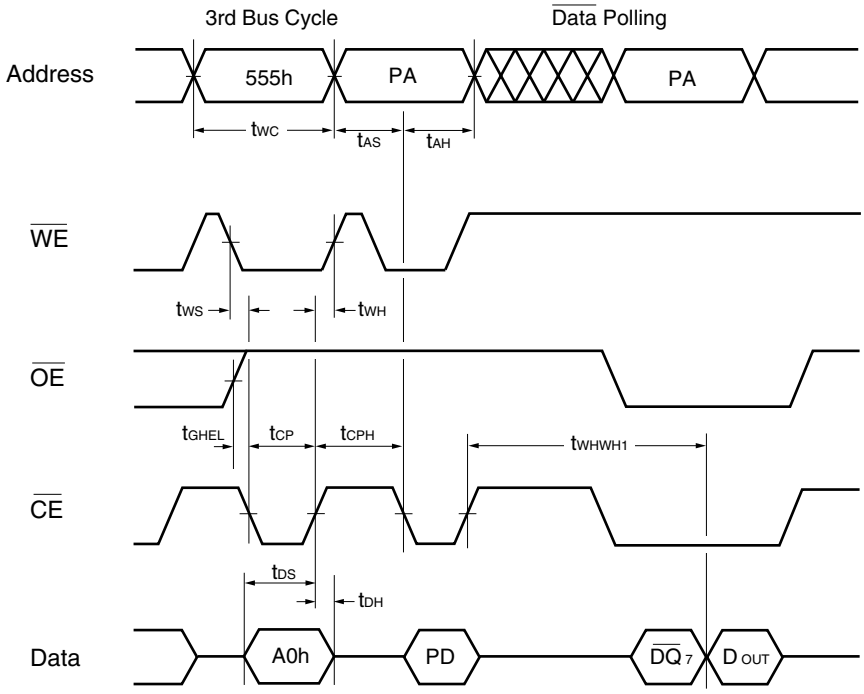


Hardware Reset/Read Operation Timing Diagram



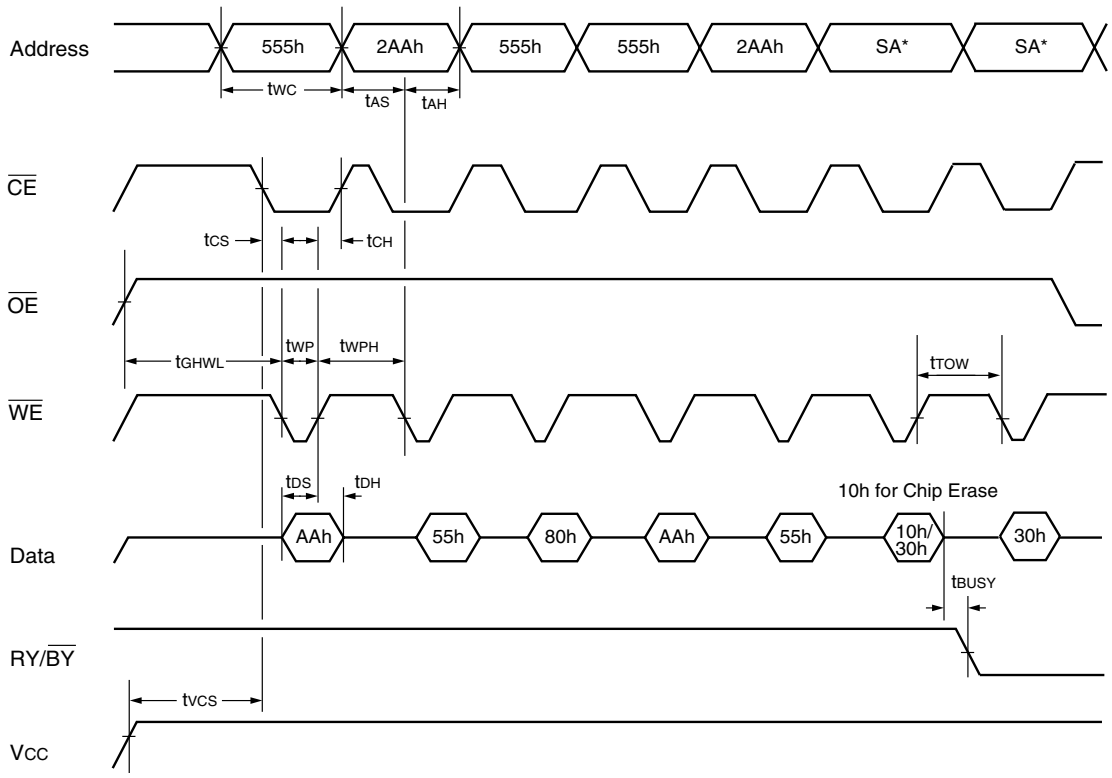
Notes : • PA is address of the memory location to be programmed.
• PD is data to be programmed at word address.
• $\overline{DQ_7}$ is the output of the complement of the data written to the device.
• D_{OUT} is the output of the data written to the device.
• Figure indicates the last two bus cycles out of four bus cycle sequence.

Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram



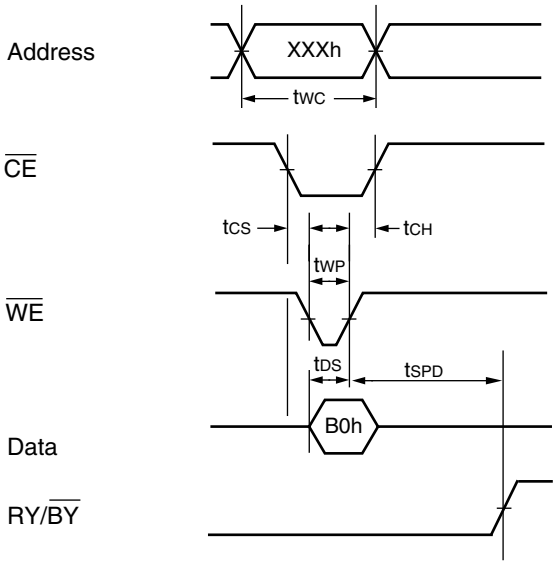
Notes : • PA is address of the memory location to be programmed.
• PD is data to be programmed at word address.
• $\overline{DQ}_7$ is the output of the complement of the data written to the device.
• D_{OUT} is the output of the data written to the device.
• Figure indicates the last two bus cycles out of four bus cycle sequence.

Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram

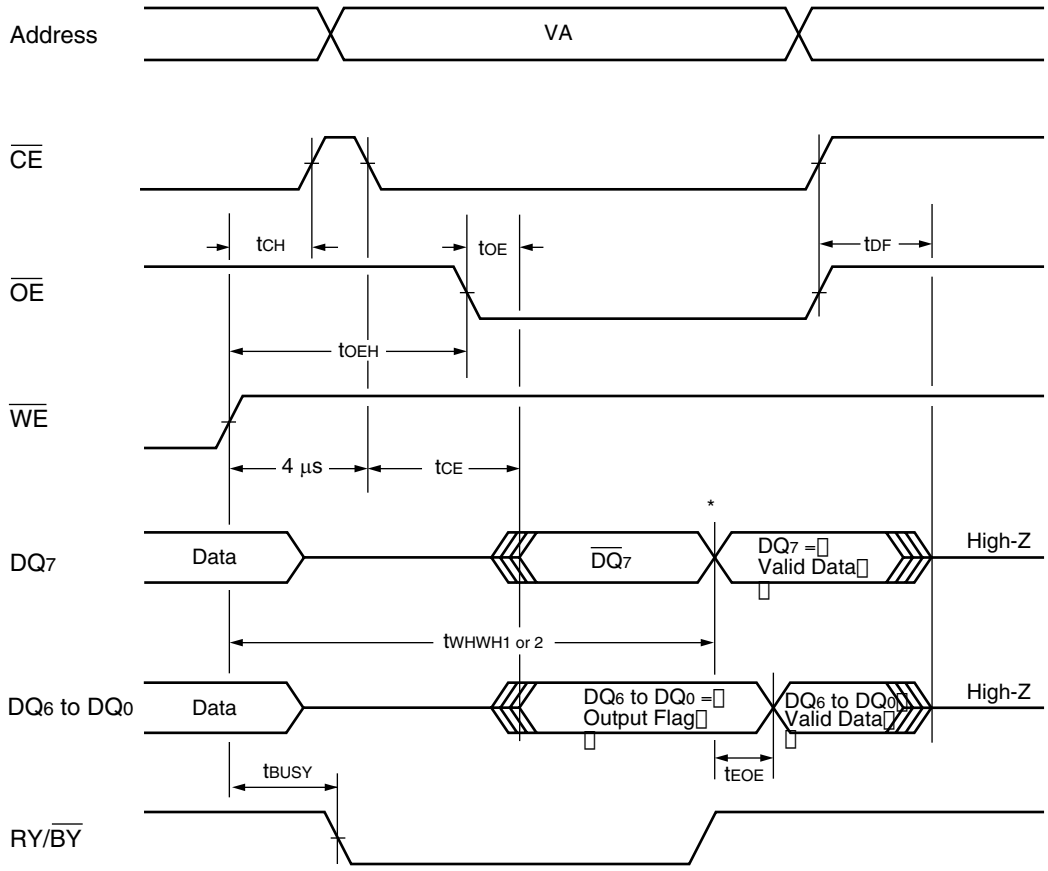


* : SA is the sector address for Sector Erase. Addresses = 555h (Word), AAAh (Byte) for Chip Erase.

Chip/Sector Erase Operation Timing Diagram



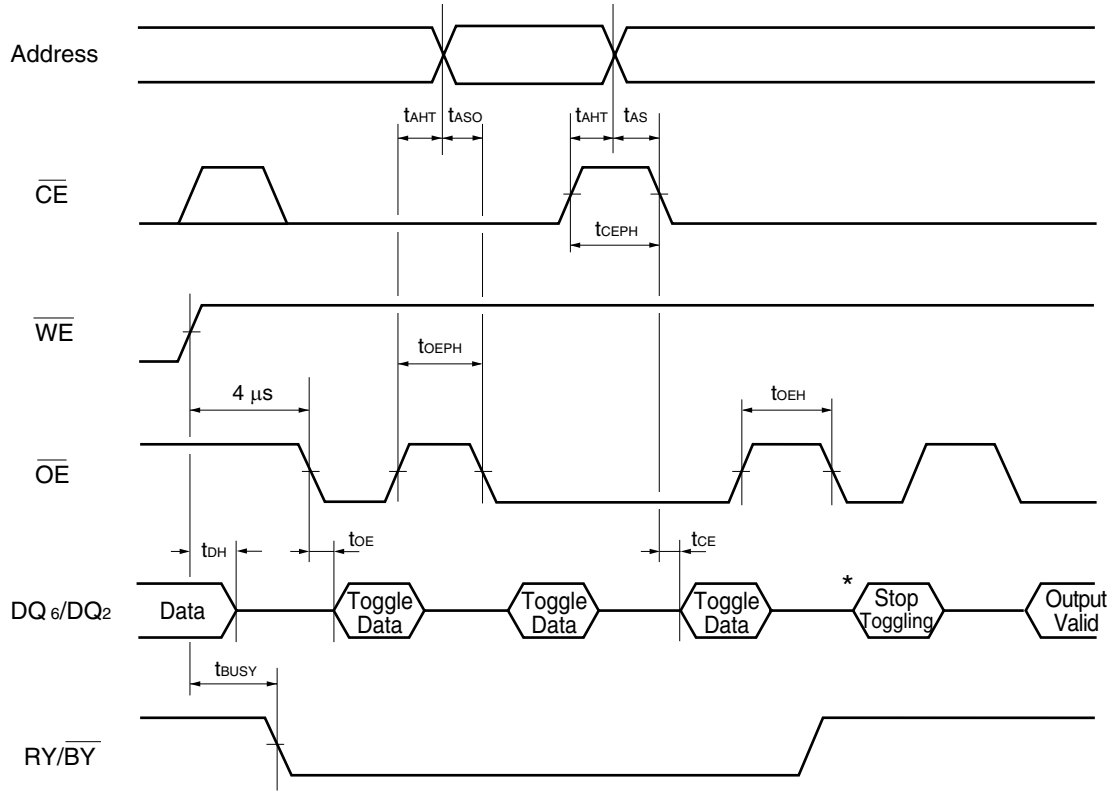
Erase Suspend Operation Timing Diagram



* : DQ_7 = Valid Data (The device has completed the Embedded operation.)

Note : When checking Hardware Sequence Flags during program operations, it should be checked 4 µs after issuing program command.

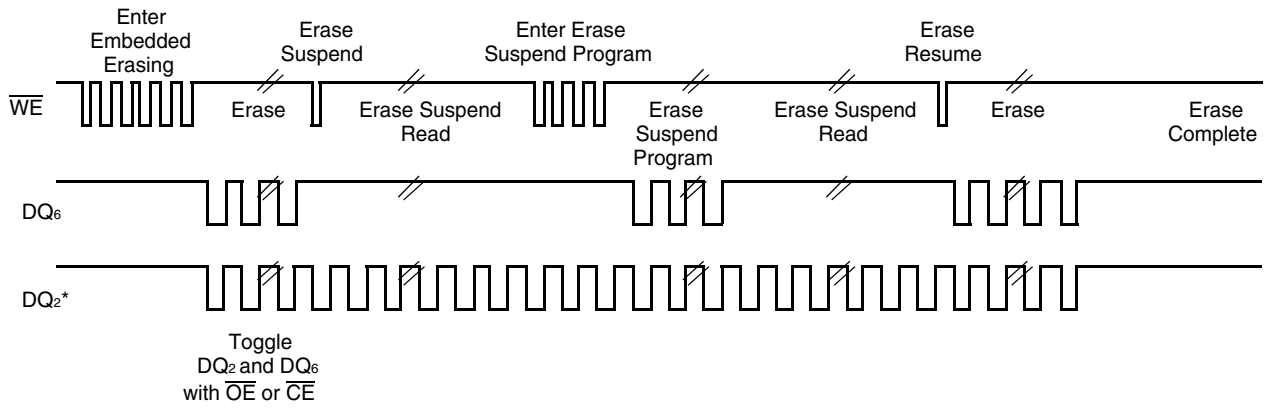
$\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram



* : DQ_6 stops toggling (The device has completed the Embedded operation).

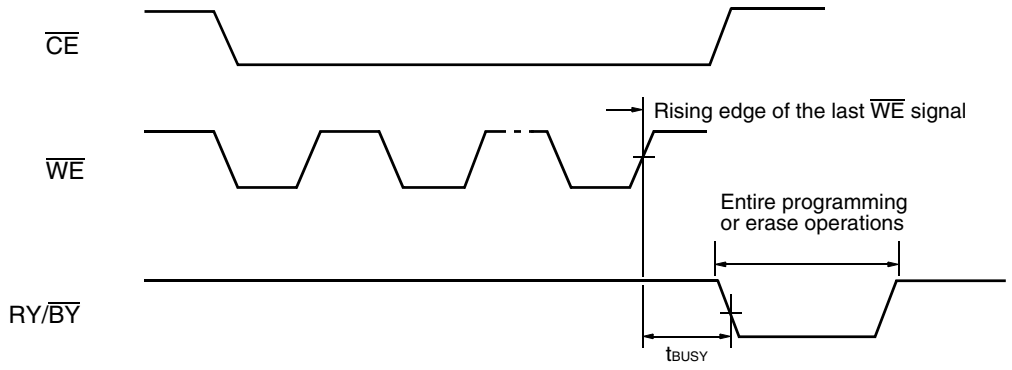
Note : When checking Hardware Sequence Flags during program operations, it should be checked 4 µs after issuing program command.

Toggle Bit I Timing Diagram during Embedded Algorithm Operations

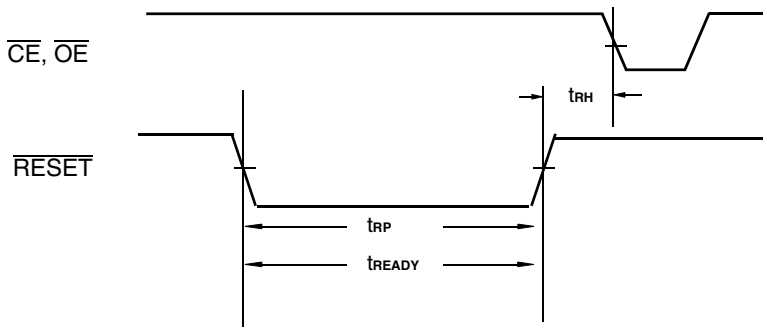


* : DQ_2 is read from the erase-suspended sector.

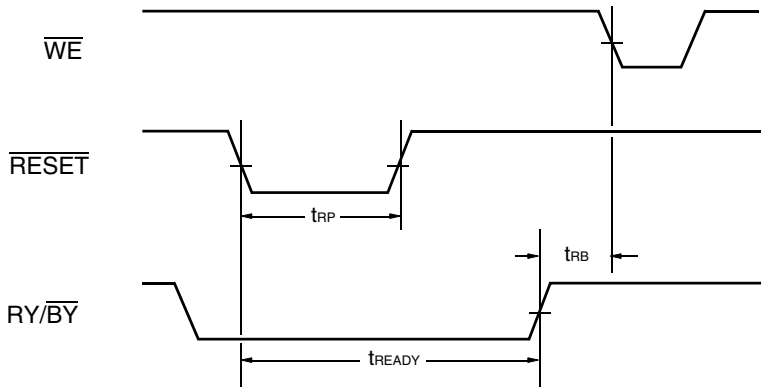
DQ_2 vs. DQ_6



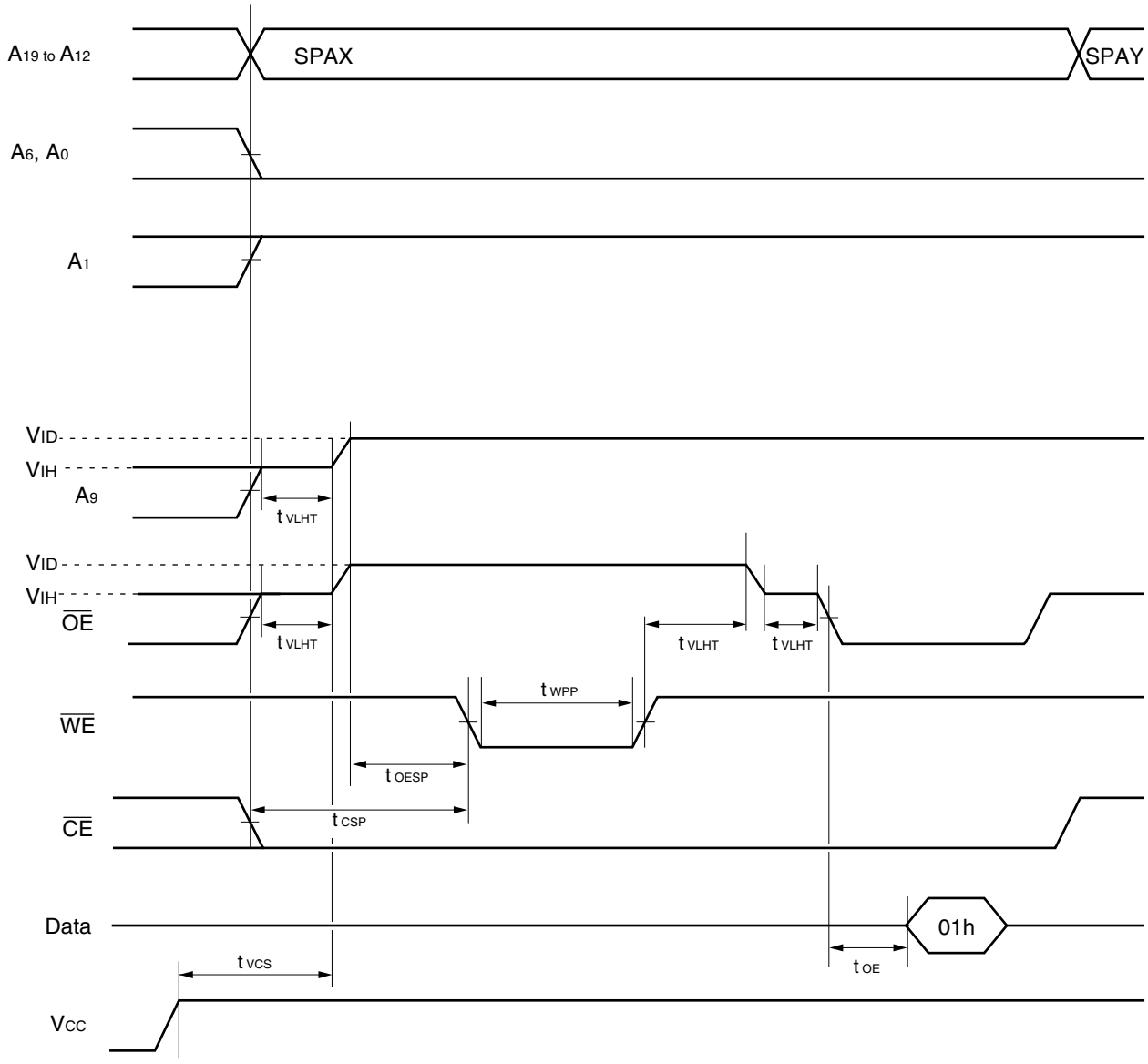
RY/$\overline{BY}$ Timing Diagram during Program/Erase Operation Timing Diagram



$\overline{RESET}$ Timing Diagram (Not during Embedded Algorithms)

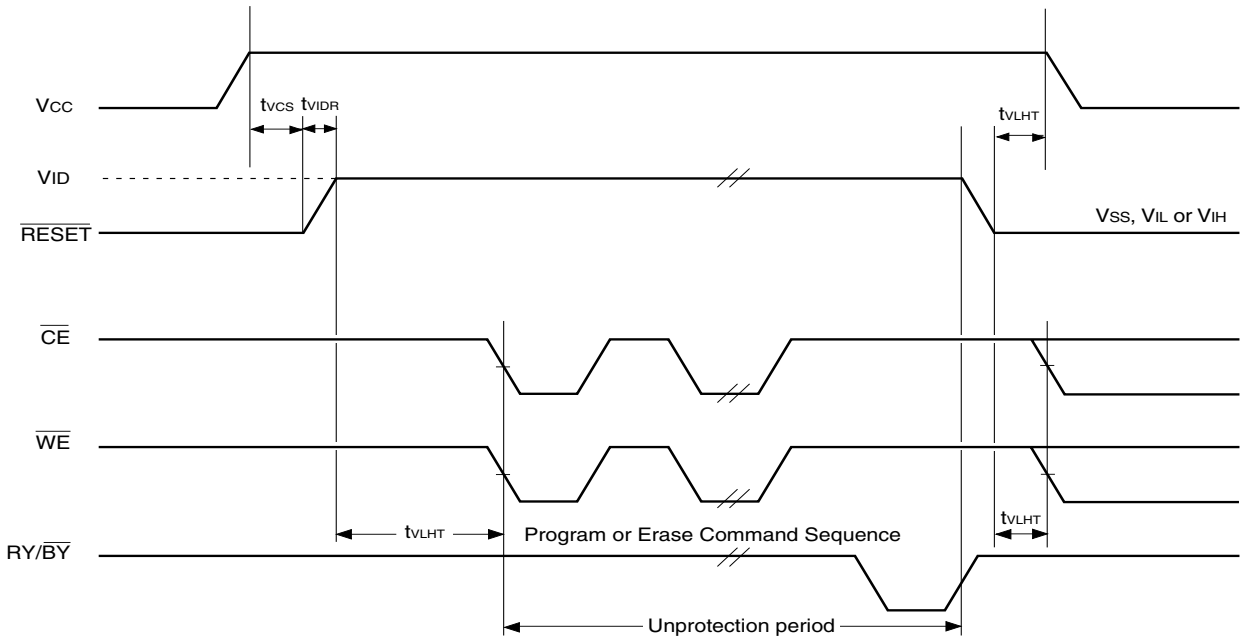


$\overline{\text{RESET}}$ Timing Diagram (During Embedded Algorithms)

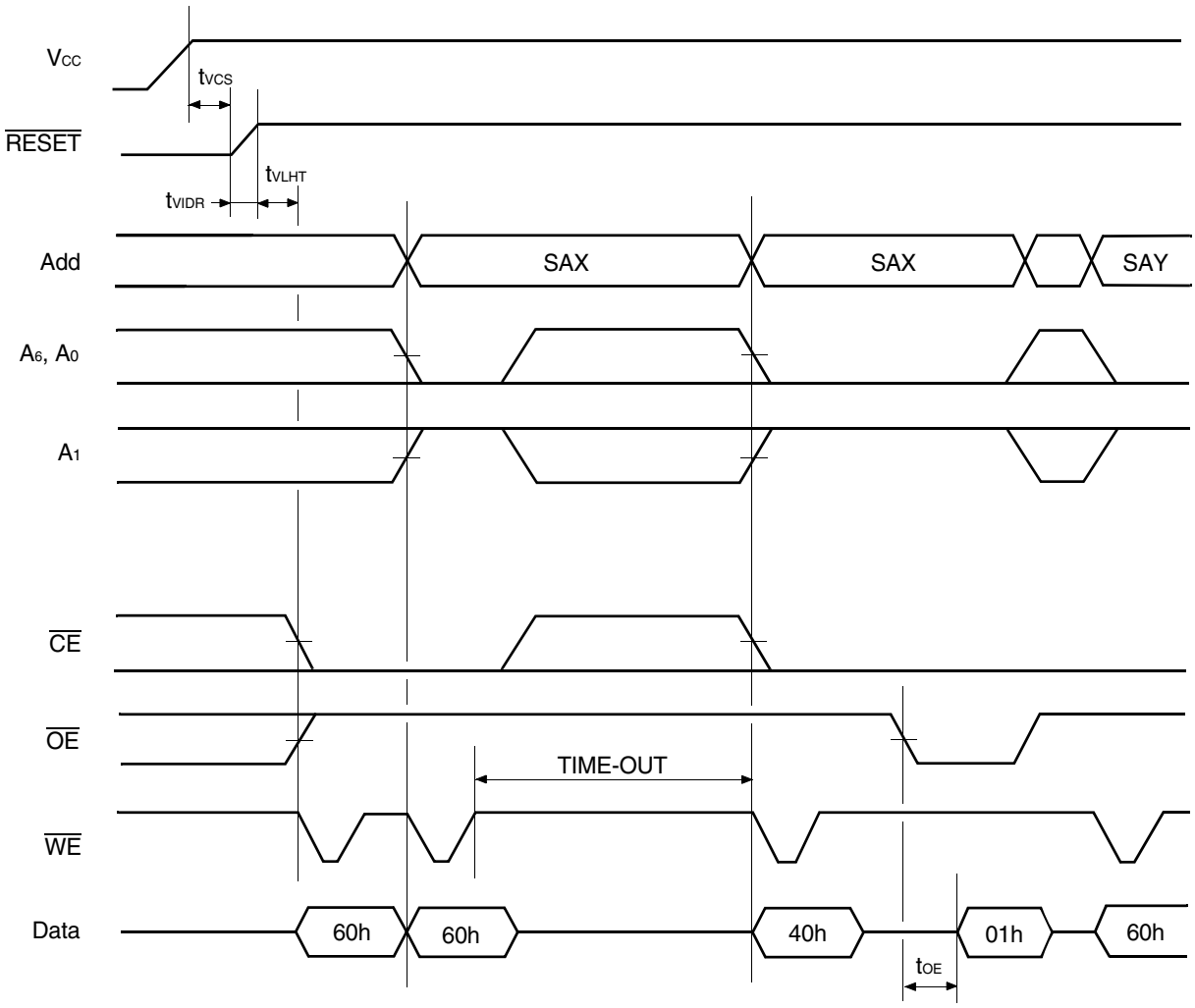


SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected

Sector Protection Timing Diagram



Temporary Sector Unprotection Timing Diagram

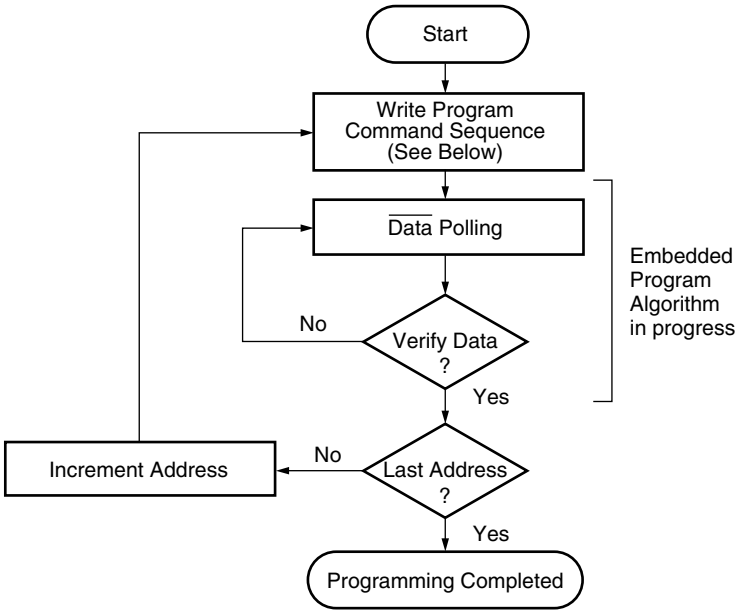


SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
TIME-OUT : Time-Out window = 250 μs (Min)

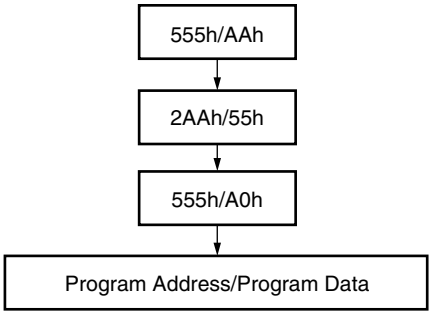
Extended Sector Protection Timing Diagram

■ FLOW CHART

EMBEDDED ALGORITHMS



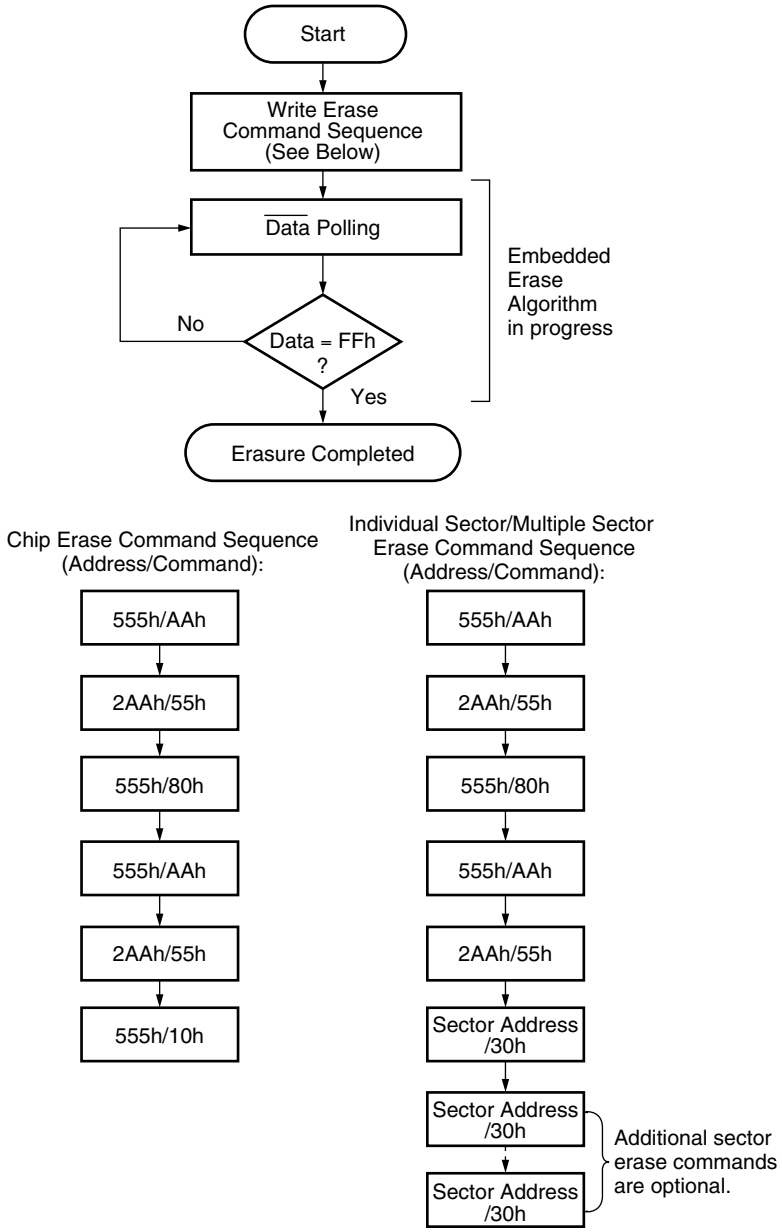
Program Command Sequence (Address/Command):



Note : The sequence is applied for Word (×16) mode.
The addresses differ from Byte (× 8) mode.

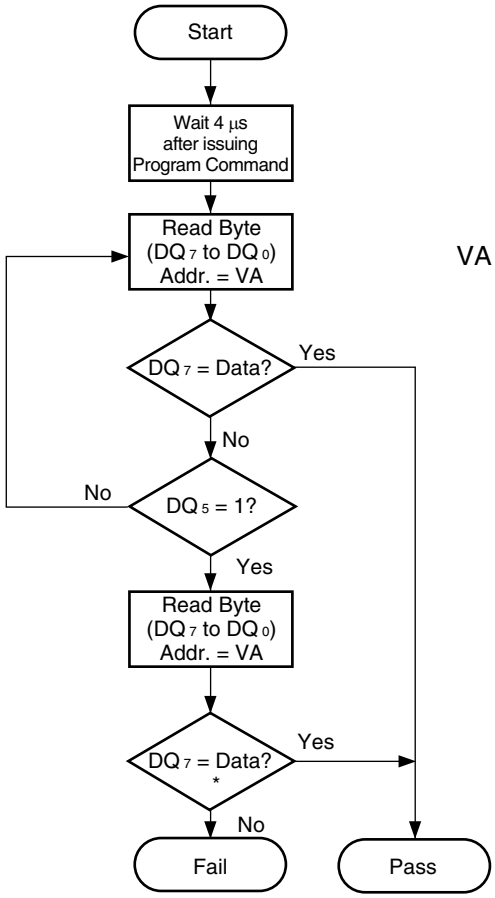
Embedded Program™ Algorithm

EMBEDDED ALGORITHMS



Note : The sequence is applied for Word (×16) mode.
The addresses differ from Byte (× 8) mode.

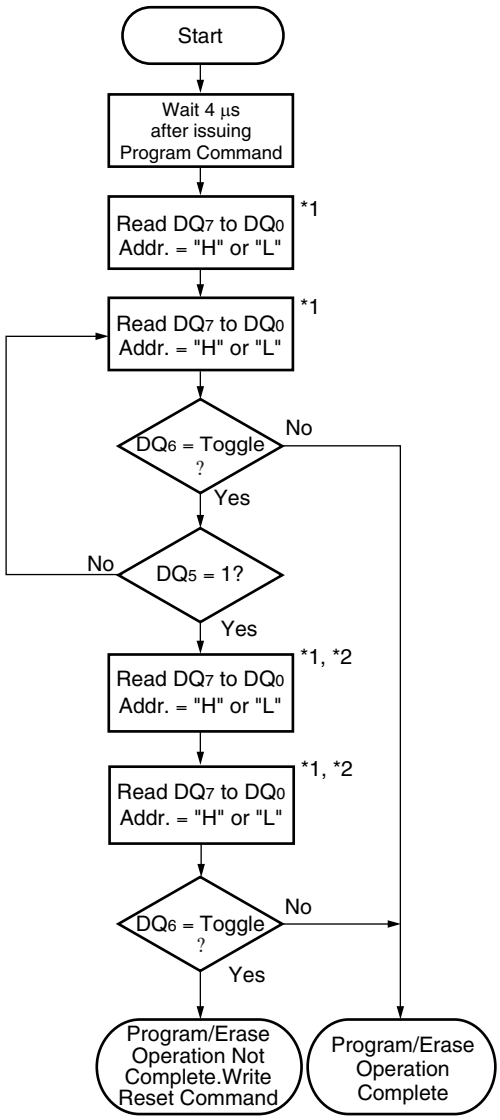
Embedded Erase™ Algorithm



VA = Valid address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple sector erases operation
= Any of the sector addresses within the sector not being protected during chip erase operation

* : DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.

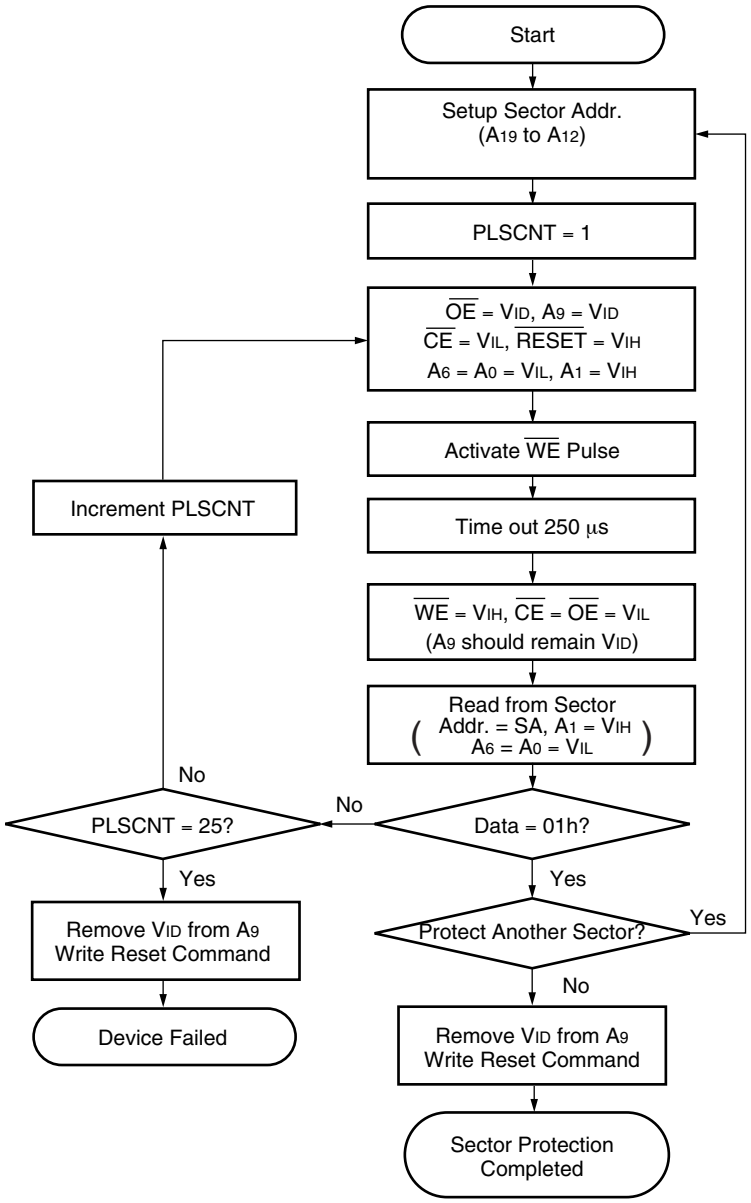
$\overline{\text{Data}}$ Polling Algorithm



*1 : Read Toggle bit twice to determine whether it is toggling.

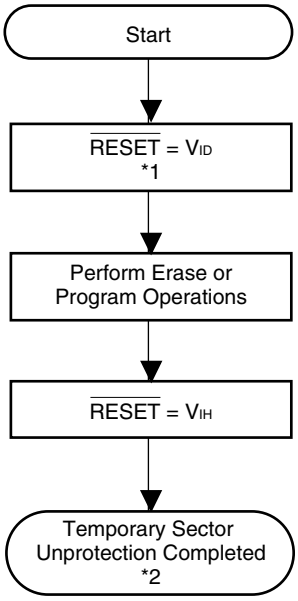
*2 : Recheck Toggle bit because it may stop toggling as DQ_5 changes to “1”.

Toggle Bit Algorithm



Note : A_{-1} is V_{IL} in Byte (× 8) mode.

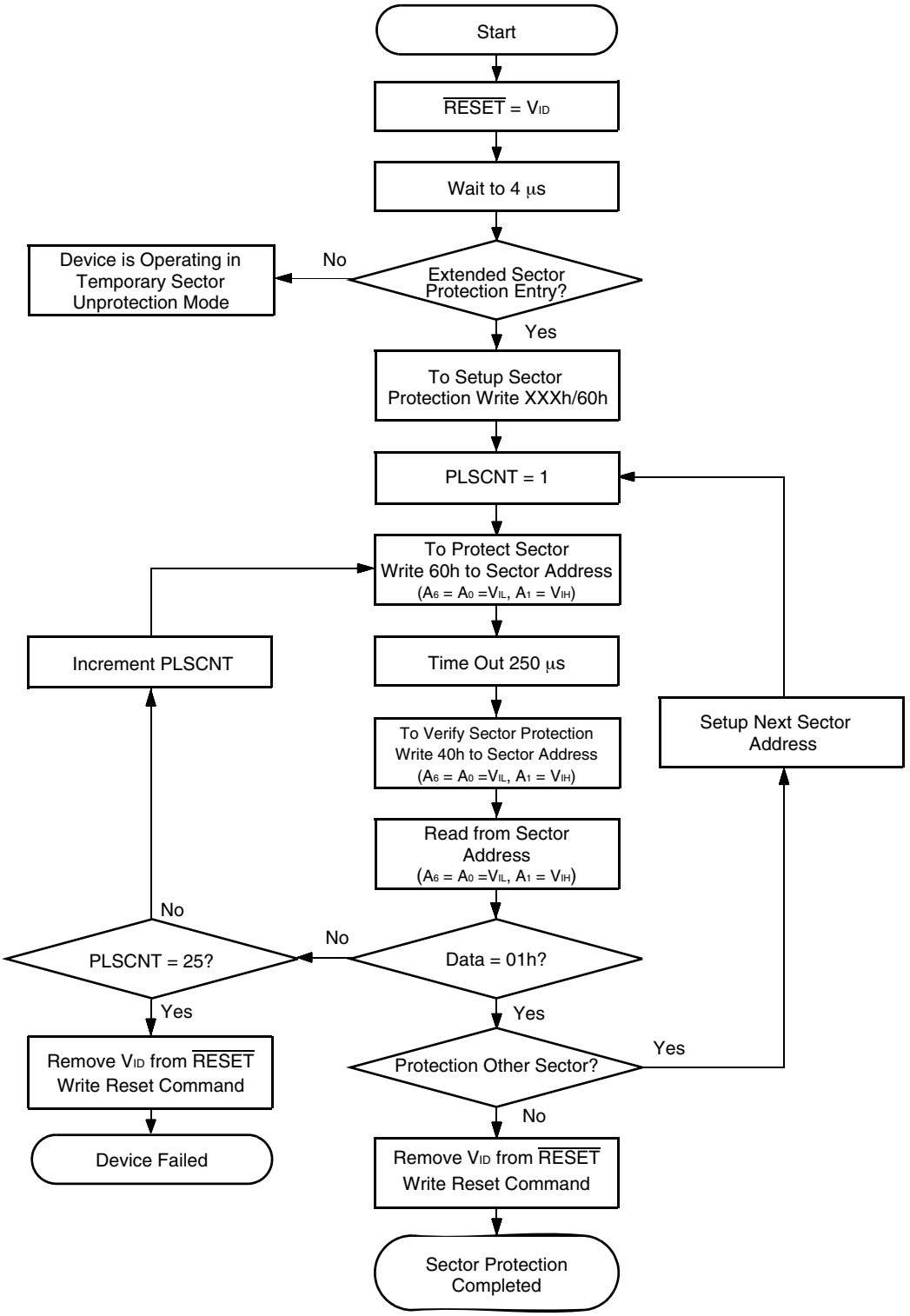
Sector Protection Algorithm



*1 : All protected sectors are unprotected.

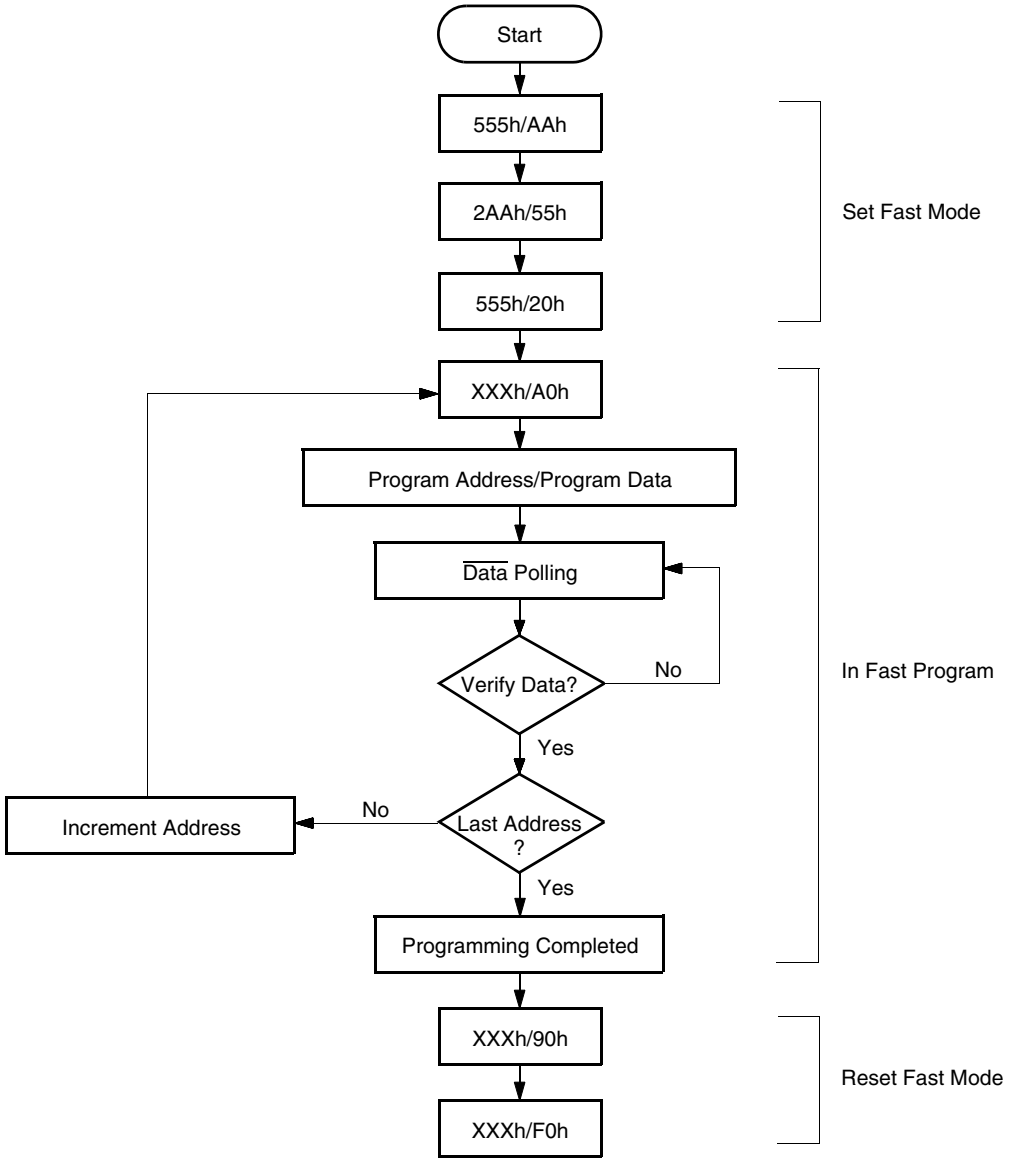
*2 : All previously protected sectors are protected.

Temporary Sector Unprotection Algorithm



Extended Sector Protection Algorithm

FAST MODE ALGORITHM



Notes : • The sequence is applied for Word (×16) mode.
• The addresses differ from Byte (× 8) mode.

Embedded Program™ Algorithm for Fast Mode

■ ORDERING INFORMATION

Part No.	Package	Access Time (ns)	Remarks
MBM29LV160TM90TN	48-pin, plastic TSOP (1) (FPT-48P-M19) (Normal Bend)	90 ns	Top Sector
MBM29LV160TM90PBT	48-ball, plastic FBGA (BGA-48P-M20)		
MBM29LV160BM90TN	48-pin, plastic TSOP (1) (FPT-48P-M19) (Normal Bend)	90 ns	Bottom Sector
MBM29LV160BM90PBT	48-ball, plastic FBGA (BGA-48P-M20)		

MBM29LV160TM/BM 90 TN

PACKAGE TYPE
TN = 48-Pin Thin Small Outline Package (TSOP(1)) Standard Pinout
PBT = 48-Ball Fine Pitch Ball Grid Array Package (FBGA)

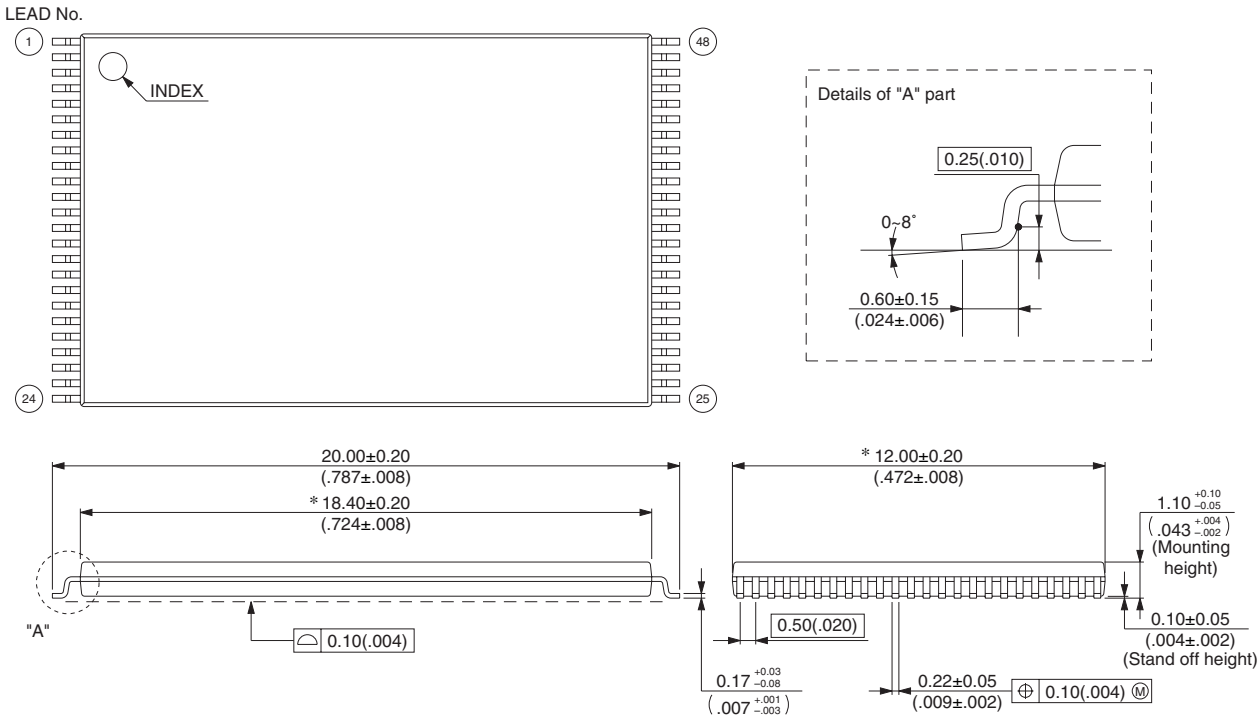
SPEED OPTION
90 = 90 ns access time

DEVICE NUMBER/DESCRIPTION
16 Mega-bit (2M × 8/1M × 16) MirrorFlash, Boot Sector
3.0 V-only Read, Program, and Erase

■ PACKAGE DIMENSIONS

48-pin plastic TSOP(1)
(FPT-48P-M19)

Note 1) * : Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15(.006)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

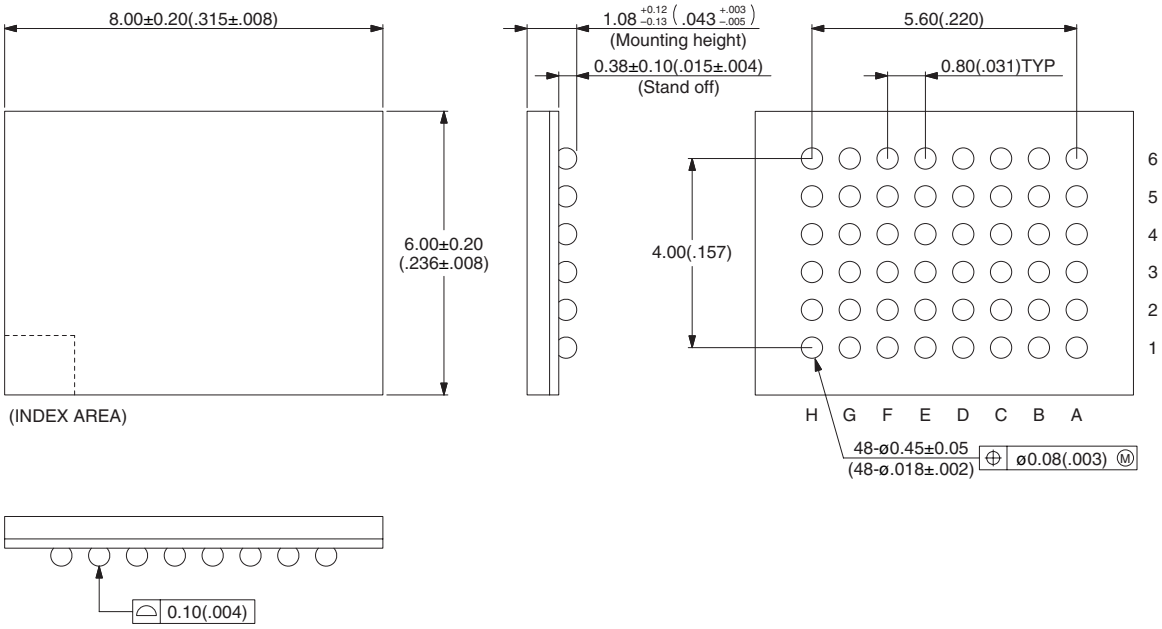


Dimensions in mm (inches)
Note : The values in parentheses are reference values.

(Continued)

(Continued)

48-ball plastic FBGA
(BGA-48P-M20)



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

MEMO

MEMO

MEMO

Revision History

Revision DS05-20906-4E（July 31, 2007）

The following comment is added.

This product has been retired and is not recommended for new designs. Availability of this document is retained for reference and historical purposes only.

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Marketing Division
Electronic Devices
Shinjuku Dai-Ichi Seimei Bldg. 7-1,
Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0721, Japan
Tel: +81-3-5322-3353
Fax: +81-3-5322-3386

http://edevice.fujitsu.com/

North and South America

FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94088-3470, U.S.A.
Tel: +1-408-737-5600
Fax: +1-408-737-5999

http://www.fma.fujitsu.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fme.fujitsu.com/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-6281-0770
Fax: +65-6281-0220

http://www.fmal.fujitsu.com/

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

http://www.fmk.fujitsu.com/

F0312

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.
The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.
Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.
The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.
Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.
If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.