DATA SHEET

OKI ASIC PRODUCTS

MG73N/74N/75N
0.22µm Customer Structure Array

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Oki Semiconductor

CONTENTS

MG73N/74N/75N

0.22 μm Customer Structure Array

DESCRIPTION

Oki's 0.22μm Application-Specific Integrated Circuit (ASIC) products are available in Customer Structured Array (CSA) architectures. The CSA-based MG75N series use a five-layer metal process on 0.22μm drawn CMOS technology. The MG73N/74N CSA series uses three and four metal layers, respectively.

The 0.22μm families provide significant performance, density, and power improvement over previous 0.25μm technologies. An innovative 4-transistor cell structure provides 20% less power and 70% more usable gates than traditional cell designs. The Oki 0.22μm family operates using 2.5-V VDD core with optimized 3-V I/O buffers.

The 3-, 4-, and 5-layer metal MG73N/74N/75N CSA series contains 21 array bases, offering up to 868 I/O pads and over 9.3M raw gates. These CSA array sizes are designed to fit the most popular quad flat pack (QFP), low profile QFPs (LQFPs), thin QFPs (TQFPs), and plastic ball grid array (PBGA).

The 3-layer-metal MG73N, 4-layer-metal MG74N and 5-layer-metal MG75N CSA series contains 21 array bases, offering a wider span of gate and I/O counts. Oki uses the Virage Components memory compiler which provides high performance, embedded synchronous single- and dual-port RAM macrocells for CSA designs. As such, the MG73N/74N/75N series is suited to memory-intensive ASICs and high-volume designs where fine-tuning of package size produces significant cost or real estate savings.

FEATURES

- 0.22μm drawn 3-, 4-, and 5-layer metal CMOS
- Optimized 2.5-V core
- Optimized 3-V I/O
- Optimized 5-V Tolerant I/O
- SOG and CSA architecture availability
- 50-ps typical gate propagation delay (for a 4x drive inverter gate with a fanout of 2 and 0 mm of wire, operating at 2.5 V)
- Over 9.3M raw gates and 868 I/O pads using 60μ staggered I/O
- User-configurable I/O with V_{SS}, V_{DD}, TTL, 3-state, and 1- to 24-mA options
- Slew-rate-controlled outputs for low-radiated noise
- Clock tree cells which reduces the maximum skew for clock signals
- Gated clock
- Low 0.2μW/MHz/gate power dissipation
- User-configurable single- and dual-port memories
- Specialized IP cores and macrocells including 32-bit ARM7TDMI CPU, phase-locked loop (PLL), and peripheral component interconnect (PCI) cells
- Floorplanning for front-end simulation, backend layout controls, and link to synthesis
- Joint Test Action Group (JTAG) boundary scan and scan path Automatic Test Pattern Generation (ATPG)
- Built-In Self Test (BIST) for memory testing
- Support for popular CAE systems including Cadence, Model Technology, Inc. (MTI), and Synopsys

MG73N/74N/75N FAMILY LISTING

EA Base Array	No. of Pads	No. of Rows	No. of Column	No. of Raw Gates	MG73N Family 3LM Usable Gates	MG74N Family 4LM Usable Gates	MG75N Family 5LM Usable Gates
MG7XNB02	68	124	360	44,640	36,158	42,408	42,408
MG7XNB04	108	206	600	123,600	86,520	117,420	117,420
MG7XNB06	148	290	848	245,920	157,389	223,787	233,624
MG7XNB08	188	374	1,088	406,912	236,009	329,599	382,497
MG7XNB10	228	456	1,336	609,216	322,884	444,728	523,926
MG7XNB12	268	540	1,576	851,040	425,520	561,686	663,811
MG7XNB14	308	624	1,824	1,138,176	534,943	694,287	830,868
MG7XNB16	348	706	2,064	1,457,184	655,733	830,595	990,885
MG7XNB18	388	790	2,312	1,826,480	785,386	986,299	1,168,947
MG7XNB20	428	874	2,552	2,230,448	914,484	1,137,528	1,360,573
MG7XNB22	468	956	2,800	2,676,800	1,070,720	1,311,632	1,552,544
MG7XNB24	508	1,040	3,040	3,161,600	1,201,408	1,485,952	1,770,496
MG7XNB26	548	1,124	3,288	3,695,712	1,330,456	1,663,070	1,958,727
MG7XNB28	588	1,206	3,528	4,254,768	1,489,169	1,829,550	2,169,932
MG7XNB30	628	1,290	3,776	4,871,040	1,656,154	1,997,126	2,435,520
MG7XNB32	668	1,374	4,016	5,517,984	1,820,935	2,207,194	2,648,632
MG7XNB34	708	1,456	4,264	6,208,384	1,986,683	2,421,270	2,855,857
MG7XNB36	748	1,540	4,504	6,936,160	2,150,210	2,635,741	3,121,272
MG7XNB38	788	1,624	4,752	7,717,248	2,315,174	2,855,382	3,395,589
MG7XNB40	828	1,706	4,992	8,516,352	2,469,742	3,065,887	3,662,031
MG7XNB42	868	1,790	5,240	9,379,600	2,626,288	3,282,860	3,939,432

ARRAY ARCHITECTURE

The primary components of a 0.22μm MG73N/74N/75N circuit include:

- I/O base cells
- 60μm pad pitch
- Configurable I/O pads for VDD, VSS, or I/O (optimized 3-V I/O)
- VDD and VSS pads dedicated to wafer probing
- Separate power bus for output buffers
- Separate power bus for internal core logic and input buffers
- Core base cells containing N-channel and P-channel pairs, arranged in column of gates
- Isolated gate structure for reduced input capacitance and increased routing flexibility
- Each array has 24 dedicated corner pads for power and ground use during wafer probing, with four pads per corner. The arrays also have separate power rings for the internal core functions (VDDCORE and VSS) and output drive transistors (VDDO and VSSO).

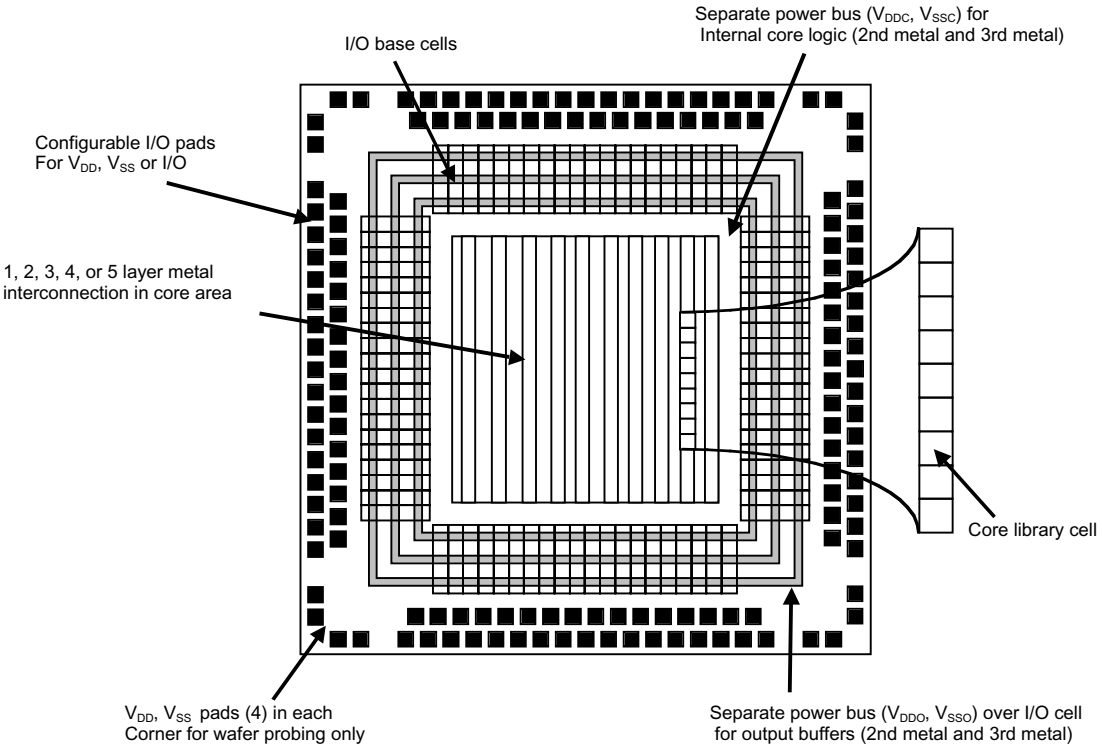


Figure 1. MG75N Array Architecture

MG73N/74N/75N CSA LAYOUT METHODOLOGY

The procedure to design, place, and route a CSA follows.

1. Select suitable base array frame from the available predefined sizes. To select an array size:
   - Identify macrocell functions required and minimum array size to hold macrocell functions.
   - Add together all the area occupied by the required random logic and macrocells and select the optimum array.
2. Make a floor plan for the design's megacells.
   - Oki Design Center engineers verify the master slice and review simulation.
   - Oki Design Center or customer engineers floorplan the array using Oki's supported floorplanner and customer performance specifications.
   - Using Oki CAD software, Design Center engineers remove the SOG transistors and replace them with diffused memory macrocells to the customer's specifications *Figure 2* shows an array base after placement of the optimized memory macrocells.

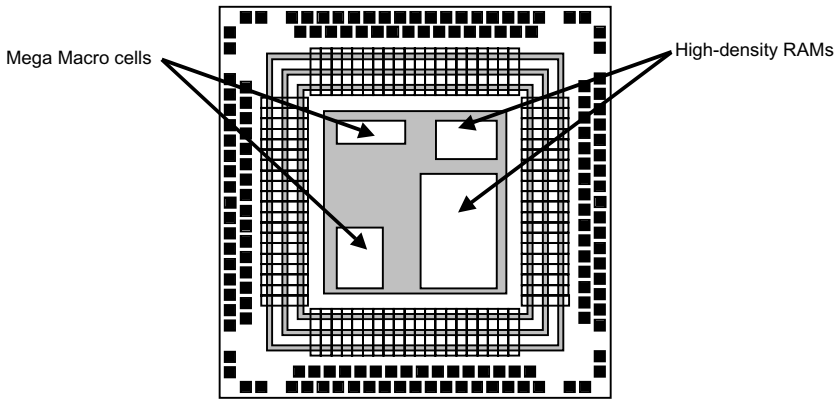


Figure 2. Optimized Memory Macrocell Floor Plan

3. Place and route logic into the array transistors.
   - Oki Design Center engineers use layout software and customer performance specifications to connect the random logic and optimized memory macrocells *Figure 3* marks the area in which placement and routing is performed with cross hatching.

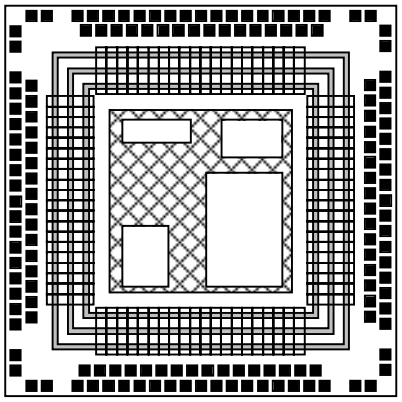


Figure 3. Random Logic Place and Route

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (Vss = 0 V, Tj = 25°C) [1]

Parameter		Symbol	Condition	Rated Value	Unit
Supply Voltage	Core	V_{DDCORE}	—	- 0.3 ~ +3.6	V
	I/O	V_{DDIO}	—	- 0.3 ~ +4.6	
Input Voltage	Normal buffer	V_I	—	- 0.3 ~ V_{DDIO} +0.3	
	5-V Tolerant Buffer		V_{DDIO} = 3.0 ~ 3.6 V	- 0.3 ~ +6.0	
			V_{DDIO} < 3.0 V	- 0.3 ~ V_{DDIO} +0.3	
Output Voltage	Normal buffer	V_O	—	- 0.3 ~ V_{DDIO} +0.3	
	5-V Tolerant Buffer		V_{DDIO} = 3.0 ~ 3.6 V	- 0.3 ~ +6.0	
			V_{DDIO} < 3.0 V	- 0.3 ~ V_{DDIO} +0.3	
Input Current [2]		I_I	—	- 10 ~ +10	mA
Output Current	1 mA buffer	I_O	—	- 4 ~ +4	
	2 mA buffer			- 9 ~ +9	
	4 mA buffer			- 18 ~ +18	
	6 mA buffer			- 18 ~ +18	
	8 mA buffer			- 18 ~ +18	
	12 mA buffer			- 36 ~ +36	
	24 mA buffer			- 36 ~ +36	
Storage Temperature		T_{STG}	—	- 65 ~ +150	°C

Notes:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions in the other specifications of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Do not drive inputs while VDD is low or 0V. Driving any pin with a positive signal while VCC is low or 0V would result in a lot of current through an ESD protection diode and cause device failure.

Recommended Operating Conditions (Vss = 0 V)

Paramater	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}core	2.25	2.5	2.75	V
	V_{DDIO}	3	3.3	3.6	
Junction Temperture	Tj	- 40	—	85	°C
Input rise time/ fall time	tr, tf	—	2	20	ns

DC Characteristics (V_{DDCORE} = 2.5V ± 0.25 V, V_{DDIO} = 3.3V ± 0.3 V, VSS = 0 V, Tj = - 40 ~ +85°C)

Parameter		Symbol	Condition		Rated Value			Unit
					Min	Typ[1]	Max	
High-level Input Voltage	Normal buffer	V_{IH}	TTL level Input		2	—	V_{DD}+0.3	V
	5V Tolerant				2	—	5.5	
Low-level Input Voltage	Normal buffer	V_{IL}	TTL level Input		- 0.3	—	0.8	
	5V Tolerant				- 0.3	—	0.8	
TTL-level Schmitt Trigger Input buffer		Vt+	—		—	—	2.1	
Threshold Voltage		Vt -			0.7	—	—	
(Normal buffer)		DVt	Vt+ – Vt -		0.4	—	—	
TTL-level Schmitt Trigger Input buffer		Vt+	—		—	—	2.1	
Threshold Voltage		Vt -			0.7	—	—	
(5V Tolerant buffer)		DVt	Vt+ – Vt -		0.4	—	—	
High-level Output Voltage (Normal buffer)		V_{OH}	I_{OH} = –100 μA		V_{DDIO} - 0.2	—	—	
			I_{OH} = -1, - 2, - 4, - 6, - 8, - 12, - 24 mA		2.4	—	—	
High-level Output Voltage (5V Tolerant buffer)			I_{OH} = - 100 μA		V_{DDIO} - 0.2	—	—	
			I_{OH} = - 1, - 2, - 4, - 6, - 8, - 12, - 24 mA		2.4	—	—	
Low-level Output Voltage (Normal buffer)		V_{OL}	I_{OL} = 100 μA		—	—	0.2	
			I_{OL} = 1, 2, 4, 6, 8, 12, 24 mA		—	—	0.4	
Low-level Output Voltage (5V Tolerant buffer)			I_{OL} = 100 μA		—	—	0.2	
			I_{OL} = 1, 2, 4, 6, 8, 12, 24 mA		—	—	0.4	
High-level Input current (Normal buffer)		I_{IH}	V_{IH} = V_{DD}io		—	—	10	μA
				(50 kΩ pull down)	10	73	200	
High-level Input current (5V Tolerant)			V_{IH} = V_{DD}io		—	—	10	
				(50 kΩ pull down)	10	73	200	
			V_{IH} = 5.5 V		—	—	10	
				(3 k/50 kΩ pull up)	—	—	100	
				(50 kΩ pull down)	10	73	200	
Low-level Input current (Normal buffer)		I_{IL}	V_{IL} = V_{SS}		-10	—	—	
				(50 kΩ pull up)	- 200	- 73	-10	
				(3 kΩ pull up)	- 3.3	- 1.3	-0.3	mA
Low-level Input current (5V Tolerant)			V_{IL} = V_{SS}		- 10	—	—	μA
				(50 kΩ pull up)	- 200	- 73	-10	
				(3 kΩ pull up)	- 3.3	- 1.3	-0.3	mA

1. VDD_{CORE} = 2.5 V, V_{DDIO} = 3.3 V, and T_j = 25°C on a typical process.

AC Characteristics (VDDcore = 2.5 V, V_{SS} = 0 V, Tj = +25 °C)

Paramater		Driving Type	Condition[1][2]	Rated Value[3]	Unit
Internal gate propagation delay	Inverter	1X	F/O = 2, L = 0 mm	0.073	ns
		2X		0.062	
		4X		0.05	
	2-input NAND	1X		0.094	
		2X		0.077	
		4X		0.067	
	Inverter	1X	F/O = 2, Standard wire length	0.317	
		2X		0.224	
		4X		0.133	
	2-input NAND	1X		0.376	
		2X		0.218	
		4X		0.139	
Toggle Frequency			F/O = 1, L = 0 mm	1830	MHz

1. Input transition time in 0.15 ns / 2.5 V (Internal gate)
2. Typical condition is V DDCORE = 2.5 V, V DDIO = 3.3 V and Tj = 25 °C for a typical process.
3. Rated value is calculated as an average of the L-H and H-L delay times of each macro type on a typical process.

AC Characteristics (I/O V_{DD} = 3.3 V, V_{SS} = 0 V, T_j = 25 °C)

Paramater		Driving Type	Condition[1][2]	Rated Value[3]	Unit
Input buffer propagation delay	TTL-level normal buffer		F/O = 2 Standard wire length	0.391	ns
	TTL-level 5V Tolerant buffer			0.708	
Output buffer propagation delay	push-pull Normal output buffer	4 mA	CL = 20 pF	1.88	
		8 mA	CL = 50 pF	2.072	
		12 mA	CL = 100 pF	2.597	
	Tri-state 5V tolerant output buffer	4 mA	CL = 20 pF	2.193	
		8 mA	CL = 50 pF	2.689	
		12 mA	CL = 100 pF	2.82	
Output buffer traisition time[4]	push-pull Normal output buffer	12 mA	CL = 100 pF	3.524 (r) 3.526 (f)	
	Tri-state 5V tolerant output buffer	12 mA	CL = 100 pF	3.571 (r) 3.466 (f)	

1. Input transition time in , 0.2ns / 3.3V(Input buffer)
2. CL = 100 pF
3. Rated value is calculated as an average of the L-H and H-L delay times of each macro type on a typical process.
4. Output rising and falling times are both specified over a 10 to 90% range.

MACRO LIBRARY

Oki Semiconductor supports a wide range of macrocells and macrofunctions, ranging from simple hard macrocells for basic Boolean operations to large, user-parameterizable macrofunctions. The following figure illustrates the main classes of macrocells and macrofunctions available.

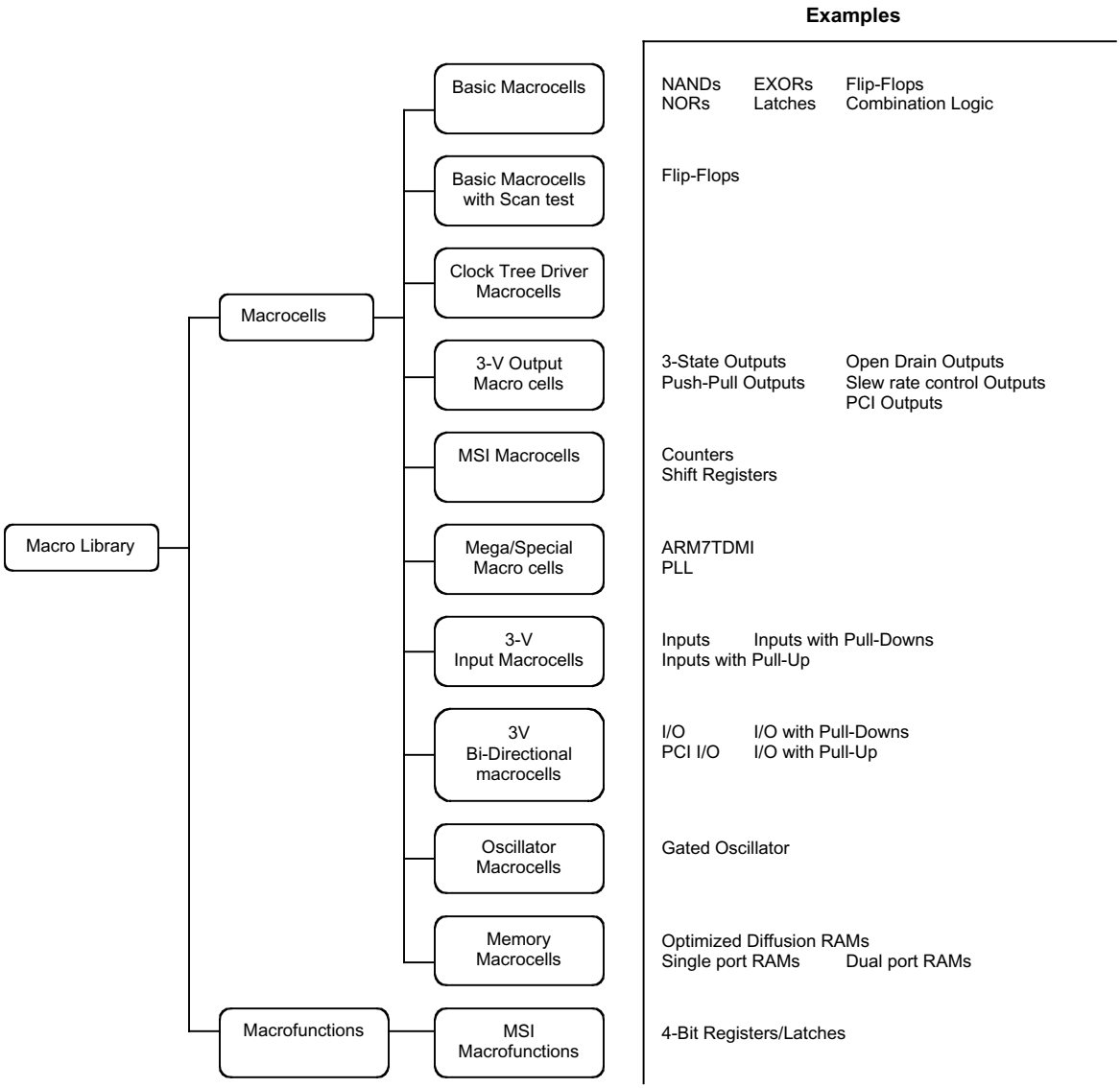


Figure 4. OKI Macrocell and Macrofunction Library

Macrocells for Driving Clock Trees

Oki offers the Envisia™ clock-tree clock tree generator (CT-Gen). The CT-Gen generates post placement buffered clock trees that help minimize problems associated with clock skew. CT-Gen optimizes the following when it generates clock trees:

- Maximum load, maximum transition, wire self-heat, and hot electron constraints
- Maximum insertion delay
- Maximum skew
- Clock tree size (if the above constraints are met)
- Minimum insertion delay (satisfied by padding the root)

OKI ADVANCED DESIGN CENTER CAD TOOLS

Oki's advanced design center CAD tools include support for the following:

- Floorplanning for front-end simulation and back-end layout control
- Clock tree structures improve first-time silicon success by eliminating clock skew problems
- JTAG Boundary scan support
- Power calculation which predicts circuit power under simulation conditions to accurately model package requirements

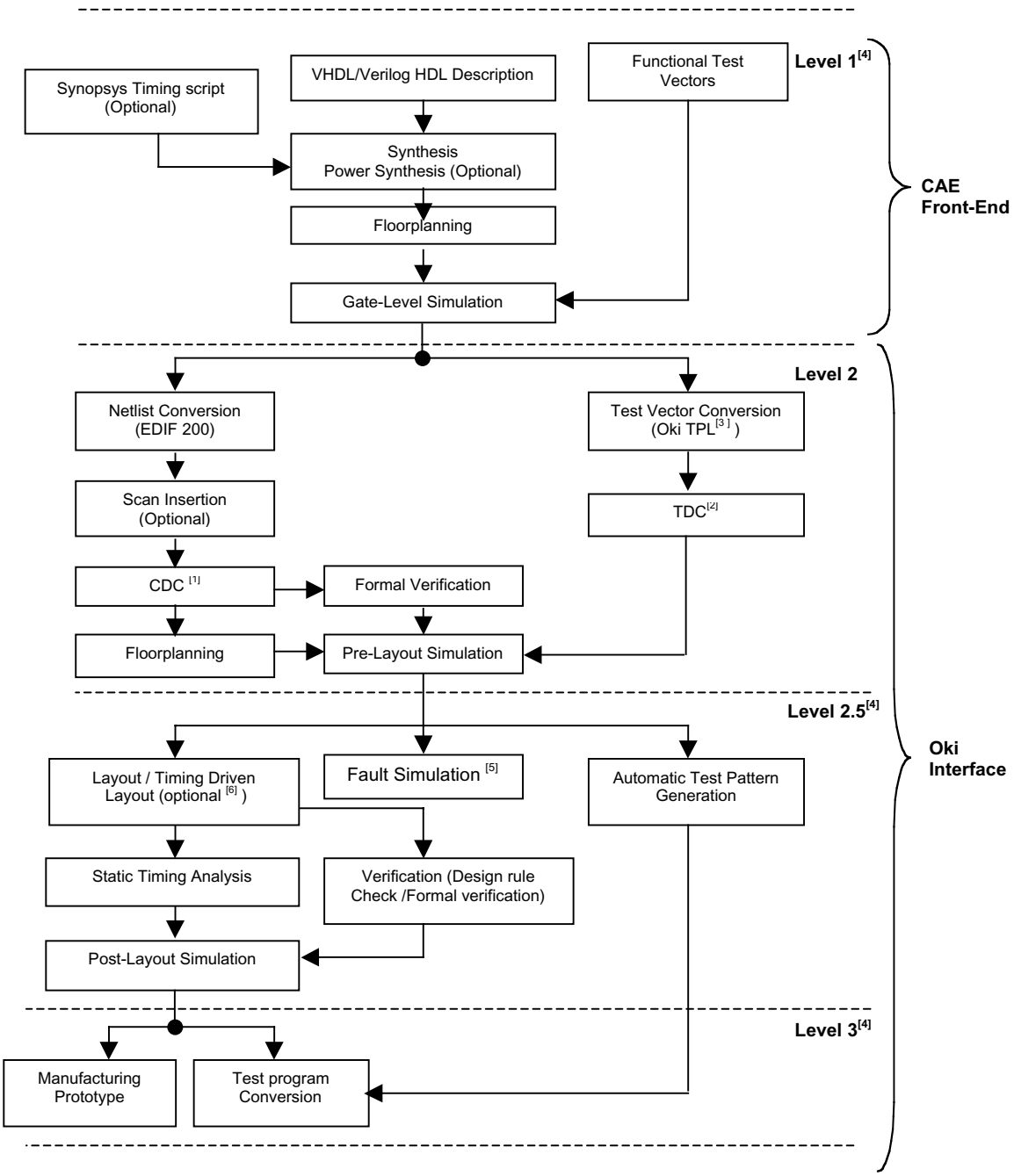
Oki Design Kit Availability

Vender	Platform	Operating System[1]	Vender Software [1]	Description
Cadence	Sun® [2]	Solaris	Ambit Buildgates NC_Verilog Verilog_XL	Design Synthesis Design Simulation Design Simulation
Syntest	Sun® [2]	Solaris	Turbo Fault	Fault Simulation
Synopsys	Sun® [2]	Solaris	Design Compiler Ultra + Tetramax/ATPG Primetime DFT Compiler/Test Compiler RTL Analyzer VCS	Design Synthesis Test Synthesis Static Timing Analysis Test Synthesis RTL Check Design Simulation
Model Technology Inc. (MTI)	Sun® [2] NT	Solaris WinNT4.0	MTI-VHDL MTI-Verilog	Design Simulation Design Simulation
Oki	Sun® [2]	Solaris	Floorplanner	Floor Planning
Verplex	Sun® [2]	Solaris	Conformal	Formal Verification

1. Contact Oki Application Engineering for current software versions
2. Sun or Sun-compatible

DESIGN PROCESS

The following figure illustrates the overall IC design process, also indicating the three main interface points between external design houses and Oki ASIC Application Engineering.



[1] Oki s Circuit Data Check program (CDC) verifies logic design rules
[2] Oki s Test Data Check program (TDC) verifies test vector rules
[3] Oki s Test Pattern Language (TPL)
[4] Ultimate Customer-OKI design Interface available in addition to standard level 2
[5] Standard design process Includes fault simulation
[6] Requires Synopsys timing script for Oki Timing driven layout

Figure 5. Oki s Design Process

AUTOMATIC TEST PATTERN GENERATION

Oki's 0.22μm ASIC technologies support ATPG using full scan-path design techniques, including the following:

- Increases fault coverage ≥95%
- Uses Synopsys Test Compiler and Tetramax
- Automatically inserts scan structures
- Connects scan chains
- Traces and reports scan chains
- Checks for rule violations
- Generates complete fault reports
- Allows multiple scan chains
- Supports vector compaction

ATPG methodology is described in detail in Oki's *Scan Path Application Note*.

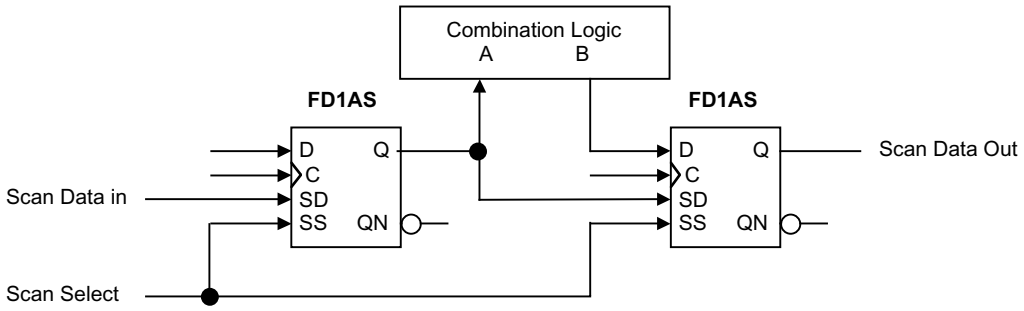


Figure 6. Full Scan Path Configuration

FLOORPLANNING DESIGN FLOW

Oki offers the floorplanning tool (OKI FP) for high-density ASIC design. The three main purposes for Oki's floorplanning tool is to:

- Ensure conformance of critical circuit performance specifications
- Shorten overall design TAT
- Hierarchical Layout

In a traditional design approach with synthesis tools, timing violations after pre layout simulation are fixed by manual editing of the net list. This process is difficult and time consuming. Also, there is no physical cluster information provided in the synthesis tool, and so it is difficult to synthesize logic using predicted interconnection delay due to wire length. Synthesis tools may therefore create over-optimized result Floorplanning allows designers to control parasitic capacitance in a circuit by participating in the physical design process. Designers can partition their ASIC circuit in the most efficient hierarchical manner, and/or specify the exact placement of critical timing paths to guarantee high-speed performance. Floorplanning also allows the reduction of layout iterations, minimizing a designs overall TAT. As parasitic capacitance dominates a circuit's timing in sub-micron technologies, an accurate capacitance estimation is crucial for accurate pre-layout timing simulation. Quite often, designers have to iterate the circuit layout because unexpected post-layout capacitance causes unacceptable circuit performance.

More information on Oki's floorplanning capabilities is available in Oki's Application Note, *Using Oki's Floorplanner: Standalone Operation and Links to Synopsys*.

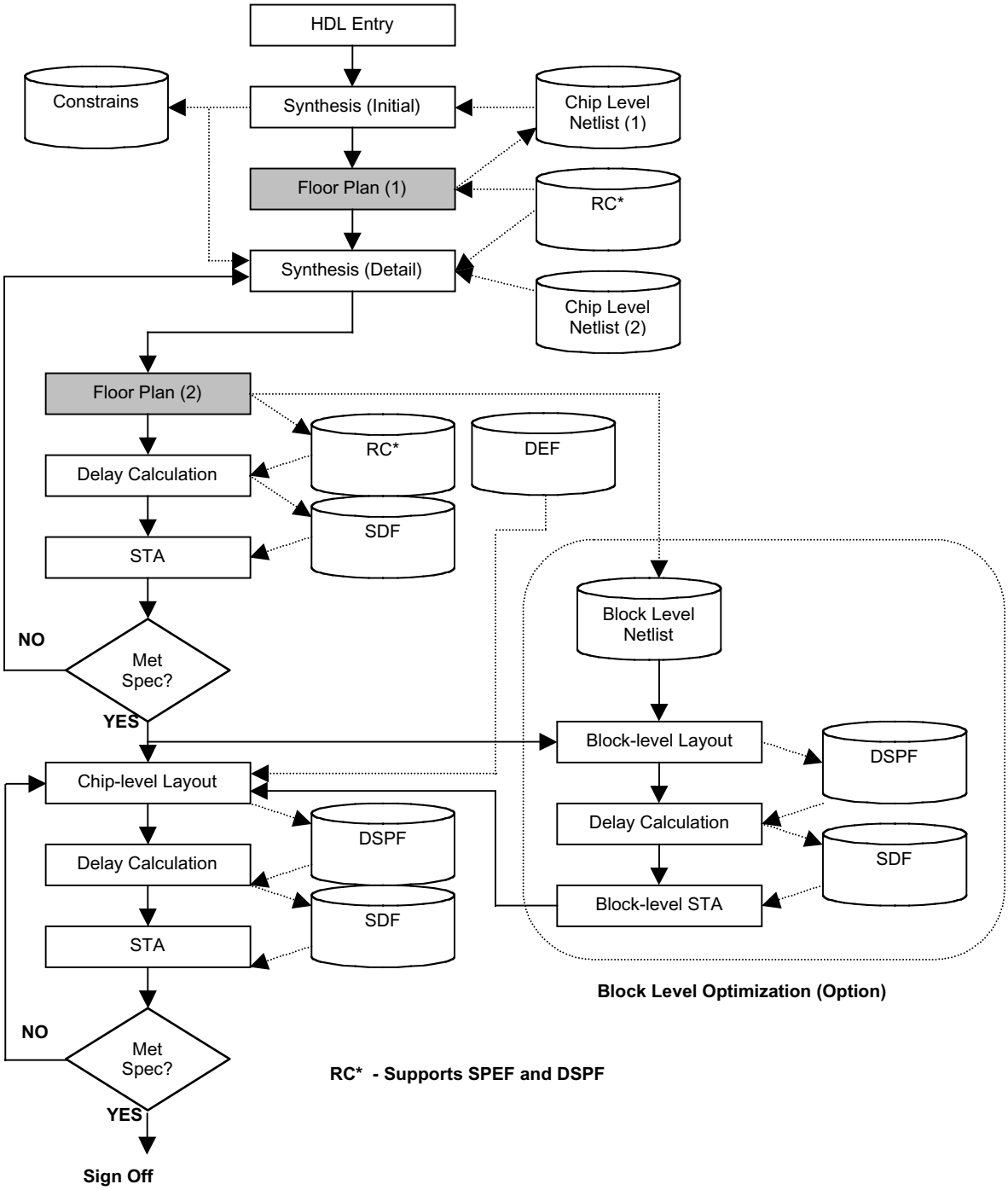


Figure 7. Design Flow

IEEE JTAG BOUNDARY SCAN SUPPORT

Boundary scan offers efficient board-level and chip-level testing capabilities. Benefits resulting from incorporating boundary-scan logic into a design include:

- Improved chip-level and board-level testing and failure diagnostic capabilities
- Support for testing of components with limited probe access
- Easy-to-maintain testability and system self-test capability with on-board software
- Capability to fully isolate and test components on the scan path
- Built-in test logic that can be activated and monitored
- An optional Boundary Scan Identification (ID) Register

Oki's boundary scan methodology meets the JTAG Boundary Scan standard, IEEE 1149.1-1990. Oki supports boundary scan on both Sea of Gates (SOG) and Customer Structured Array (CSA) ASIC technologies. Either the customer or Oki can perform boundary-scan insertion. More information is available in Oki's *JTAG Boundary Scan Application Note*. (Contact the Oki Application Engineering Department for interface options.)

PACKAGE OPTIONS

TQFP, LQFP and QFP Package Menu

Product Name	I/O Pads[1]	TQFP				LQFP			QFP	
		64	80	100	128	144	176	208	64	208
MG7xNB02	68									
MG7xNB04	108			●						
MG7xNB06	148			●	●					
MG7xNB08	188			●	●				●	
MG7xNB10	228	●	●	●	●	●	●	●	●	●
MG7xNB12	268	●	●	●	●	●	●	●	●	●
MG7xNB14	308	●	●	●	●	●	●	●	●	●
MG7xNB16	348		●	●		●	●	●	●	●
MG7xNB18	388		●	●		●	●	●	●	●
MG7xNB20	428		●	●		●		●	●	
MG7xNB22	468		●	●		●	●	●	●	●
MG7xNB24	508			●		●	●	●	●	●
MG7xNB26	548			●		●	●	●	●	●
MG7xNB28	588					●	●	●		●
MG7xNB30	628					●	●	●		●
MG7xNB32	668					●	●	●		●
MG7xNB34	708					●	●	●		
MG7xNB36	748					●	●	●		
MG7xNB38	788							●		
MG7xNB40	828							●		
MG7xNB42	868							●		
Body size (mm) ˚		10 x 10	12 x 12	14 x 14	14 x 14	20 x 20	24 x 24	28 x 28	14 x 14	28 x 28
Lead Pitch (mm) ˚		0.5	0.5	0.5	0.4	0.5	0.5	0.5	0.8	0.5

1. I/O Pads can be used for input, output, bi-directional, power, or ground

● = Available now.

PBGA and MBGA Package Menu

Product Name	I/O Pads[1]	PBGA 256	PBGA 352	PBGA 420
MG7xNB02	68			
MG7xNB04	108			
MG7xNB06	148			
MG7xNB08	188			
MG7xNB10	228			
MG7xNB12	268	•		
MG7xNB14	308	•		
MG7xNB16	348	•	•	
MG7xNB18	388	•	•	•
MG7xNB20	428	•	•	•
MG7xNB22	468	•	•	•
MG7xNB24	508	•	•	•
MG7xNB26	548	•	•	•
MG7xNB28	588	•	•	•
MG7xNB30	628	•	•	•
MG7xNB32	668	•	•	•
MG7xNB34	708		•	•
MG7xNB36	748		•	
MG7xNB38	788		•	
MG7xNB40	828		•	
MG7xNB42	868		•	
Body size (mm)		27 x 27	35 x 35	35 x 35
Ball pitch (mm)		1.27	1.27	1.27
Ball count		256	352	420
Signal I/O		231	304	352
Power Ball		12	16	32
GND Ball		13	32	36

1. I/O Pads can be used for input, output, bi-directional, power, or ground

• = Available now.

The information contained herein can change without notice owing to product and/or technical improvements.

Please make sure before using the product that the information you are referring to is up-to-date.

The outline of action and examples of application circuits described herein have been chosen as an explanation of the standard action and performance of the product. When you actually plan to use the product, please ensure that the outside conditions are reflected in the actual circuit and assembly designs.

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