DATA SHEET

O K I A S I C P R O D U C T S

MG74K/75K/76K
0.15µm Customer Structured Arrays

March 2003

Oki Semiconductor

CONTENTS

Oki Semiconductor

MG74K/75K/76K

0.15µm Customer Structured Arrays

DESCRIPTION

Oki's 0.15µm Application-Specific Integrated Circuit (ASIC) products are available in Customer Structured Array (CSA) architectures. The CSA-based MG74K/75K/76K series uses a six-layer metal process on 0.15µm drawn CMOS technology.

The MG74K/75K/76K series uses four, five, and six layer metal, respectively.

The 0.15µm CSA family provides significant performance, density, and power improvement over previous 0.16µm technologies. Using an innovative 4-transistor cell structure, the MG74K/75K/76K offers a 30% speed increase, consumes 25% less power, and has 20% higher density than traditional cell designs. The 0.15µm CSA family operates using 1.5V VDD core with optimized 3.3V I/O and 5V tolerant I/O buffers. The 4-, 5-, and 6-layer metal MG74K/75K/76K series contains 21 base arrays, offering up to 868 I/O pads and over 25M raw gates. These CSA sizes are designed to fit the most popular quad flat pack (QFP), low profile QFPs (LQFPs), thin QFPs (TQFPs), thin fine pitch land grid array (TFLGAs), low profile fine pitch ball grid array (LFBGAs), and plastic ball grid array (PBGA) packages.

The MG74K/75K/76K series is ideally suited for memory-intensive ASICs and high volume designs where fine tuning of package size produces significant cost and/or real-estate savings.

FEATURES

- 0.15µm drawn 4-, 5-, and 6-layer metal CMOS
- Optimized 1.5V core
- Optimized 3.3V I/O
- Optimized 5V Tolerant I/O
- 28-ps typical gate propagation delay (for a 4x-drive inverter gate with a fanout of 2 and 0 mm of wire, operating at 1.5V)
- Over 25M raw gates and 868 I/O pads using 60µm staggered I/O
- User-configurable I/O with V_{SS}, V_{DD}, CMOS, TTL, and 2- to 24-mA options
- Slew-rate-controlled outputs for low-radiated noise
- Clock tree cells that reduce the maximum skew for clock signals
- Low 44 nW/MHz/gate power dissipation
- User-configurable single- and dual-port memories
- Specialized IP cores and macrocells including 32-bit ARM CPU, phase-locked loop (PLL), and peripheral component interconnect (PCI) cells
- Floorplanning for front-end simulation, back-end layout controls, and link to synthesis
- Joint Test Action Group (JTAG) boundary scan and scan path Automatic Test Pattern Generation (ATPG)
- Built-in Self Test (BIST) for memory test
- Support for popular CAE systems including Cadence, Model Technology, Inc. (MTI), and Synopsys

MG74K/75K/76K FAMILY LISTING

CSA Base Array	No. of Pads	No. of Raw Gates	MG74K Family 4LM Usable Gates	MG75K Family 5LM Usable Gates	MG76K Family 6LM Usable Gates
MG7xKB02	68	221,184	161,464	188,006	205,701
MG7xKB04	108	481,664	320,307	370,881	409,414
MG7xKB06	148	848,256	517,436	602,262	661,640
MG7xKB08	188	1,317,888	738,017	869,806	955,469
MG7xKB10	228	1,890,560	992,544	1,153,242	1,304,486
MG7xKB12	268	2,555,840	1,265,141	1,482,387	1,686,854
MG7xKB14	308	3,351,040	1,574,989	1,843,072	2,111,155
MG7xKB16	348	4,233,600	1,862,784	2,222,640	2,540,160
MG7xKB18	388	5,204,288	2,185,801	2,628,165	2,992,466
MG7xKB20	428	6,291,456	2,516,582	3,051,356	3,491,758
MG7xKB22	468	7,481,664	2,843,032	3,478,974	4,040,099
MG7xKB24	508	8,774,912	3,202,843	3,948,710	4,606,829
MG7xKB26	548	10,150,400	3,552,640	4,415,424	5,176,704
MG7xKB28	588	11,681,728	3,913,379	4,906,326	5,782,455
MG7xKB30	628	13,284,864	4,251,156	5,380,370	6,376,735
MG7xKB32	668	14,991,040	4,572,267	5,846,506	7,045,789
MG7xKB34	708	16,773,504	4,948,184	6,373,932	7,631,944
MG7xKB36	748	18,684,288	5,325,022	6,819,765	8,314,508
MG7xKB38	788	20,698,112	5,691,981	7,347,830	9,003,679
MG7xKB40	828	22,783,808	6,037,709	7,860,414	9,683,118
MG7xKB42	868	25,051,264	6,388,072	8,392,173	10,396,275

ARRAY ARCHITECTURE

The primary components of a 0.15µm MG74K/75K/76K circuit include:

- I/O base cells
- 60µm pad pitch
- Configurable I/O pads for V_{DD}, V_{SS}, or I/O (optimized 3.3V I/O, 5V tolerant I/O)
- V_{DD} and V_{SS} pads dedicated to wafer probing
- Separate power bus for output buffers
- Separate power bus for internal core logic and input buffers
- Core base cells containing N-channel and P-channel pairs, arranged in column of gates
- Isolated gate structure for reduced input capacitance and increased routing flexibility
- Innovative 4-transistor core cell architecture, licensed from In-Chip Systems, Inc

Each array has 24 dedicated corner pads for power and ground use during wafer probing, with six pads per corner. The arrays also have separate power rings for the internal core functions (V_{DDC} and V_{SSC}) and output drive transistors (V_{DDO} and V_{SSO}).

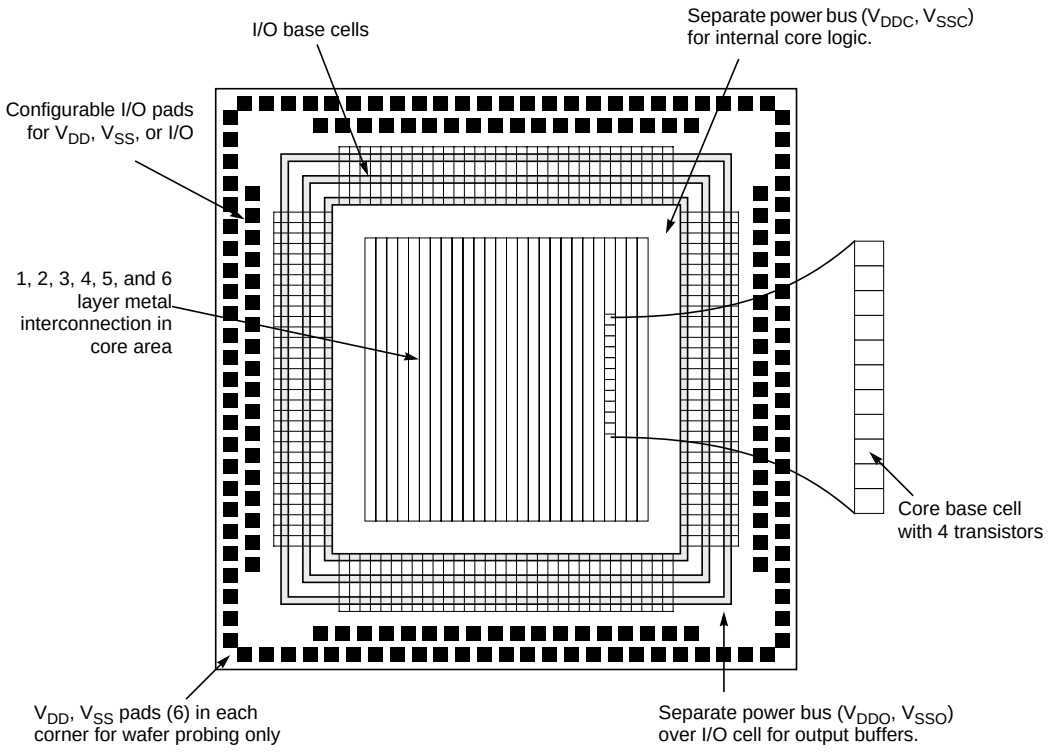


Figure 1. MG76K Array Architecture

MG74K/75K/76K CSA Layout Methodology

The procedure to design, place, and route a CSA is as follows.

1. Select suitable base array frame from the available predefined sizes. To select a base array size:
   - Identify macrocell functions required and minimum array size to hold macrocell functions.
   - Add together all the area occupied by the required random logic and macrocells and select the optimum array.
2. Make a floor plan for the design's megacells.
   - Oki Design Center engineers verify the master slice and review simulation.
   - Oki Design Center or customer engineers floorplan the array using Oki's supported floor-planner or Cadence DP3 and customer performance specifications.
   - Using Oki CAD software, Design Center engineers remove the SOG transistors and replace them with diffused memory macrocells to the customer's specifications.

Figure 2 shows a base array after placement of the optimized memory macrocells.

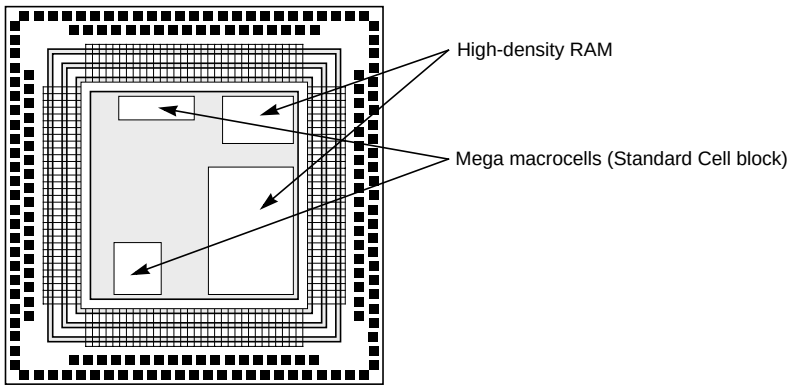


Figure 2. Optimized Memory Macrocell Floor Plan

3. Place and route logic into the array transistors.
   - Oki Design Center engineers use layout software and customer performance specifications to connect the random logic and optimized memory macrocells.

Figure 3 marks the area in which placement and routing is performed with cross hatching.

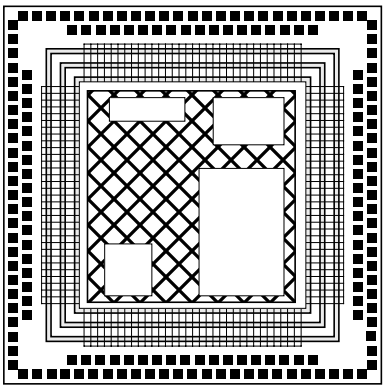


Figure 3. Random Logic Place and Route

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (V_{SS} = 0 V, T_J = 25°C) [1]

Parameter		Symbol	Conditions	Rated Value	Unit
Power supply voltage	Core	V_{DDCORE}	-	-0.3 ~ +2.0	V
	I/O	V_{DDIO}	-	-0.3 ~ +4.6	
Input voltage	(Normal Buffer)	V_I	-	-0.3 ~ V_{DDIO}+0.3	
	(5V Tolerant Buffer)		V_{DDIO} = +3.0 ~ +3.6V	-0.3 ~ +6.0	
			V_{DDIO} < +3.0V	-0.3 ~ V_{DDIO}+0.3	
Output voltage	(Normal Buffer)	V_O	-	-0.3 ~ V_{DDIO}+0.3	
	(5V Tolerant Buffer)		V_{DDIO} = +3.0 ~ +3.6V	-0.3 ~ +6.0	
			V_{DDIO} < +3.0V	-0.3 ~ V_{DDIO}+0.3	
Input current [2]	-	I_I	-	-10 ~ +10	mA
Output current	2mA buffer	I_O	-	-8 ~ +8	
	4mA buffer		-	-16 ~ +16	
	6mA buffer		-	-24 ~ + 24	
	8mA buffer		-	-32 ~ + 32	
	10mA buffer		-	-42 ~ +42	
	12mA buffer		-	-42 ~ +42	
	14mA buffer		-	-42 ~ +42	
	16mA buffer		-	-42 ~ +42	
	24mA buffer		-	-42 ~ +42	
Storage temperature	-	T_{stg}	-	-65 ~ +150	˚C

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions in the other specifications of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Do not drive inputs while V_{DD} is low or 0V. Driving any pin with a positive signal while V_{DD} is low or 0V can result in a current surge through the ESD protection diode and cause device failure.

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter		Symbol	Rated Value			Unit
			Min	Typ.	Max	
Power supply voltage	Core	V_{DDCORE}	+1.35	+1.5	+1.65	V
	I/O	V_{DDIO}	+3.0	+3.3	+3.6	
Junction temperature		T_j [1]	-40	-	+85	˚C
Input rise time/fall time		t_r, t_f	-	2	20	ns

1. Maximum junction temperature (T_j max) must be equal to or less than 125°C. If T_j is over 85°C, please refer to the DC Characteristics table with the tempature range T_j = -40°C to +125°C.

DC Characteristics (V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, V_{SS} = 0 V, T_j = -40 to +85°C)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min.	Typ. [1]	Max.	
High-level input voltage	V_{IH}	TTL input (normal)	2.0	–	V_{DDIO} + 0.3	V
		TTL input (5V Tolerant)	2.0	–	5.5	
Low-level input voltage	V_{IL}	TTL input (normal)	-0.3	–	0.8	
		TTL input (5V Tolerant)	-0.3	–	0.8	
TTL- level Schmitt Trigger input buffer Threshold voltage	V_{t+}	TTL normal input	–	–	2.1	
	V_{t-}		0.7	–	–	
	ΔV_t	Vt+ - Vt-	0.25	–	–	
High-level output voltage (Normal buffer)	V_{OH}	I_{OH} = -100 µA	V_{DDIO} - 0.2	–	–	
		I_{OH} = -2, -4, -6, -8, -10, -12, -14, -16, -24 mA	2.4	–	–	
High-level output voltage (5V Tolerant buffer)		I_{OH} = -100 µA	V_{DDIO} - 0.2	–	–	
		I_{OH} = -2, -4, -6, -8, -10, -12, -14, -16, -24 mA	2.4	–	–	
Low-level output voltage (Normal buffer)	V_{OL}	I_{OL} = 100 µA	–	–	0.2	
		I_{OL} = 2, 4, 6, 8, 10, 12, 14, 16, 24 mA	–	–	0.4	
Low-level output voltage (5V Tolerant buffer)		I_{OL} = 100 µA	–	–	0.2	
		I_{OL} = 2, 4, 6, 8, 10, 12, 14, 16, 24 mA	–	–	0.4	
High-level input current (Normal buffer)	I_{IH}	V_{IH} = V_{DDIO}	–	–	10	µA
		V_{IH} = V_{DDIO} (50kΩ pull-down)	10	–	200	
High-level input current (5V Tolerant buffer)		V_{IH} = V_{DDIO}	–	–	10	
		V_{IH} = 5.5V	–	–	10	
Low-level input current (Normal buffer)	I_{IL}	V_{IL} = V_{SS}	-10	–	–	
		V_{IL} = V_{SS} (50kΩ pull-up)	-200	–	-10	
Low-level input current (5V Tolerant buffer)		V_{IL} = V_{SS}	-10	–	–	
3-state output leakage current (Normal buffer)	I_{OZH}	V_{OH} = V_{DDIO}	–	–	10	
		V_{OH} = V_{DDIO} (50kΩ pull-down)	10	–	200	
	I_{OZL}	V_{OL} = V_{SS}	-10	–	–	
		V_{OL} = V_{SS} (50kΩ pull-up)	-200	–	-10	
3-state output leakage current (5V Tolerant buffer)	I_{OZH}	V_{OH} = V_{DDIO}	–	–	10	µA
		V_{IH} = 5.5V	–	–	10	
	I_{OZL}	V_{OL} = V_{SS}	-10	–	–	

1. Typical condition is V_{DDCORE} = 1.5V, V_{DDIO} = 3.3V, and T_j = 25°C on a typical process.

DC Characteristics (V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, V_{SS} = 0 V, T_j = -40 to +125°C)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min.	Typ. [1]	Max.	
High-level input voltage	V_{IH}	TTL input (normal)	2.0	–	V_{DDIO} + 0.3	V
		TTL input (5V Tolerant)	2.0	–	5.5	
Low-level input voltage	V_{IL}	TTL input (normal)	-0.3	–	0.8	
		TTL input (5V Tolerant)	-0.3	–	0.8	
TTL- level Schmitt Trigger input buffer Threshold voltage	V_{t+}	TTL normal input	–	–	2.1	
	V_{t-}		0.7	–	–	
	ΔV_t	Vt+ - Vt-	0.25	–	–	
High-level output voltage (Normal buffer)	V_{OH}	I_{OH} = -100 µA	V_{DDIO} - 0.2	–	–	
		I_{OH} = -2, -4, -6, -8, -10, -12, -14, -16, -24 mA	2.35	–	–	
High-level output voltage (5V Tolerant buffer)		I_{OH} = -100 µA	V_{DDIO} - 0.2	–	–	
		I_{OH} = -2, -4, -6, -8, -10, -12, -14, -16, -24 mA	2.35	–	–	
Low-level output voltage (Normal buffer)	V_{OL}	I_{OL} = 100 µA	–	–	0.2	
		I_{OL} = 2, 4, 6, 8, 10, 12, 14, 16, 24 mA	–	–	0.45	
Low-level output voltage (5V Tolerant buffer)		I_{OL} = 100 µA	–	–	0.2	
		I_{OL} = 2, 4, 6, 8, 10, 12, 14, 16, 24 mA	–	–	0.45	
High-level input current (Normal buffer)	I_{IH}	V_{IH} = V_{DDIO}	–	–	50	µA
		V_{IH} = V_{DDIO} (50kΩ pull-down)	10	–	200	
High-level input current (5V Tolerant buffer)		V_{IH} = V_{DDIO}	–	–	50	
		V_{IH} = 5.5V	–	–	50	
Low-level input current (Normal buffer)	I_{IL}	V_{IL} = V_{SS}	-50	–	–	
		V_{IL} = V_{SS} (50kΩ pull-up)	-200	–	-10	
Low-level input current (5V Tolerant buffer)		V_{IL} = V_{SS}	-50	–	–	
3-state output leakage current (Normal buffer)	I_{OZH}	V_{OH} = V_{DDIO}	–	–	50	
		V_{OH} = V_{DDIO} (50kΩ pull-down)	10	–	200	
	I_{OZL}	V_{OL} = V_{SS}	-50	–	–	
		V_{OL} = V_{SS} (50kΩ pull-up)	-200	–	-10	
3-state output leakage current (5V Tolerant buffer)	I_{OZH}	V_{OH} = V_{DDIO}	–	–	50	
		V_{IH} = 5.5V	–	–	50	
	I_{OZL}	V_{OL} = V_{SS}	-50	–	–	

1. Typical condition is V_{DDCORE} = 1.5V, V_{DDIO} = 3.3V, and T_j = 25°C on a typical process.

AC Characteristics (V_{DDCORE} = 1.5V, V_{DDIO} = 3.3V, V_{SS} = 0 V, T_j = 25°C)

Parameter		Driving Type	Conditions [1] [2]	Rated Value [3]	Unit
Internal gate propagation delay	Inverter	1X	F/O = 2, L = 0 mm	0.038	ns
		2X		0.034	
		4X		0.027	
	2-input NAND	1X		0.047	
		2X		0.038	
		4X		0.033	
	Inverter	1X	F/O = 2, L = standard wire length	0.231	
		2X		0.168	
		4X		0.097	
	2-input NAND	1X		0.280	
		2X		0.155	
		4X		0.093	
Toggle frequency			F/O = 1, L = 0 mm	3530	MHz
Input buffer propagation delay	TTL level normal input buffer		F/O = 2, L = standard wire length	0.391	ns
	TTL 5V Tolerant input buffer			0.708	
Output buffer propagation delay	Push-pull Normal output buffer	4 mA	CL = 20 pF	1.880	
		8 mA	CL = 50 pF	2.072	
		12mA	CL = 100 pF	2.597	
	Tri-state 5V Tolerant buffer	4 mA	CL = 20 pF	2.193	
		8 mA	CL = 50 pF	2.689	
		12 mA	CL = 100 pF	2.820	
Output buffer transition time [4]	Push-pull Normal output buffer	12 mA	CL = 100 pF	3.524 (r)	
				3.526 (f)	
	Tri-state 5V Tolerant buffer	12 mA	CL = 100 pF	3.571 (r)	
				3.466 (f)	

1. Input transition time in 1.5 V/0.1 ns (internal gate), 3.3 V/0.2 ns (input/output buffer).
2. Typical condition is V_{DDCORE} = 1.5 V, V_{DDIO} = 3.3 V, and T_j = 25°C for a typical process.
3. Rated value is calculated as an average of the L-H and H-L delay times of each macro type on a typical process.
4. Output rising and falling times are both specified over a 10% to 90% range.

MACRO LIBRARY

Oki Semiconductor supports a wide range of macrocells ranging from simple hard macrocells for basic boolean operations to large, user-parameterizable macrocells. The following figure illustrates the main classes of macrocells available.

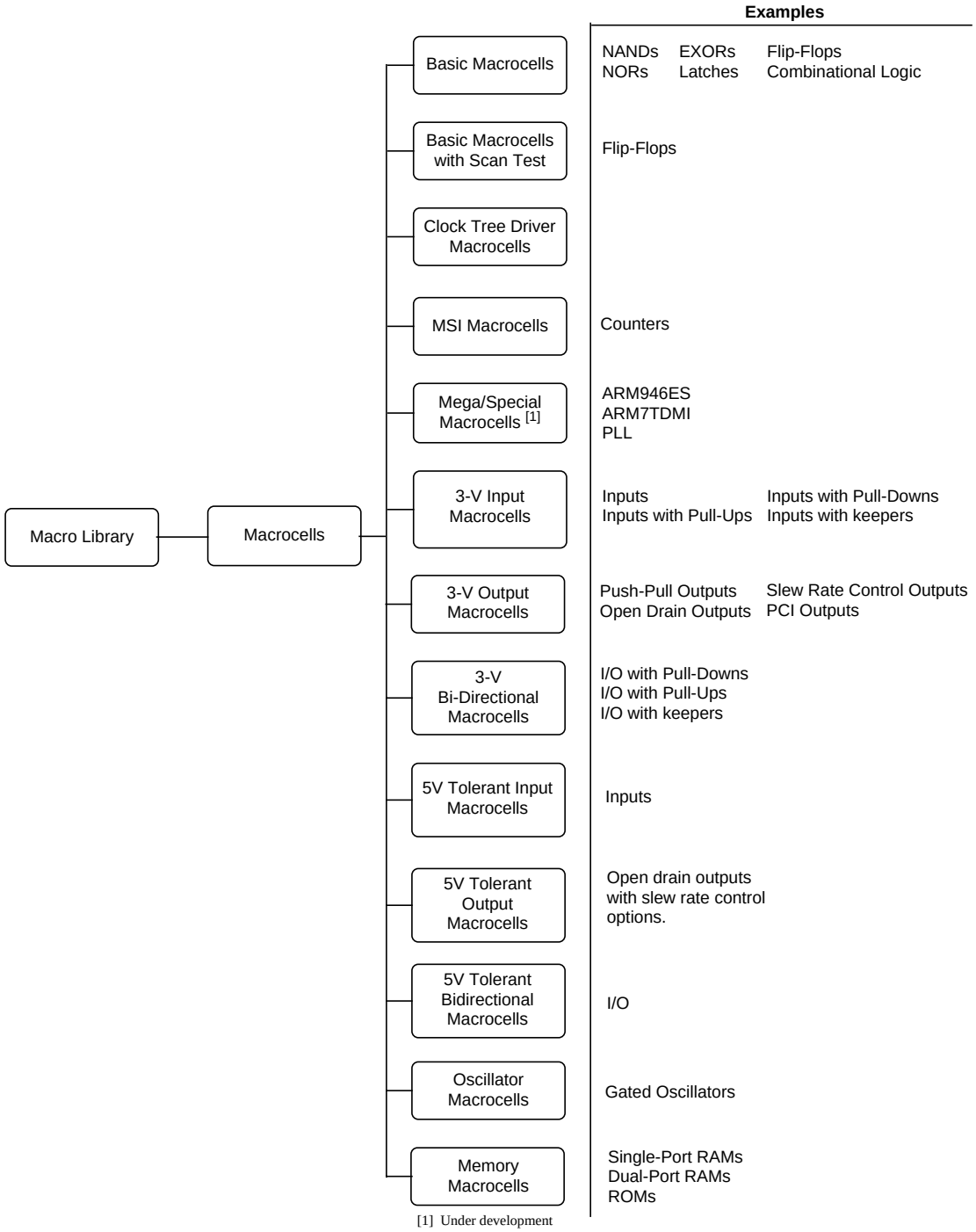


Figure 4. Oki Macrocell Library

Macrocells for Driving Clock Trees

Oki offers the clock tree synthesis (CTPKS) in the Cadence Design Systems, Inc. Physically Knowledgeable Synthesis (PKS) tool. CTPKS constructs buffer trees for any number of specified clocks in a design. CTPKS builds these clock trees one by one, then explores the different tree structures. For each structure, CTPKS places new buffers or inverters and groups the clock leaf pins into clusters so that the pin and wire loads are balanced. PKS timing verification is run on the newly created clock tree, with parasitics extracted from the location of each buffer and inverter. If the performance of the clock tree is better than that of the previous one, the new tree is kept. Otherwise it is rejected.

CTPKS uses the following predefined priority of constraints when selecting the best clock tree topology:

1. Satisfy the maximum load and maximum transition delay constraints.
2. Satisfy the maximum delay constraint.
3. Satisfy the maximum skew constraint.
4. Minimize the size of the clock tree.

After finding the best topology according to the priority list above, CTPKS satisfies the minimum delay constraint by adding appropriate padding buffers.

OKI ADVANCED DESIGN CENTER CAD TOOLS

Oki's advanced design center CAD tools include support for the following:

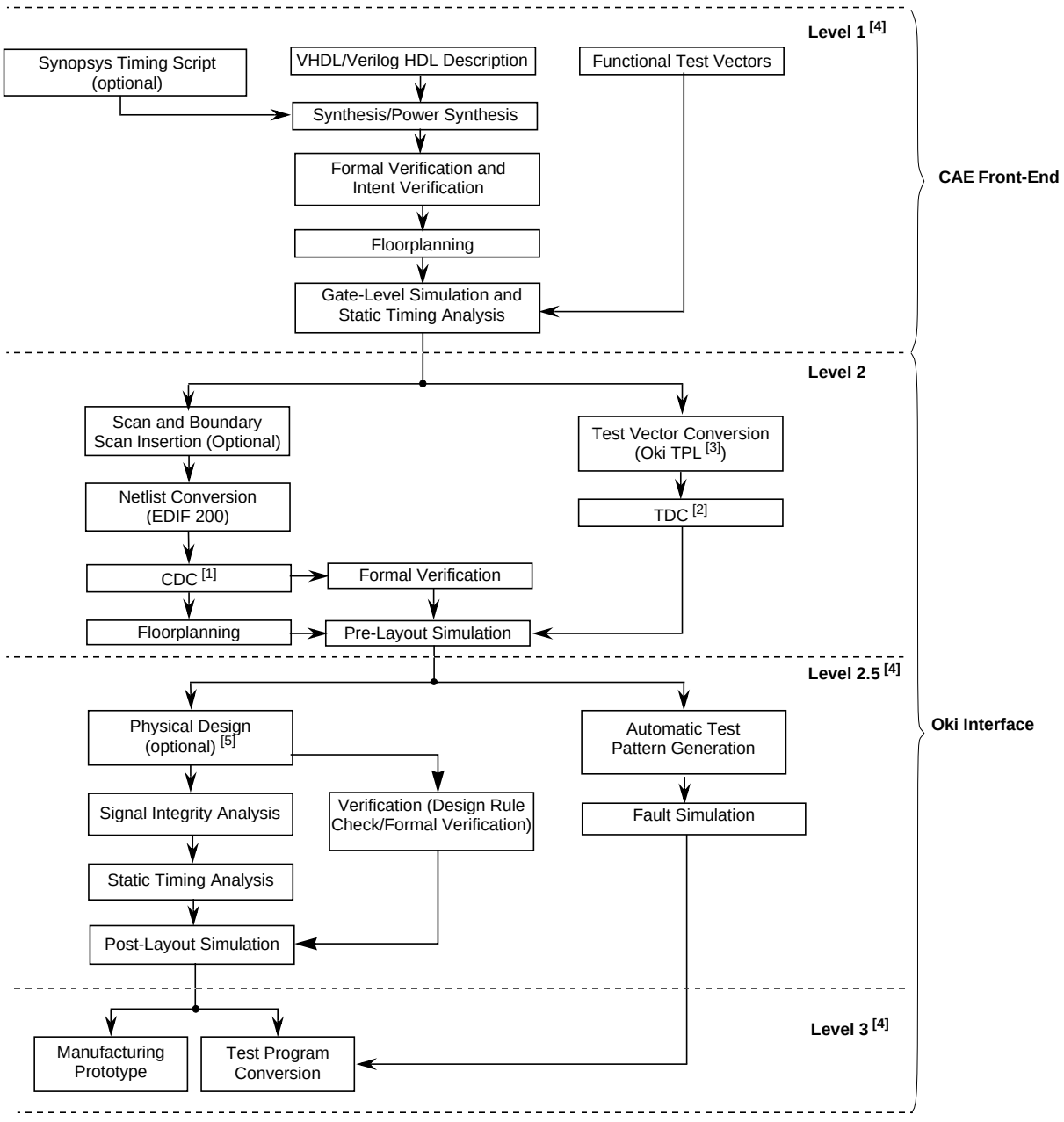
- Floorplanning for front-end simulation and back-end layout control
- Clock tree structures improve first-time silicon success by eliminating clock skew problems
- JTAG Boundary scan support
- Power calculation which predicts circuit power under simulation conditions to accurately model package requirements

Vendor	Platform	Operating System [1]	Vendor Software/Revision [1]	Description
Cadence	Sun® [2]	Solaris 8	Ambit Buildgates NC-Verilog™ Verilog XL NC-VHDL Delay Storm Turbo Fault	Design Synthesis Design Simulation Design Simulation Design Simulation Timing Calculation Fault Grading
Synopsys	Sun® [2]	Solaris 8	Design Compiler Ultra + Tetramax/ATPG Primetime DFT Compiler/Test Compiler RTL Analyzer BSD Complier VCS	Design synthesis Test Synthesis Static Timing Analysis (STA) Test synthesis HDL Source Code Identification JTAG Insertion Design Simulation
Model Technology Inc. (MTI)	Sun® [2] NT	Solaris 8 WinNT4.0	MTI-VHDL MTI-Verilog	VHDL Simulation Verilog Simulation
Xemplar	Sun® [2] NT	Solaris 8 WinNT4.0	Leonardo Spectrum	Design Synthesis
Oki	Sun® [2]	Solaris 8	Floorplanner Hier Floorplanner	Design Floorplanning Design Floorplanning
Verplex	Sun® [2]	Solaris 8	Conformal LEC	Formal Verification

1. Contact Oki Application Engineering for current software versions.
2. Sun or Sun-compatible.

DESIGN PROCESS

The following figure illustrates the overall IC design process, also indicating the three main interface points between external design houses and Oki ASIC Application Engineering.



[1] Oki's Circuit Data Check program (CDC) verifies logic design rules
[2] Oki's Test Data Check program (TDC) verifies test vector rules
[3] Oki's Test Pattern Language (TPL)
[4] Alternate Customer-Oki design interfaces available in addition to standard level 2
[5] Requires Synopsys timing script for Oki timing driven layout

Figure 5. Oki's Design Process

Automatic Test Pattern Generation

Oki's 0.15µm ASIC technologies support ATPG using full scan-path design techniques, including the following:

- High fault coverage
- Uses Synopsys DFT Compiler and Tetramax
- Automatically inserts scan structures
- Connects scan chains
- Traces and reports scan chains
- Checks for rule violations
- Generates complete fault reports
- Allows multiple scan chains
- Supports test point insertion and vector compaction

ATPG methodology is described in detail in Oki's *Scan Path Application Note*.

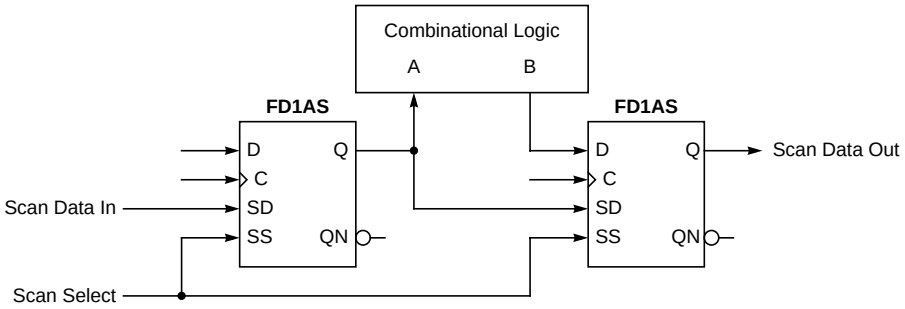


Figure 6. Full Scan Path Configuration

Floorplanning Design Flow

Oki offers the floorplanning tool (OKI FP) for high-density ASIC design. The three main purposes for Oki's floorplanning tool is to:

- Ensure conformance of critical circuit performance specifications
- Shorten overall design TAT
- Hierarchical Layout

In a traditional design approach with synthesis tools there is no physical cluster information provided in the synthesis tool, and so it is difficult to synthesize logic using predicted interconnection delay due to wire length. Synthesis tools may therefore create an over-optimized or under-optimized result.

Floorplanning allows designers to estimate and control parasitic capacitance in a circuit by participating in the physical design process. Designers can partition their ASIC circuit in the most efficient hierarchical manner, and/or specify the exact placement of critical timing paths to guarantee high-speed performance.

Floorplanning also allows the reduction of layout iterations, minimizing a design's overall TAT. As parasitic capacitance dominates a circuit's timing in sub-micron technologies, an accurate capacitance estimation is crucial for accurate pre-layout timing simulation. Quite often, designers have to iterate the circuit layout because unexpected post-layout capacitance causes unacceptable circuit performance.

More information on OKI's floorplanning capabilities is available in Oki's Application Note, *Using Oki's Floorplanner: Standalone Operation and Links to Synopsys.*

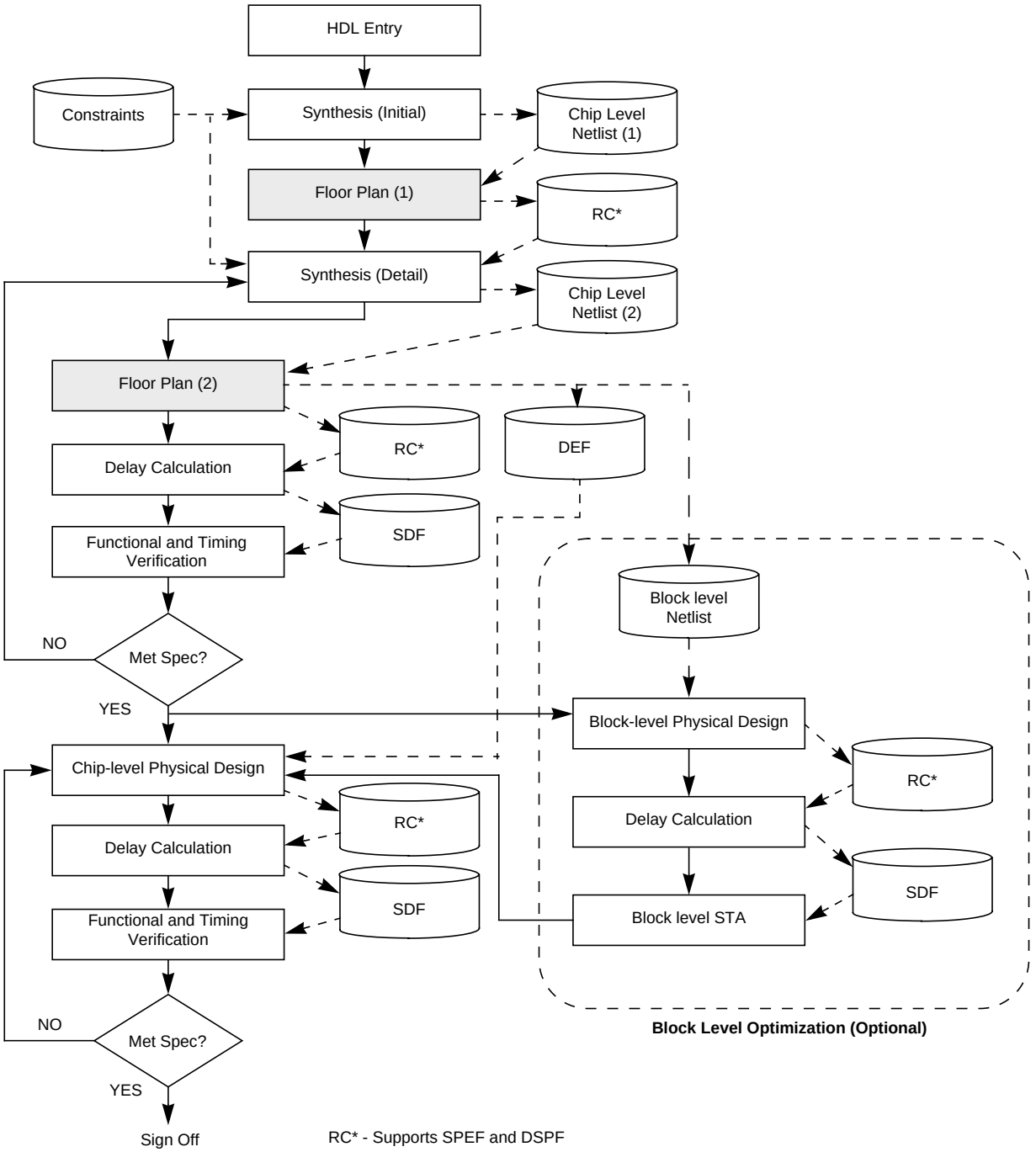


Figure 7. Design Flow

IEEE JTAG Boundary Scan Support

Boundary scan offers efficient board-level and chip-level testing capabilities. Benefits resulting from incorporating boundary-scan logic into a design include:

- Improved chip-level and board-level testing and failure diagnostic capabilities
- Support for testing of components with limited probe access
- Easy-to-maintain testability and system self-test capability with on-board software
- Capability to fully isolate and test components on the scan path
- Built-in test logic that can be activated and monitored
- An optional Boundary Scan Identification (ID) Register

Oki's boundary scan methodology meets the JTAG Boundary Scan standard, IEEE 1149.1-1990. Oki supports boundary scan on Customer Structured Array (CSA) ASIC technologies. Either the customer or Oki can perform boundary-scan insertion. More information is available in Oki's *JTAG Boundary Scan Application Note.* (Contact the Oki Application Engineering Department for interface options.)

PACKAGE OPTIONS

TQFP, LQFP, and QFP Package Menu

		TQFP					LQFP			QFP					
Product Name	**I/O Pads [1]**	**44**	**64**	**80**	**100**	**128**	**144**	**176**	**208**	**44**	**64**	**80**	**100**	**208**	**240**
MG7xKB02	68	#													
MG7xKB04	108	#			●						●	#			
MG7xKB06	148	●		●	●	●					●	#	#		
MG7xKB08	188	●	●	●	●	●				#	●	#	#		
MG7xKB10	228	●	●	●	●	●	●	●	●	#	●	#		●	
MG7xKB12	268	●	●	●	●	●	●	●	●	#	●	#	#	●	
MG7xKB14	308		●	●	●	●	●	●	●	#	●	#	#	●	
MG7xKB16	348		#	●	●		●	●	●		●	#	#	●	
MG7xKB18	388			●	●		●	●	●		●	#	#	●	#
MG7xKB20	428			●	●		●	●	●		●	#	#	●	●
MG7xKB22	468			●	●		●	●	●		●	#	#	●	
MG7xKB24	508				●		●	●	●		●	#	#	●	
MG7xKB26	548				●		●	●	●		●		#	●	●
MG7xKB28	588						●	●	●					●	●
MG7xKB30	628						●	●	●					●	
MG7xKB32	668						●	●	●					●	#
MG7xKB34	708						●	●	●						●
MG7xKB36	748						●	●	●						
MG7xKB38	788								●						
MG7xKB40	828								●						
MG7xKB42	868								●						
Body Size (mm)		10 x 10	10 x 10	12 x 12	14 x 14	14 x 14	20 x 20	24 x 24	28 x 28	9 x 10	14 x 14	14 x 20	14 x 20	28 x 28	32 x 32
Lead Pitch (mm)		0.80	0.50	0.50	0.50	0.40	0.50	0.50	0.50	0.80	0.80	0.80	0.65	0.50	0.50

1. I/O Pads can be used for input, output, bi-directional, power, or ground.

● = Available

= Planning

TFLGA, LFBGA, and PBGA Package Menu

Product Name	I/O Pads [1]	TFLGA			LFBGA				PBGA				
		48	56	84	48	84	144	224	256	352	420	676	896
MG7xKB02	68	●		●	●	●							
MG7xKB04	108	●		●	●	●							
MG7xKB06	148	●		●	●	●							
MG7xKB08	188	●		●	●	●							
MG7xKB10	228		#	●	●	●							
MG7xKB12	268		#	●		●	●						
MG7xKB14	308			●		●	●		●				
MG7xKB16	348						●	●	●	●			
MG7xKB18	388						●	●	●	●	●		
MG7xKB20	428						●	●	●	●	●		
MG7xKB22	468						●	#	●	●	●		
MG7xKB24	508							●	●	●	●		
MG7xKB26	548								●	●	●		
MG7xKB28	588								●	●	●	#	
MG7xKB30	628								●	●	●	#	
MG7xKB32	668								●	●	●	#	
MG7xKB34	708									●	●		
MG7xKB36	748									●			
MG7xKB38	788									●			#
MG7xKB40	828									●			#
MG7xKB42	868									●			#
Body Size (mm)		7x7	8x8	9x9	7x7	9x9	11x11	15x15	27x27	35x35	35x35	27x27	31x31
Ball Pitch (mm)		0.80	0.80	0.80	0.80	0.80	0.80	0.80	1.27	1.27	1.27	1.00	1.00
Ball Count		48	56	84	48	84	144	224	256	352	420	676	896
Signal I/O [2]		48	56	84	48	84	144	224	231	304	352	540	700
Power Balls		0	0	0	0	0	0	0	12	16	32	48	68
GND Balls		0	0	0	0	0	0	0	13	32	36	88	128

1. I/O pads can be used for input, output, bi-directional, power, or ground.
2. Signal I/O can be used for input, output, bi-directional, power, or ground.

● = Available now

= Planning

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