

May 2000

Preliminary Information

1.0 Features

- Develops all the high-speed clocks required for LAN Hub applications
- Clock skew on CLKB1:4 clocks < 250ps
- Period jitter: 150ps pk-pk typical
- Available in 20-pin SSOP and TSSOP packages

Figure 2: Pin Configuration

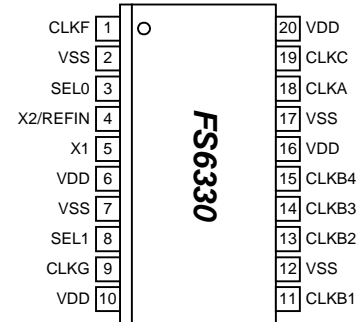


Figure 1: Block Diagram

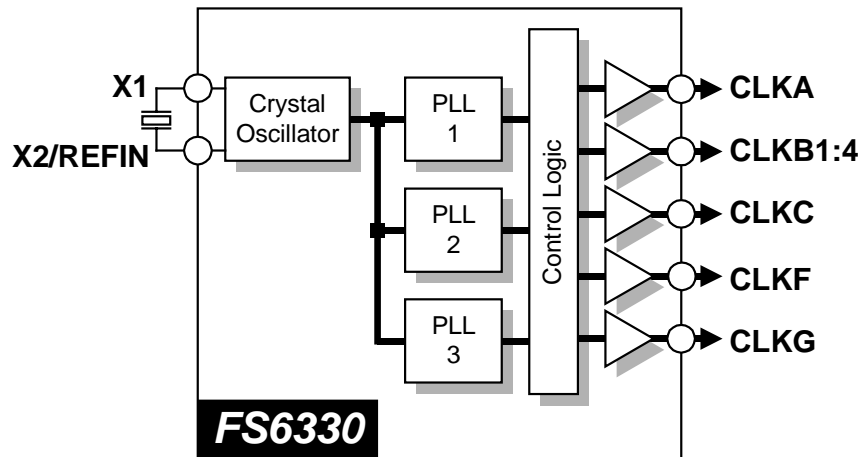


Table 1: Frequency Table

FONT	CRYSTAL	SEL1	SELO	CLKA	CLKB[1:4]	CLKC	CLKF	CLKG
FS6330-01	25MHz	0	0	25.000MHz	50.000MHz	66.667MHz	100.000MHz	125.000MHz
		0	1	25.000MHz	50.000MHz	75.000MHz	125.000MHz	125.000MHz
		1	0	25.000MHz	50.000MHz	83.333MHz	125.000MHz	125.000MHz
		1	1	25.000MHz	50.000MHz	100.000MHz	100.000MHz	125.000MHz

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Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI^D = Input with Internal Pull-Down; DO = Digital Output; P = Power/Ground; # = Active-low pin

PIN	TYPE	NAME	DESCRIPTION
1	DO	CLKF	Clock Output
2, 7, 12, 17	P	VSS	Ground
3	DI ^U	SEL0	Clock Select (LSB)
4	AO	X2/REFIN	Crystal oscillator drive / external reference input
5	AI	X1	Crystal oscillator feedback
6, 10, 16, 20	P	VDD	+3.3V power supply
8	DI ^U	SEL1	Clock Select (MSB)
9	DO	CLKG	Clock Output
11, 13, 14, 15	DO	CLKB1:4	Four clock outputs
18	DO	CLKA	Clock Output
19	DO	CLKC	Clock Output

2.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	$V_{SS}-0.5$	7	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Input Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{IK}	-50	50	mA
Output Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV



CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		3.135	3.3	3.465	V
Operating Temperature Range	T_A	No airflow	0		70	°C

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Table 5: DC Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V ± 5%, no load on any output, and ambient temperature $T_A = 0^\circ\text{C}$ to 70°C . Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	All 3.3V supplies = 3.465V				mA
X1 Crystal Oscillator Feedback						
Threshold Bias Voltage	V_{TH}			$0.5V_{DD}$		V
High-Level Input Current	I_{IH}	$V_{IH} = 3.3V$		32		μA
Low-Level Input Current	I_{IL}	$V_{IL} = 0V$		-32		μA
Crystal Loading Capacitance *	$C_{L(xtal)}$	As seen by an external crystal connected to XIN and XOUT	13.5	18	22.5	pF
Input Loading Capacitance *	$C_{L(XIN)}$	As seen by an external clock driver on XOUT; XIN unconnected		36		pF
X2 Crystal Oscillator Drive						
High Level Output Source Current	I_{OH}	$V_I = 3.3V, V_O = 0V$		-8		mA
Low Level Output Sink Current	I_{OL}	$V_I = 0V, V_O = 3.3V$		9		mA
Clock Outputs						
High-Level Output Source Current	I_{OH}	$V_O = 2.4V$				mA
Low-Level Output Sink Current	I_{OL}	$V_O = 0.4V$				mA
Output Impedance	Z_O	Measured at 1.5V				Ω
Short Circuit Output Source Current	I_{OSH}	$V_O = 0V$; shorted for 30s, max.				mA
Short Circuit Output Sink Current	I_{OSL}	$V_O = 3.3V$; shorted for 30s, max.				mA

Table 6: AC Timing Specifications

Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature $T_A = 25^\circ\text{C}$. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Clock Outputs						
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45		55	%
Clock Skew *	$t_{sk(o)}$	CLKB1 to CLKB4 at 1.5V			250	ps
Jitter, Long Term ($\sigma_j(\tau)$) *	$t_{j(LT)}$	On rising edges 500 μs apart at 1.5V relative to an ideal clock, $C_L=15\text{pF}$, all PLLs active				ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.5V, $C_L=15\text{pF}$, all PLLs active			150	ps
Rise Time *	t_r	Measured @ 0.4V – 2.4V; $C_L=15\text{pF}$		1.2		ns
Fall Time *	t_f	Measured @ 2.4V – 0.4V; $C_L=15\text{pF}$		1.2		ns

3.0 Package Information

Table 7: 20-pin SSOP (5.3mm) Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	-	0.079	-	2.0
A ₁	0.002	-	0.05	-
A ₂	0.065	0.073	1.65	1.85
b	0.009		0.22	0.38
c	0.0004	0.0098	0.09	0.25
D	0.272	0.295	6.90	7.50
E	0.291	0.323	7.40	8.20
E ₁	0.197	0.220	5.00	5.60
e	0.0255 BSC		0.65 BSC	
L	0.022	0.037	0.55	0.95
θ	0°	8°	0°	8°

Table 8: 20-pin SSOP (5.3mm) Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	110	°C/W
Lead Inductance, Self	L ₁₁	Longest trace	2.260	nH
		Shortest trace	0.958	
Lead Inductance, Mutual	L ₁₂	Longest trace to first adjacent trace	0.848	nH
		Shortest trace to first adjacent trace	0.408	
Lead Capacitance, Bulk	C ₁₁	Longest trace to V _{SS}	0.395	pF
		Shortest trace to V _{SS}	0.209	
Lead Capacitance, Mutual	C ₁₂	Longest trace to first adjacent trace	0.163	pF
		Shortest trace to first adjacent trace	0.057	

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Table 9: 20-pin TSSOP (4.4mm) Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	-	0.047	-	1.2
A ₁	0.002	0.006	0.05	0.15
A ₂	0.031	0.041	0.80	1.05
b	0.007	0.012	0.19	0.30
c	0.0035	0.0078	0.09	0.20
D	0.252	0.260	6.40	6.60
E	0.252 BSC		6.40 BSC	
E ₁	0.169	0.177	4.30	4.50
e	0.0255 BSC		0.65 BSC	
L	0.022	0.037	0.45	0.75
S	0.0078	-	0.20	-
θ ₁	0°	8°	0°	8°
θ ₂	12° REF		12° REF	
θ ₃	12° REF		12° REF	

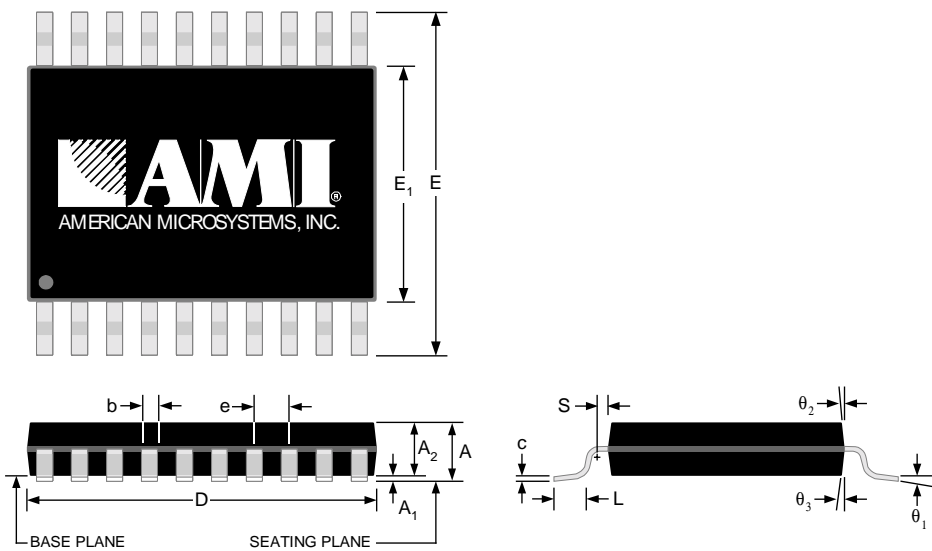


Table 10: 20-pin SSOP (4.4mm) Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	θ _{JA}	Air flow = 0 m/s	95	°C/W
Lead Inductance, Self	L ₁₁	Longest trace	1.680	nH
		Shortest trace	0.701	
Lead Inductance, Mutual	L ₁₂	Longest trace to first adjacent trace	0.606	nH
		Shortest trace to first adjacent trace	0.248	
Lead Capacitance, Bulk	C ₁₁	Longest trace to V _{SS}	0.306	pF
		Shortest trace to V _{SS}	0.184	
Lead Capacitance, Mutual	C ₁₂	Longest trace to first adjacent trace	0.110	pF
		Shortest trace to first adjacent trace	0.043	

FS6330

LAN Hub Clock Generator IC



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4.0 Ordering Information

4.1 Device Ordering Codes

DEVICE NUMBER	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS6330-01	11825-807	20-pin SSOP	0° C to 70° C (Commercial)	Tape and Reel
		20-pin TSSOP	0° C to 70° C (Commercial)	Tape and Reel

5.0 Revision Information

DATE	PAGE	DESCRIPTION
March 17, 2000		Modified device pinout to add SELECT inputs for CLKC and CLKF
March 27, 2000	1,2	Changed CLKA and CLKF pin locations. Changed frequency table for CLKF
May 23, 2000		Upgraded data sheet to Preliminary Information, added SSOP Ordering Code

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