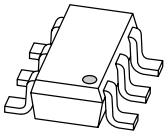


PVR100AD-B series

Voltage regulator series

Rev. 01 — 31 October 2006 **Product data sheet**

1. Product profile

1.1 General description

Integrated Zener diode and NPN bipolar transistor in one package.

Table 1. Product overview

Type number	Package		SOT223 complement
	NXP	JEITA	
PVR100AD-B2V5	SOT457	SC-74	PVR100AZ-B2V5
PVR100AD-B3V0			PVR100AZ-B3V0
PVR100AD-B3V3			PVR100AZ-B3V3
PVR100AD-B5V0			PVR100AZ-B5V0
PVR100AD-B12V			PVR100AZ-B12V

1.2 Features

- Integrated Zener diode and bipolar transistor
- Output voltage options: 2.5 V, 3 V, 3.3 V, 5 V and 12 V
- Output power dissipation capability: 380 mW
- Small Surface-Mounted Device (SMD) plastic package

1.3 Applications

- Linear voltage regulation

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NPN transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	45	V
I_C	collector current		-	-	0.1	A
h_{FE}	DC current gain	V_{CE} = 1 V; I_C = 100 mA	160	-	400	

Table 2. Quick reference data *...continued*

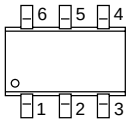
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Zener diode							
V_Z	working voltage	I_Z = 5 mA					
	PVR100AD-B2V5			3.23	3.3	3.37	V
	PVR100AD-B3V0			3.53	3.6	3.67	V
	PVR100AD-B3V3			3.82	3.9	3.98	V
	PVR100AD-B5V0			5.49	5.6	5.71	V
	PVR100AD-B12V			12.7	13	13.3	V
Voltage regulator							
V_O	output voltage	I_O = 10 mA	[1]				
	PVR100AD-B2V5	V_I = 4.5 V; I_{ctrl} = 3.5 mA		2.25	2.5	2.75	V
	PVR100AD-B3V0	V_I = 5 V; I_{ctrl} = 6.5 mA		2.7	3	3.3	V
	PVR100AD-B3V3	V_I = 5.3 V; I_{ctrl} = 6.5 mA		3.07	3.3	3.53	V
	PVR100AD-B5V0	V_I = 7 V; I_{ctrl} = 10 mA		4.65	5	5.35	V
	PVR100AD-B12V	V_I = 14 V; I_{ctrl} = 5 mA		11.4	12.3	13.2	V
Line regulation							
$\Delta V_O/V_O$	relative output voltage variation	I_O = 10 mA	[1]				
	PVR100AD-B2V5	4.5 V ≤ V_I ≤ 40 V; I_{ctrl} = 3.5 mA		–10	-	+10	%
	PVR100AD-B3V0	5 V ≤ V_I ≤ 40 V; I_{ctrl} = 6.5 mA		–10	-	+10	%
	PVR100AD-B3V3	5.3 V ≤ V_I ≤ 40 V; I_{ctrl} = 6.5 mA		–7	-	+7	%
	PVR100AD-B5V0	7 V ≤ V_I ≤ 40 V; I_{ctrl} = 10 mA		–7	-	+7	%
	PVR100AD-B12V	14 V ≤ V_I ≤ 40 V; I_{ctrl} = 5 mA		–7	-	+7	%
Load regulation							
$\Delta V_O/V_O$	relative output voltage variation	5 mA ≤ I_O ≤ 100 mA	[1]				
	PVR100AD-B2V5	V_I = 4.5 V; I_{ctrl} = 3.5 mA		–10	-	+10	%
	PVR100AD-B3V0	V_I = 5 V; I_{ctrl} = 6.5 mA		–10	-	+10	%
	PVR100AD-B3V3	V_I = 5.3 V; I_{ctrl} = 6.5 mA		–7	-	+7	%
	PVR100AD-B5V0	V_I = 7 V; I_{ctrl} = 10 mA		–7	-	+7	%
	PVR100AD-B12V	V_I = 14 V; I_{ctrl} = 5 mA		–7	-	+7	%

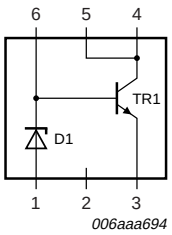
[1] Pulse test: $t_p \leq 300\ \mu s$; $\delta \leq 0.02$.

2. Pinning information

Table 3. Pinning

Pin	Symbol	Description	Simplified outline	Symbol
1	GND	ground		
2	n.c.	not connected		
3	VO	output voltage		
4	VI	input voltage		
5	VI	input voltage		
6	REXT	base		





3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PVR100AD-B2V5	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457
PVR100AD-B3V0			
PVR100AD-B3V3			
PVR100AD-B5V0			
PVR100AD-B12V			

4. Marking

Table 5. Marking codes

Type number	Marking code
PVR100AD-B2V5	T1
PVR100AD-B3V0	T2
PVR100AD-B3V3	T3
PVR100AD-B5V0	T4
PVR100AD-B12V	T5

5. Limiting values

Table 6. Limiting values

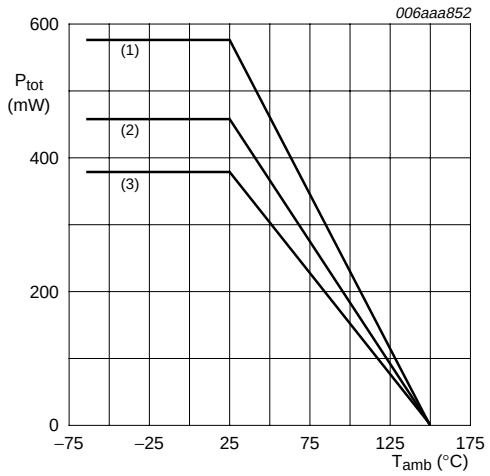
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
NPN transistor						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	45	V
V_{EBO}	emitter-base voltage	open collector		-	5	V
I_C	collector current			-	0.1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	0.2	A
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms		-	0.2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	300	mW
			[2]	-	380	mW
			[3]	-	480	mW
Zener diode						
I_F	forward current			-	200	mA
I_{ZSM}	non-repetitive peak reverse current	$V_Z < 6$ V		-	6	A
		$V_Z = 13$ V		-	2.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	140	mW
Voltage regulator						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	380	mW
			[2]	-	460	mW
			[3]	-	580	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.



(1) Ceramic PCB, Al_2O_3, standard footprint

(2) FR4 PCB, mounting pad for collector 1 cm^2

(3) FR4 PCB, standard footprint

Fig 1. Power derating curves

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
NPN transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W
			[2]	-	-	329	K/W
			[3]	-	-	260	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	125	K/W
Zener diode							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	893	K/W
Voltage regulator							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	329	K/W
			[2]	-	-	272	K/W
			[3]	-	-	216	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.

7. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NPN transistor						
I_{CBO}	collector-base cut-off current	V_{CB} = 20 V; I_E = 0 A	-	-	100	nA
		V_{CB} = 20 V; I_E = 0 A; T_j = 150 °C	-	-	5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A	-	-	100	nA
h_{FE}	DC current gain	V_{CE} = 1 V; I_C = 100 mA	160	-	400	
V_{BE}	base-emitter voltage	V_{CE} = 1 V; I_C = 10 mA	-	0.72	-	V
Zener diode						
V_F	forward voltage	I_F = 10 mA	-	-	0.9	V
I_R	reverse current					
	PVR100AD-B2V5	V_R = 1 V	-	-	5	µA
	PVR100AD-B3V0	V_R = 1 V	-	-	5	µA
	PVR100AD-B3V3	V_R = 1 V	-	-	3	µA
	PVR100AD-B5V0	V_R = 2 V	-	-	1	µA
	PVR100AD-B12V	V_R = 8 V	-	-	0.1	µA
V_Z	working voltage	I_Z = 5 mA				
	PVR100AD-B2V5		3.23	3.3	3.37	V
	PVR100AD-B3V0		3.53	3.6	3.67	V
	PVR100AD-B3V3		3.82	3.9	3.98	V
	PVR100AD-B5V0		5.49	5.6	5.71	V
	PVR100AD-B12V		12.7	13	13.3	V
r_{dif}	differential resistance	I_Z = 1 mA				
	PVR100AD-B2V5		-	350	600	Ω
	PVR100AD-B3V0		-	375	600	Ω
	PVR100AD-B3V3		-	400	600	Ω
	PVR100AD-B5V0		-	80	400	Ω
	PVR100AD-B12V		-	50	170	Ω
r_{dif}	differential resistance	I_Z = 5 mA				
	PVR100AD-B2V5		-	85	95	Ω
	PVR100AD-B3V0		-	85	90	Ω
	PVR100AD-B3V3		-	85	90	Ω
	PVR100AD-B5V0		-	15	40	Ω
	PVR100AD-B12V		-	10	30	Ω

Table 8. Characteristics *...continued*

T_{amb} = 25 °C unless otherwise specified.

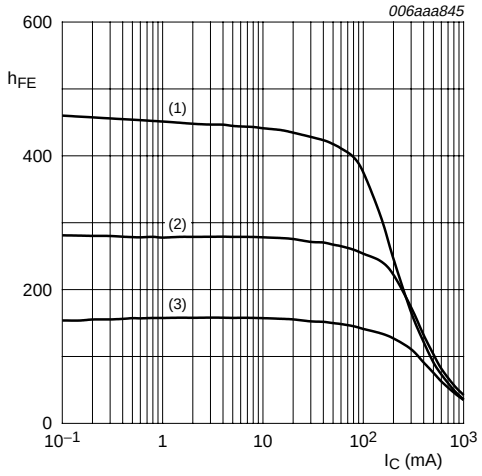
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
S_Z	temperature coefficient	I_Z = 5 mA					
	PVR100AD-B2V5			–3.5	–2.4	0	mV/K
	PVR100AD-B3V0			–3.5	–2.4	0	mV/K
	PVR100AD-B3V3			–3.5	–2.5	0	mV/K
	PVR100AD-B5V0			–2	1.2	2.5	mV/K
	PVR100AD-B12V			7	9.4	11	mV/K
Voltage regulator							
V_O	output voltage	I_O = 10 mA	[1]				
	PVR100AD-B2V5	V_I = 4.5 V; I_{ctrl} = 3.5 mA		2.25	2.5	2.75	V
	PVR100AD-B3V0	V_I = 5 V; I_{ctrl} = 6.5 mA		2.7	3	3.3	V
	PVR100AD-B3V3	V_I = 5.3 V; I_{ctrl} = 6.5 mA		3.07	3.3	3.53	V
	PVR100AD-B5V0	V_I = 7 V; I_{ctrl} = 10 mA		4.65	5	5.35	V
	PVR100AD-B12V	V_I = 14 V; I_{ctrl} = 5 mA		11.4	12.3	13.2	V
$\Delta V_O/(V_O \times \Delta T_{amb})$	relative output voltage variation over ambient temperature	I_O = 100 mA; T_{amb} = –55 °C to 150 °C	[1]				
	PVR100AD-B2V5	V_I = 4.5 V		-	38	-	10^{-6}/K
	PVR100AD-B3V0	V_I = 5 V		-	–78	-	10^{-6}/K
	PVR100AD-B3V3	V_I = 5.3 V		-	–61	-	10^{-6}/K
	PVR100AD-B5V0	V_I = 7 V		-	634	-	10^{-6}/K
	PVR100AD-B12V	V_I = 14 V		-	892	-	10^{-6}/K
Line regulation							
$\Delta V_O/V_O$	relative output voltage variation	I_O = 10 mA	[1]				
	PVR100AD-B2V5	4.5 V ≤ V_I ≤ 40 V; I_{ctrl} = 3.5 mA		–10	-	+10	%
	PVR100AD-B3V0	5 V ≤ V_I ≤ 40 V; I_{ctrl} = 6.5 mA		–10	-	+10	%
	PVR100AD-B3V3	5.3 V ≤ V_I ≤ 40 V; I_{ctrl} = 6.5 mA		–7	-	+7	%
	PVR100AD-B5V0	7 V ≤ V_I ≤ 40 V; I_{ctrl} = 10 mA		–7	-	+7	%
	PVR100AD-B12V	14 V ≤ V_I ≤ 40 V; I_{ctrl} = 5 mA		–7	-	+7	%

Table 8. Characteristics *...continued*

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta V_O/(V_O \times \Delta V_I)$	relative output voltage variation over input voltage	I_O = 10 mA	[1]				
	PVR100AD-B2V5	4.5 V ≤ V_I ≤ 40 V; I_{ctrl} = 3.5 mA		-	100	-	10^{-6}/V
	PVR100AD-B3V0	5 V ≤ V_I ≤ 40 V; I_{ctrl} = 6.5 mA		-	80	-	10^{-6}/V
	PVR100AD-B3V3	5.3 V ≤ V_I ≤ 40 V; I_{ctrl} = 6.5 mA		-	70	-	10^{-6}/V
	PVR100AD-B5V0	7 V ≤ V_I ≤ 40 V; I_{ctrl} = 10 mA		-	40	-	10^{-6}/V
	PVR100AD-B12V	14 V ≤ V_I ≤ 40 V; I_{ctrl} = 5 mA		-	20	-	10^{-6}/V
Load regulation							
$\Delta V_O/V_O$	relative output voltage variation	5 mA ≤ I_O ≤ 100 mA	[1]				
	PVR100AD-B2V5	V_I = 4.5 V; I_{ctrl} = 3.5 mA		–10	-	+10	%
	PVR100AD-B3V0	V_I = 5 V; I_{ctrl} = 6.5 mA		–10	-	+10	%
	PVR100AD-B3V3	V_I = 5.3 V; I_{ctrl} = 6.5 mA		–7	-	+7	%
	PVR100AD-B5V0	V_I = 7 V; I_{ctrl} = 10 mA		–7	-	+7	%
	PVR100AD-B12V	V_I = 14 V; I_{ctrl} = 5 mA		–7	-	+7	%
$\Delta V_O/(V_O \times \Delta I_O)$	relative output voltage variation over output current	5 mA ≤ I_O ≤ 100 mA	[1]				
	PVR100AD-B2V5	V_I = 4.5 V; I_{ctrl} = 3.5 mA		-	–840	-	10^{-6}/mA
	PVR100AD-B3V0	V_I = 5 V; I_{ctrl} = 6.5 mA		-	–630	-	10^{-6}/mA
	PVR100AD-B3V3	V_I = 5.3 V; I_{ctrl} = 6.5 mA		-	–540	-	10^{-6}/mA
	PVR100AD-B5V0	V_I = 7 V; I_{ctrl} = 10 mA		-	–320	-	10^{-6}/mA
	PVR100AD-B12V	V_I = 14 V; I_{ctrl} = 5 mA		-	–130	-	10^{-6}/mA

[1] Pulse test: $t_p \leq 300\ \mu s$; $\delta \leq 0.02$.



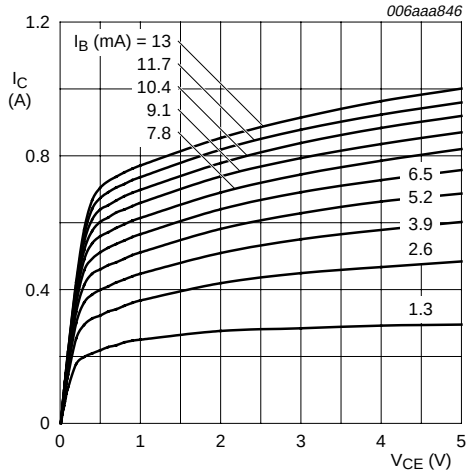
V_{CE} = 1 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

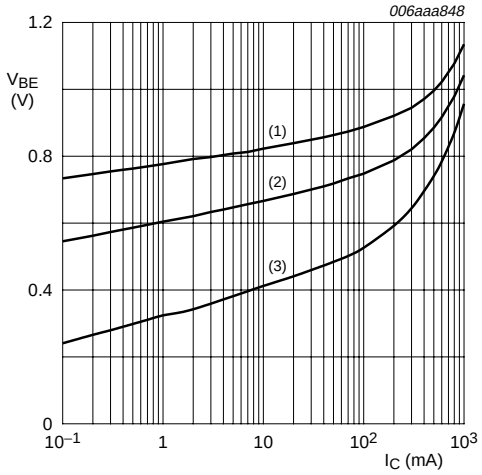
(3) T_{amb} = –55 °C

Fig 2. NPN transistor: DC current gain as a function of collector current; typical values



T_{amb} = 25 °C

Fig 3. NPN transistor: Collector current as a function of collector-emitter voltage; typical values



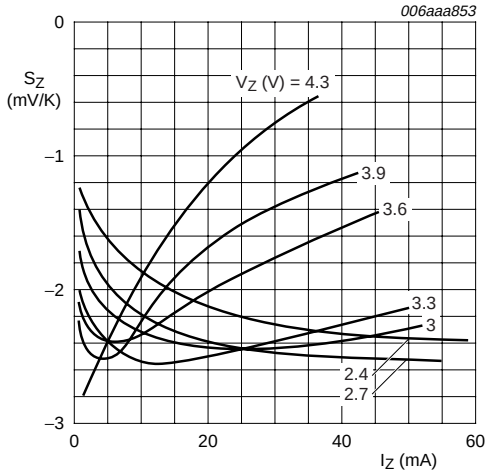
V_{CE} = 1 V

(1) T_{amb} = –55 °C

(2) T_{amb} = 25 °C

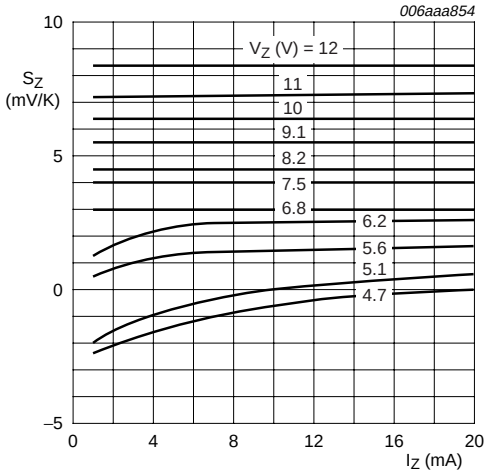
(3) T_{amb} = 150 °C

Fig 4. NPN transistor: Base-emitter voltage as a function of collector current; typical values



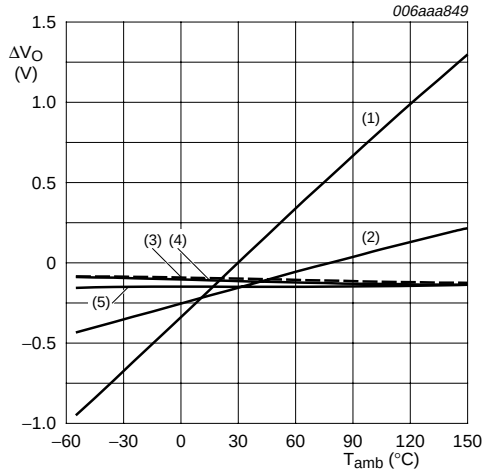
T_j = 25 °C to 150 °C

Fig 5. Zener diode: Temperature coefficient as a function of working current; typical values



T_j = 25 °C to 150 °C

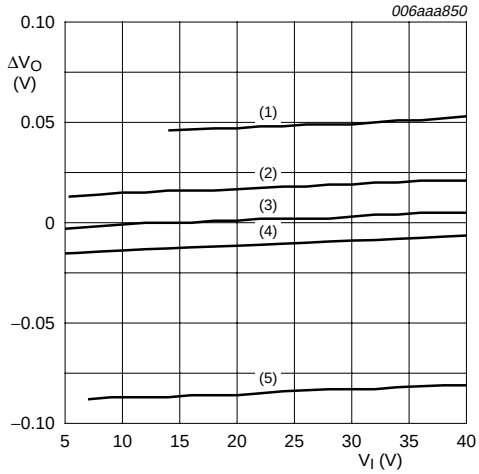
Fig 6. Zener diode: Temperature coefficient as a function of working current; typical values



$V_I = V_{O(typ)} + 2$ V; $I_O = 100$ mA;
$T_{amb} = -55$ °C to 150 °C

(1) PVR100AD-B12V
(2) PVR100AD-B5V0
(3) PVR100AD-B3V3
(4) PVR100AD-B3V0
(5) PVR100AD-B2V5

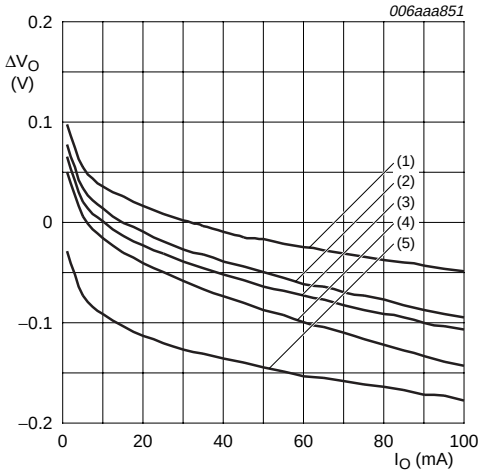
Fig 7. Voltage regulator: Output voltage variation as a function of ambient temperature; typical values



$T_{amb} = 25$ °C; $I_O = 10$ mA

(1) PVR100AD-B12V; $I_{ctrl} = 5$ mA
(2) PVR100AD-B3V3; $I_{ctrl} = 6.5$ mA
(3) PVR100AD-B3V0; $I_{ctrl} = 6.5$ mA
(4) PVR100AD-B2V5; $I_{ctrl} = 3.5$ mA
(5) PVR100AD-B5V0; $I_{ctrl} = 10$ mA

Fig 8. Voltage regulator: Output voltage variation as a function of input voltage; typical values



$T_{amb} = 25$ °C; $V_I = V_{O(typ)} + 2$ V

(1) PVR100AD-B12V; $I_{ctrl} = 5$ mA
(2) PVR100AD-B3V3; $I_{ctrl} = 6.5$ mA
(3) PVR100AD-B3V0; $I_{ctrl} = 6.5$ mA
(4) PVR100AD-B2V5; $I_{ctrl} = 3.5$ mA
(5) PVR100AD-B5V0; $I_{ctrl} = 10$ mA

Fig 9. Voltage regulator: Output voltage variation as a function of output current; typical values

8. Test information

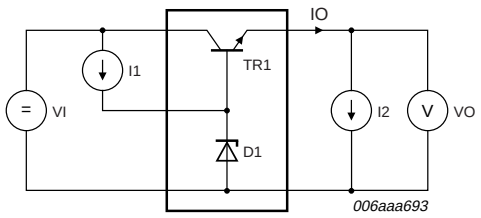


Fig 10. Voltage regulator test setup

9. Package outline

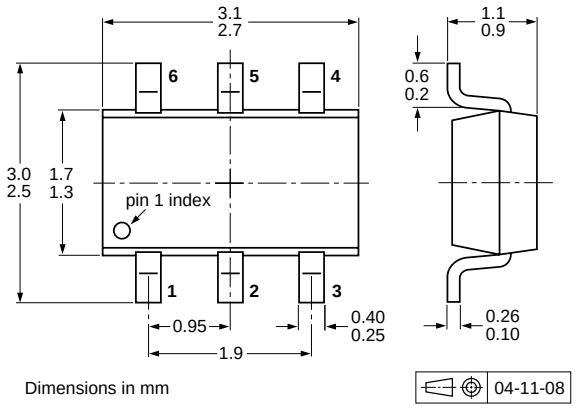


Fig 11. Package outline SOT457 (SC-74)

10. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

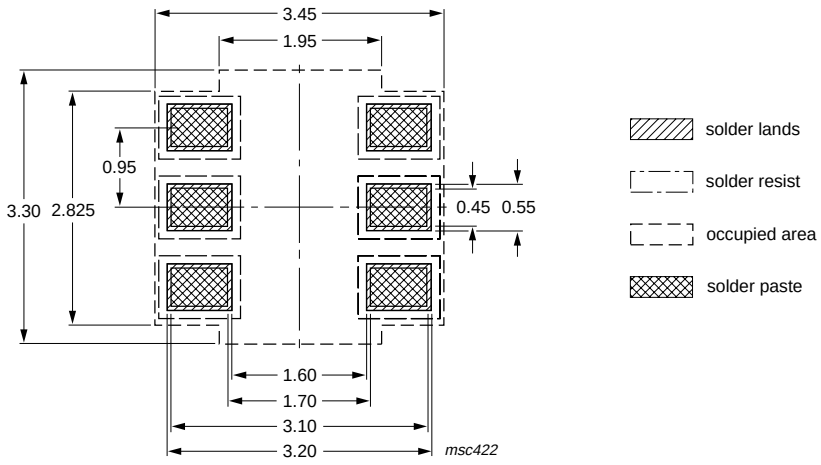
Type number	Package	Description		Packing quantity	
				3000	10000
PVR100AD-B2V5	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-165
PVR100AD-B3V0	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-165
PVR100AD-B3V3	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-165
PVR100AD-B5V0	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-165
PVR100AD-B12V	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-165

[1] For further information and the availability of packing methods, see Section 14.

[2] T1: normal taping

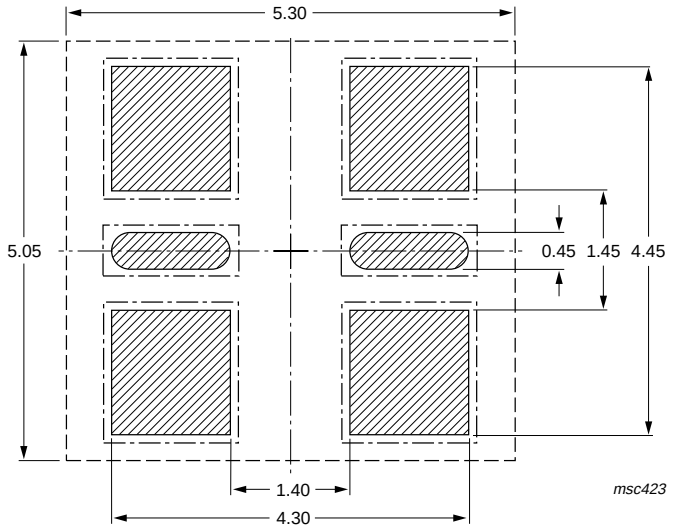
[3] T2: reverse taping

11. Soldering



Dimensions in mm

Fig 12. Reflow soldering footprint SOT457 (SC-74)



Dimensions in mm

Fig 13. Wave soldering footprint SOT457 (SC-74)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PVR100AD-B_SER_1	20061031	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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15. Contents

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