MPV3 Series
9x14 mm, 3.3 Volt, LVPECL/LVDS, VCXO

MtronPTI®

RoHS Compliant

- Versatile VCXO to 800 MHz with good jitter (3 ps typical)
- Used in low jitter clock synthesizers and SONET applications

Mechanical Dimensions

0.565 (14.22) MAX

6 5 4

0.385 (9.78) MAX

0.035 (0.89) RAD REF

0.300 (7.62) TYP

1 2 3

@ DENOTES PIN 1.

All dimensions in inches (mm).

0.185 (4.70) MAX
0.040 (1.02) TYP
0.018 (0.46) TYP

0.200 (5.08) TYP
0.100 (2.54) TYP

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SUGGESTED SOLDER PAD LAYOUT

0.200 (5.08)
0.050 (1.27)
0.118 (3.00)
0.346 (8.80)
0.100 (2.54)
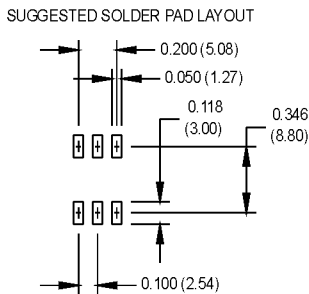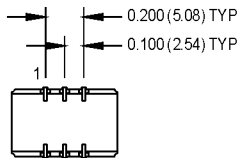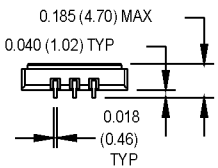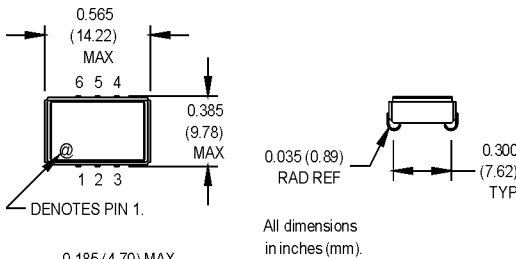
Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Enable/Disable or N/C
3	Ground/Case
4	Output Q
5	Output Q̄ or N/C
6	+Vcc

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	0.75		800	MHz	
Operating Temperature	TA	(See Ordering Information)				
Storage Temperature	Ts	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				See Note 1
Aging						
1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz
Pullability/APR		(See Ordering Information)				See Note 2
Control Voltage	Vc	0.3	1.65	3	V	Pin 1 voltage
Linearity			5	10	%	Positive Monotonic Slope
Modulation Bandwidth	fm	10			kHz	-3 dB bandwidth
Input Impedance	Zin	50k			Ohms	
Input Voltage	Vcc	3.135	3.3	3.465	V	
Input Current	Icc					
0.75 MHz to 26 MHz				60/30	mA	PECL/LVDS
26 MHz to 104 MHz				95/60	mA	PECL/LVDS
104 MHz to 800 MHz				105/60	mA	PECL/LVDS
Output Type						PECL/LVDS
Load						See Note 3
			50 Ohms to Vcc -2 VDC			PECL waveform
			100 Ohm differential load			LVDS waveform
Symmetry (Duty Cycle)						Vcc -1.3 VDC (PECL)
(Per Symmetry Code)		(See Ordering Information)				50% of Waveform (LVDS)
Output Skew				200	ps	
Differential Voltage	Vo	250	340	450	mV	LVDS only
Logic "1" Level	Voh	Vcc -1.02			V	PECL
Logic "0" Level	Vol			Vcc -1.63	V	PECL
Rise/Fall Time	Tr/Tf		0.35	0.55	ns	@ 20/80% LVPECL
			.50	1.0	ns	@ 20/80% LVDS
Enable Function		80% Vcc min or N/C: output active				
		20% Vcc max: output disables to high-Z				
Start up Time			5		ps	
Phase Jitter	φ J		3	5	ps RMS	Integrated 12 kHz - 20 MHz

Phase Noise (Typical)

Phase Noise (Typical)	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier
@ 19.44 MHz	-60	-90	-112	-140	-150	dBc/Hz
@ 155.52 MHz	-60	-90	-112	-123	-120	dBc/Hz
@ 622.08 Mhz	-60	-90	-108	-108	-105	dBc/Hz

1. Stability given for deviation over temperature.
2. APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging.
3. PECL load - see load circuit diagram #5.   LVDS load - see load circuit diagram #9.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.

Please see **www.mtronpti.com** for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI **1-800-762-8800.**

Revision: 11-21-06

MtronPTI Lead Free Solder Profile

RAMP-UP
3°C/SECOND MAX.

CRITICAL TEMPERATURE
ZONE

RAMP-DOWN
6°C/SECOND

260°C
217°C
200°C
150°C

TEMPERATURE

PREHEAT
180 SECONDS MAX.

90 SECONDS MAX.

8 MINUTES MAX.

260°C MAX. FOR 10 SECONDS MAX.

TIME

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