On-Screen Display Controller for CRT/LCD Monitor

FEATURES

- Horizontal SYNC input up to 150 KHz.
- On-chip PLL circuitry or external pixel clock input up to 150 MHz.
- *Software control for CRT/LCD applications.*
- *Programmable R,G,B input level for timing measurement among HFLB, VFLB, RIN, GIN and BIN for auto sizing.*
- Full screen self-test pattern generator.
- Programmable Hor. resolutions up to 1524 dots per line.
- Full-screen display consists of 15 (rows) by 30 (columns)
- Two font size 12x16 or 12x18 dot matrix per character.
- *True totally 544 mask ROM fonts including 512 standard fonts and 32 multi-color fonts.*
- *Character button boxes with programmable box length.*
- Double character height and/or width control.
- Programmable positioning for display screen center.
- Character bordering, shadowing and blinking effect.
- *Character (per row) and window intensity control.*
- Row to row spacing control to avoid expansion distortion.
- 4 programmable windows with multi-level operation.
- Shadowing on windows with programmable shadow width/height/color.
- Programmable adaptive approach to handle H, V sync collision automatically by hardware.
- Software clears bit for full-screen erasing.
- Fade-in/fade-out or blending-in/blending-out effects.
- Compatible with SPI bus or I^{2}C interface with slave address 7AH/7BH (slave address is mask option).
- 16-pin or 20-pin PDIP/SOP package.

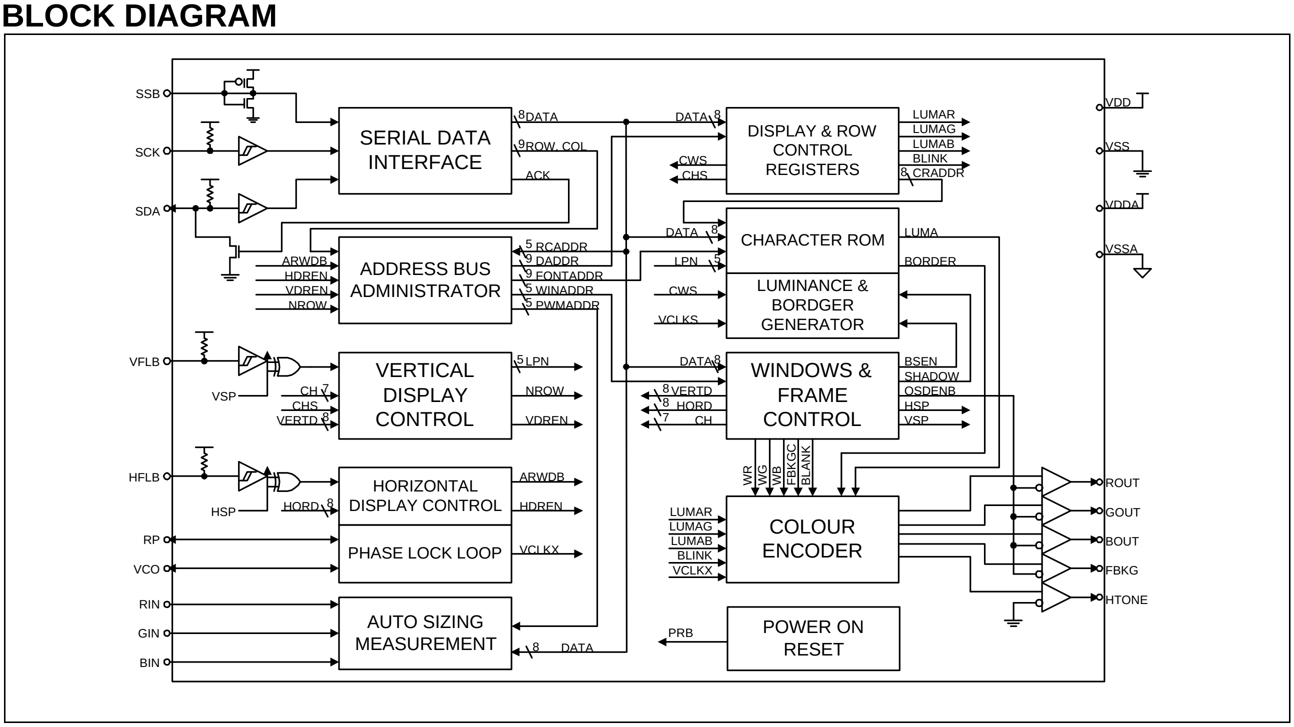
GENERAL DESCRIPTION

MTV038 is designed for CRT/LCD monitor applications to display built-in characters or fonts onto monitor screens. The display operation occurs by transferring data and control information from the micro-controller to RAM through a serial data interface. It can execute full-screen display automatically, as well as specific functions such as character background, bordering, shadowing, blinking, double height and width, font by font color control, character button boxes, frame positioning, frame size control by character height and row-to-row spacing, horizontal display resolution, full-screen erasing, fade-in/fade-out effect, windowing effect, shadowing on window and full-screen self-test pattern generator.

MTV038 provides 544 fonts including 512 standard fonts and 32 multi-color fonts and 2 font sizes, 12x16 or 12x18 for more efficacious applications. The full OSD menu is formed by 15 rows x 30 columns, which can be positioned anywhere on the monitor screen by changing vertical or horizontal delay.

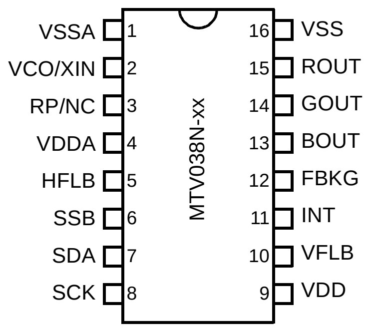
The auto sizing video measurement module measure the timing relationship among HFLB, VFLB, and R, G, BIN with 12-bit resolution at the speed related to the OSD pixel clock. And the R, G, BIN input level can be programming by software. MCU can get the measurement data, active video, front porth and back porth, through I^{2}C bus read/write operation to keep the appropriate display size and center.

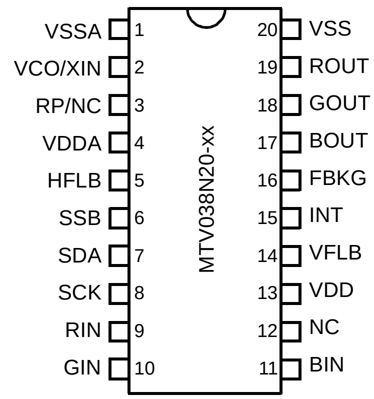
BLOCK DIAGRAM



This datasheet contains new product information. Myson Technology reserves the rights to modify the product specification without notice. No liability is assumed as a result of the use of this product. No rights under any patent accompany the sales of the product.

1.0 PIN CONNECTION





2.0 PIN DESCRIPTIONS

Name	I/O	Pin No.		Descriptions
		16	20	
VSSA	-	1	1	**Analog ground.** This ground pin is used to internal analog circuitry.
VCO/XIN	I/O	2	2	**Voltage Control Oscillator (bit LCD= 0).** This pin is used to control the internal oscillator frequency by DC voltage input from external low pass filter. **Pixel Clock Input (bit LCD= 1).** This is a clock input pin. MTV038 can be driven by an external pixel clock source for all the logics inside. The frequency of XIN must be the integral time of pin HFLB.
RP/NC	I/O	3	3	**Bias Resistor (bit LCD= 0).** The bias resistor is used to regulate the appropriate bias current for internal oscillator to resonate at specific dot frequency. **No connection (bit LCD= 1).**
VDDA	-	4	4	**Analog power supply.** Positive 5 V DC supply for internal analog circuitry. And a 0.1uF decoupling capacitor should be connected across to VDDA and VSSA.
HFLB	I	5	5	**Horizontal input.** This pin is used to input the horizontal synchronizing signal. It is a leading edge triggered and has an internal pull-up resistor.
SSB	I	6	6	**Serial interface enable.** It is used to enable the serial data and is also used to select the operation of I^2C or SPI bus. If this pin is left floating, I^2C bus is enabled, otherwise the SPI bus is enabled.
SDA	I	7	7	**Serial data input.** The external data transfer through this pin to internal display registers and control registers. It has an internal pull-up resistor.

Name	I/O	Pin No.		Descriptions
		16	20	
SCK	I	8	8	**Serial clock input.** The clock-input pin is used to synchronize the data transfer. It has an internal pull-up resistor.
RIN	I	-	9	**Red video input.** It is used for auto sizing measurement and this signal is came from video pre-amp red output.
GIN	I	-	10	**Green video input.** It is used for auto sizing measurement and this signal is came from video pre-amp green output.
BIN	I	-	11	**Blue video input.** It is used for auto sizing measurement and this signal is came from video pre-amp blue output.
NC	-	-	12	**No connection.**
VDD	-	9	13	**Digital power supply.** Positive 5 V DC supply for internal digital circuitry and a 0.1uF decoupling capacitor should be connected across to VDD and VSS.
VFLB	I	10	14	**Vertical input.** This pin is used to input the vertical synchronizing signal. It is leading triggered and has an internal pull-up resistor.
INT	O	11	15	**Intensity color output.** 16-color selection is achievable by combining this intensity pin with R/G/B output pins.
FBKG	O	12	16	**Fast Blanking output.** It is used to cut off external R, G, B signals of VGA while this chip is displaying characters or windows.
BOUT	O	13	17	**Blue color output.** It is a blue color video signal output.
GOUT	O	14	18	**Green color output.** It is a green color video signal output.
ROUT	O	15	19	**Red color output.** It is a red color video signal output.
VSS	-	16	20	**Digital ground.** This ground pin is used to internal digital circuitry.

3.0 FUNCTIONAL DESCRIPTIONS

3.1 SERIAL DATA INTERFACE

The serial data interface receives data transmitted from an external controller. And there are 2 types of bus can be accessed through the serial data interface, one is SPI bus and other is I^2C bus.

3.1.1 SPI bus

While SSB pin is pulled to "high" or "low" level, the SPI bus operation is selected. And a valid transmission should be starting from pulling SSB to "low" level, enabling MTV038 to receiving mode, and retain "low" level until the last cycle for a complete data packet transfer. The protocol is shown in Figure 1.

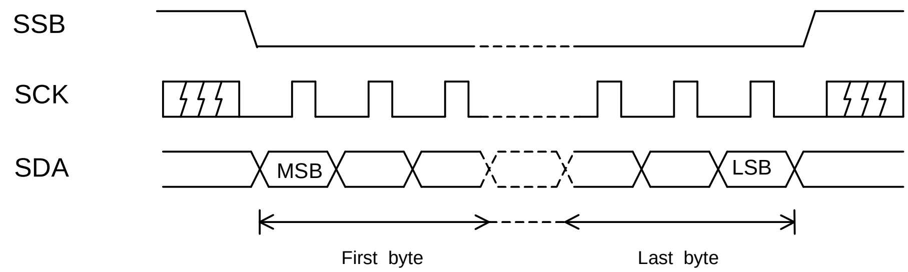


FIGURE 1. Data Transmission Protocol (SPI)

There are three transmission formats shown as below:
Format (a) R - C - D -> R - C - D -> R - C - D .....
Format (b) R - C - D -> C - D -> C - D -> C - D .....
Format (c) R - C - D -> D -> D -> D -> D -> D .....
Where R=Row address, C=Column address, D=Display data

3.1.2 I^2C bus

I^2C bus operation is only selected when SSB pin is left floating. And a valid transmission should be starting from writing the slave address 7AH(write mode), or 7BH(read mode) to MTV038. The protocol is shown in Figure 2. And the auto sizing video measurement data (total 12 bytes) are read only registers and the others are write only registers.

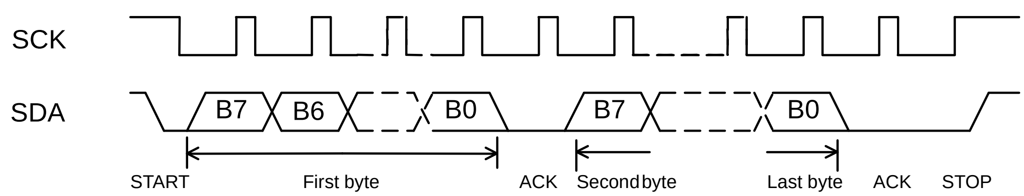


FIGURE 2. Data Transmission Protocol (I^2C)

There are three transmission formats for I^2C write mode shown as below:
Format (a) S - R - C - D -> R - C - D -> R - C - D .....
Format (b) S - R - C - D -> C - D -> C - D -> C - D .....
Format (c) S - R - C - D -> D -> D -> D -> D -> D .....
Where S=Slave address, R=Row address, C=Column address, D=Display data

And there is one transmission formats for I^2C read mode shown as below:
Format (a) S -> D -> D -> D -> D -> D -> D -> D -> D -> D -> D -> D -> D -> D -> D -> dummy D .....
Where S=Slave address, D=Measurement data

In the I^2C read mode, 14 bytes of auto sizing video measurement data will be outputed directly from byte 0 to byte 9 and continues with dummy data until stop condition occurred when R/W bit is set to 1.

Each arbitrary length of data packet consists of 3 portions viz, Row address (R), Column address (C), and Display data (D). Format (a) is suitable for updating small amount of data which will be allocated with a different row address and column address. Format (b) is recommended for updating data that has the same row address but a different column address. Massive data updating or full screen data change should use format (c) to increase transmission efficiency. The row and column address will be incremented automatically when the format (c) is applied. Furthermore, the undefined locations in display or fonts RAM should be filled with dummy data.

TABLE 1. The Configuration of Transmission Formats

	Address	b7	b6	b5	b4	b3	b2	b1	b0	Format
Address Bytes of Display Reg.	Row	1	0	0	R4	R3	R2	R1	R0	a,b,c
	Column$_{ab}$	0	0	**D8**	C4	C3	C2	C1	C0	a,b
	Column$_{c}$	0	1	**D8**	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c
Attribute Bytes of Display Reg.	Row	1	0	1	R4	R3	R2	R1	R0	a,b,c
	Column$_{ab}$	0	0	x	C4	C3	C2	C1	C0	a,b
	Column$_{c}$	0	1	x	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c

There are 2 types of data which should be accessed through the serial data interface, one is **ADDRESS** bytes of display registers, and the other is **ATTRIBUTE** bytes of display registers, the protocols are same for all except the bit5 of row address and the bit5 of column address. The MSB(b7) is used to distinguish row and column addresses when transferring data from external controller. The bit6 of column address is used to differentiate the column address for format (a), (b) and format (c) respectively. Bit5 of row address for display register is used to distinguish ADDRESS byte when it is set to "0" and ATTRIBUTE byte when it is set to "1". And **at address bytes, bit5 of column address is the MSB (bit8) and data bytes are the 8 LSB (bit7~bit0) of display fonts address** to save half MCU memory for true 512 fonts display. So each one of the 512 fonts can be displayed at the same time (see Table 1). And for format (c), since D8 is filled while program column address of address bytes, the continued data will be the same bank of upper 256 fonts or lower 256 fonts until program column address of address bytes again.
The data transmission is permitted to change from format (a) to format (b) and (c), or from format (b) to format (a) and (c), but not from format (c) back to format (a) and (b). The alternation between transmission formats is configured as the state diagram shown in Figure 3.

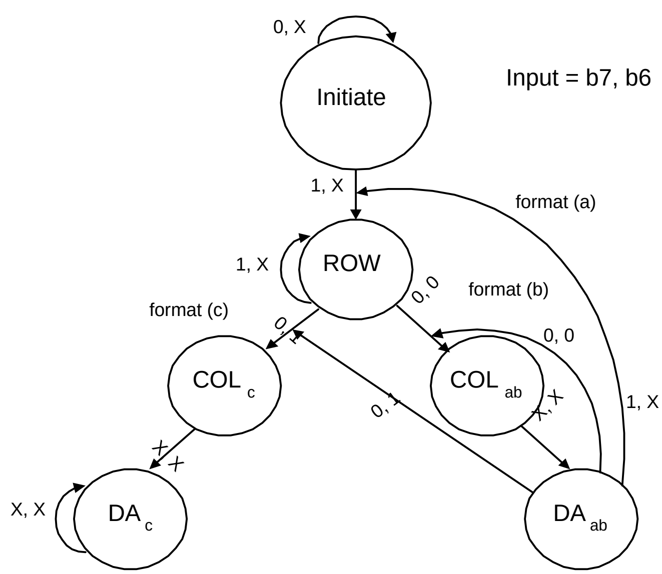


FIGURE 3. Transmission State Diagram

3.2 Address bus administrator

The administrator manages bus address arbitration of internal registers or user fonts RAM during external data write in. The external data write through serial data interface to registers must be synchronized by internal display timing. In addition, the administrator also provides automatic increment to address bus when external write using format (c).

3.3 Vertical display control

The vertical display control can generates different vertical display sizes for most display standards in current monitors. The vertical display size is calculated with the information of double character height bit(CHS), vertical display height control register(CH6-CH0).The algorithm of repeating character line display are shown as Table 2 and Table 3. The programmable vertical size range is 270 lines to maximum 2130 lines.

The vertical display center for full screen display could be figured out according to the information of vertical starting position register (VERTD) and VFLB input. The vertical delay starting from the leading edge of VFLB, is calculated with the following equation:

Vertical delay time = (VERTD * 4 + 1) * H   Where H = one horizontal line display time

TABLE 2. Repeat Line Weight of Character

CH6 - CH0	Repeat Line Weight
CH6,CH5=11	+18*3
CH6,CH5=10	+18*2
CH6,CH5=0x	+18
CH4=1	+16
CH3=1	+8
CH2=1	+4
CH1=1	+2
CH0=1	+1

TABLE 3. Repeat Line Number of Character

Repeat Line Weight	Repeat Line #																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
+1	-	-	-	-	-	-	-	-	v	-	-	-	-	-	-	-	-	-
+2	-	-	-	-	v	-	-	-	-	-	-	-	v	-	-	-	-	-
+4	-	-	v	-	-	-	v	-	-	-	v	-	-	-	v	-	-	-
+8	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	-
+16	-	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+17	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+18	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v

Note:" v " means the nth line in the character would be repeated once, while " - " means the nth line in the character would not be repeated.

3.4 Horizontal display control

The horizontal display control is used to generate control timing for horizontal display based on double character width bit (CWS), horizontal positioning register (HORD), horizontal resolution register (HORR), and HFLB input. A horizontal display line consists of (HORR*12) dots which include 360 dots for 30 display characters and the remaining dots for blank region. The horizontal delay starting from HFLB leading edge is calculated with the following equation,

For CRT: Horizontal delay time = (HORD * 6 + 49) * P - phase error detection pulse width
Where P = One pixel display time = One horizontal line display time / (HORR*12)

For LCD: Horizontal delay time = (HORD * 6 + 49) * P
Where P = 1 XIN pixel display time

3.5 Phase lock loop (PLL)

On-chip PLL generates system clock timing (VCLK) by tracking the input HFLB and horizontal resolution register (HORR). The frequency of VCLK is determined by the following equation:

VCLK Freq = HFLB Freq * HORR * 12

The VCLK frequency ranges from 6MHz to 150MHz selected by (VCO1, VCO0). In addition, when HFLB input is not present to MTV038, the PLL will generate a specific system clock, approximately 2.5MHz, by a built-in oscillator to ensure data integrity.

3.6 Display & Row control registers

The internal RAM contains display and row control registers. The display registers have 450 locations which are allocated between (row 0, column 0) to (row 14, column 29), as shown in Figure 4 and Figure 5. Each display register has its corresponding character address on ADDRESS byte, its corresponding background color, button box format, 1 blink bit and its corresponding color bits on ATTRIBUTE bytes. The row control register is allocated at column 30 for row 0 to row 14 of attribute bytes, it is used to select background color or button box and set character size to each respective row. If double width character is chosen, only even column characters could be displayed on screen and the odd column characters will be hidden.

ROW #	COLUMN #		
	0 1 ... 28 29	30	31
0 1 ... 13 14	CHARACTER ADDRESS BYTES of DISPLAY REGISTERS	ROW ATTRIBUTE CRTL REG	R E S E R V E D

FIGURE 4. Address Bytes of Display Registers Memory Map

ROW #	COLUMN # 0 1 ... 28 29	30 ... 31
0 1 ... 13 14	CHARACTER ATTRIBUTE BYTES of DISPLAY REGISTERS	RESERVED

ROW 15	COLUMN#		
	0 ... 11	12 ... 22	23 ... 31
	WINDOW1 ~ WINDOW4	FRAME CRTL REG	RESERVED

ROW 16	COLUMN#		
	0 ... 1	2 ... 4	5 ... 31
	WINDOW SHADOW COLOR	FRAME CRTL REG	RESERVED

FIGURE 5. Attribute Bytes of Display Registers Memory Map

ADDRESS BYTES:
Address registers,

b8	b7	b6	b5	b4	b3	b2	b1	b0
CRADDR MSB ... LSB								

CRADDR - Define ROM character address from address 0 to 511.

Row Control Registers, (Row 0 - 14)

	b7	b6	b5	b4	b3	b2	b1	b0
COLN 30	-	-	-	BOX	BGINT	FGINT	CHS	CWS

BOX - Select BGR, BGG, BGB or B2, B1, B0 of attributes bytes to the respective row.
= 0 -> Background color bits BGR, BGG, BGB are selected.
= 1 -> Button box bits B2, B1, B0 are selected.

BGINT - The displayed character/symbol background color intensity control to the respective row. Setting this bit to 0 means low intensity in this row. 16 character background color is achievable by this bit.

FGINT - The displayed character/symbol foreground color intensity control to the respective row. Setting this bit to 0 means low intensity in this row. 16 character foreground color is achievable by this bit.

CHS - Define double height character to the respective row.

CWS - Define double width character to the respective row.

ATTRIBUTE BYTES:

b7	b6	b5	b4	b3	b2	b1	b0
-	BGR/B2	BGG/B1	BGB/B0	BLINK	R	G	B

BGR, BGG, BGB - These three bits define the color of the background for its relative address character. If all three bits are clear, no background will be shown(transparent). Therefore, a total of 7 background colors can be selected.

B2, B1, B0 - Select the character button boxes format of its relative address character.
= 0, 0, 0 -> Button box is disabled.
= 1, 0, 0 -> Start of depressed button box which is more than 1 character button box.
= 1, 0, 1 -> Start of depressed button box which is only 1 character button box.
= 1, 1, 0 -> Start of raised button box which is more than 1 character button box.
= 1, 1, 1 -> Start of raised button box which is only 1 character button box.
= 0, 1, 0 -> Middle of button box.
= 0, 0, 1 -> End of button box.

BLINK - Enable blinking effect while this bit is set to " 1 ". And the blinking is alternate per 32 vertical frames.

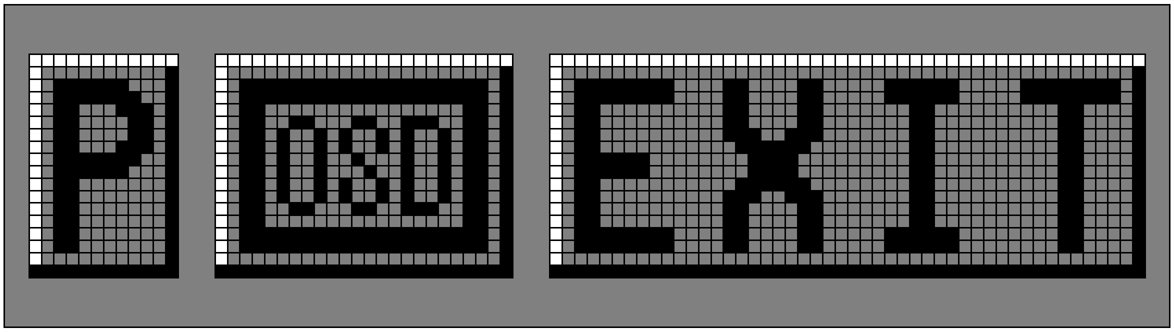
R, G, B - These three bits are used to specify its relative address character color.

3.7 Character button box generator

There are 4 character button box generators to generate 4 different types of button boxes including depressed button box with only 1 character, depressed button box with more than 1 character, raised button box with only 1 character, and raised button box with more than 1 character. The button boxes format is defined by (B2, B1, B0) bits of attribute bytes. And these bits are described as below:

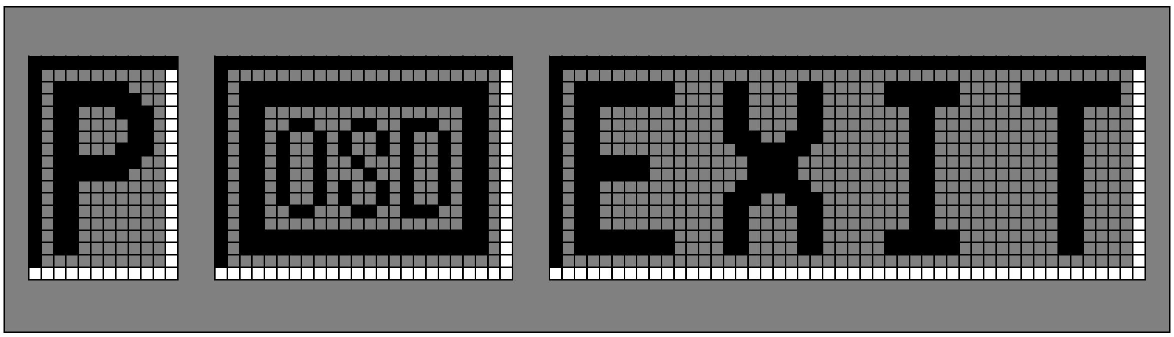
1).(1, x, x) means the start of character button box, and then B1, B0 mean button boxes format.
2).(0, 1, 0) means the middle of character button box.
3).(0, 0, 1) means the end of character button box.

The length of button box is also software control by (B2, B1, B0) bits. For example, if there is 1 raised button box which length is equal to 6 characters, these (B2, B1, B0) bits will be (1, 1, 0), (0, 1, 0), (0, 1, 0), (0, 1, 0), (0, 1, 0), (0, 0, 1). And if there is 1 depressed button box of which the length is equal to 4 characters, these (B2, B1, B0) bits will be (1, 0, 0), (0, 1, 0), (0, 1, 0), (0, 0, 1). That is, (0, 1, 0) command number define the button box length. And only one byte, the attribute byte of button box start character, should be modified when we want to change button box type to raised or depressed button. This is very easy and useful for software programming.



B2~B0 = **1, 1, 1** **1, 1, 0** **0, 0, 1** **1, 1, 0** **0, 1, 0** **0, 1, 0** **0, 0, 1**

Raised Button Boxes



B2~B0 = **1, 0, 1** **1, 0, 0** **0, 0, 1** **1, 0, 0** **0, 1, 0** **0, 1, 0** **0, 0, 1**

Depressed Button Boxes

FIGURE 6. Character Button Boxes

3.8 Character ROM

MTV038 character ROM contains 544 built-in characters and symbols including 512 standard fonts and 32 multi-color fonts. The 512 standard fonts are located from address 0 to 511. And the 32 multi-color fonts are located from address 480 to 511 while CFONT bits is set to 1. Each character and symbol consists of 12x18 dots matrix.

3.9 Multi-Color Font

The color fonts comprises three different R, G, B fonts. When the code of color font is accessed, the separate R/G/B dot pattern is output to corresponding R/G/B output. See Figure 7 for the sample displayed color font. Note: No black color can defined in color font, black window underline the color font can make the dots become black in color.

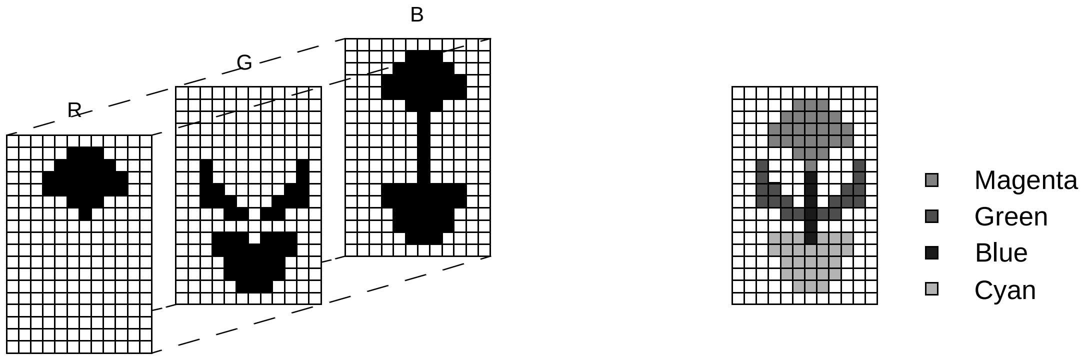


FIGURE 7. Example of Multi-Color Font

TABLE 4. The Multi-Color Font Color Selection

	R	G	B
Background Color	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

3.10 Luminance & border generator

There are 3 shift registers included in the design which can shift out of luminance and border dots to color encoder. The bordering and shadowing feature is configured in this block. For bordering effect, the character will be enveloped with blackedge on four sides. For shadowing effect, the character is enveloped with blackedge for right and bottom sides only.

3.11 Window and frame control

The display frame position is completely controlled by the contents of VERTD and HORD. The window size and position control are specified in column 0 to 11 on row 15 of memory map, as shown in Figure 5. Window 1 has the highest priority, and window 4 is the least, when two windows are overlapping. More detailed information is described as follows:

1. Window control registers,
ROW 15

<table>
<tr><td rowspan="2">Column 0,3,6,OR 9</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr>
<tr><td colspan="4">ROW START ADDR
MSB LSB</td><td colspan="4">ROW END ADDR
MSB LSB</td></tr>
</table>

<table>
<tr><td rowspan="2">Column 1,4,7,OR 10</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr>
<tr><td colspan="5">COL START ADDR
MSB LSB</td><td>WEN</td><td>WINT</td><td>WSHD</td></tr>
</table>

Column 2,5,8,OR 11	b7	b6	b5	b4	b3	b2	b1	b0
	COL END ADDR (MSB … LSB)					R	G	B

START(END) ADDR - These addresses are used to specify the window size. It should be noted that when the start address is greater than the end address, the window will be disabled.

WEN - Enable the relative background window display.

WINT - Specify the color intensity of the relative background window. Setting this bit to 0 means low intensity in this background window.

WSHD - Enable shadowing on the relative window.

R, G, B - Specify the color of the relative background window.

2. Frame control registers,
ROW 15

Column 12	b7	b6	b5	b4	b3	b2	b1	b0
	VERTD (MSB … LSB)							

VERTD - Specify the starting position for vertical display. The total steps are 256, and the increment of each step is 4 Horizontal display lines. The initial value is 4 after power up.

Column 13	b7	b6	b5	b4	b3	b2	b1	b0
	HORD (MSB … LSB)							

HORD - Define the starting position for horizontal display. The total steps are 256, and the increment of each step is 6 dots. The initial value is 15 after power up.

Column 14	b7	b6	b5	b4	b3	b2	b1	b0
	-	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CH6-CH0 - Define the character vertical height, the height is programmable from 18 to 71 lines. The character vertical height is at least 18 lines if the contents of CH6-CH0 is less than 18. For example, when the contents is " 2 ", the character vertical height is regarded as equal to 20 lines. And if the contents of CH4-CH0 is greater than or equal to 18, it will be regarded as equal to 17. See Table 2 and Table 3 for detail description of this operation.

Column 15	b7	b6	b5	b4	b3	b2	b1	b0
	-	HORR (MSB … LSB)						

(This byte is used only for CRT monitor application.)

HORR - Specify the resolution of a horizontal display line, and the increment of each step is 12 dots. That is, the number of pixels per H line equal to HORR*12. It is recommended that HORR should be greater than or equal to 36 and smaller than 150M / (Hfreq*12). The initial value is 40 after power up.

Column 16	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	RSPACE MSB … LSB				

RSPACE - Define the row to row spacing in unit of horizontal line. That is, extra RSPACE horizontal lines will be appended below each display row, and the maximum space is 31 lines. The initial value is 0 after power up.

Column 17	b7	b6	b5	b4	b3	b2	b1	b0
	OSDEN	BSEN	SHADOW	FBEN	BLEND	WENCLR	RAMCLR	FBKGC

OSDEN - Activate the OSD operation when this bit is set to "1". The initial value is 0 after power up.

BSEN - Enable the bordering and shadowing effect.

SHADOW - Bordering and shadowing effect select bit. Activate the shadowing effect if this bit is set, otherwise the bordering is chosen.

FBEN - Enable the fade-in/fade-out and blending-in/blending-out effect when OSD is turned on from off state or vice versa.

BLEND - Fade-in/fade-out and blending-in/blending-out effect select bit. Activate the blendinf-in/blending-out function if this bit is set, otherwise the fade-in/fade-out function is chosen. These function roughly takes about 0.5 second to fully display the whole menu or to disappear completely.

WENCLR - Clear all WEN bits of window control registers when this bit is set to "1". The initial value is 0 after power up.

RAMCLR - Clear all ADDRESS bytes, BGR, BGG, BGB and BLINK bits of display registers when this bit is set to "1". The initial value is 0 after power up.

FBKGC - Define the output configuration for FBKG pin. When it is set to "0", the FBKG outputs high during the displaying of characters or windows, otherwise, it outputs high only during the displaying of character.

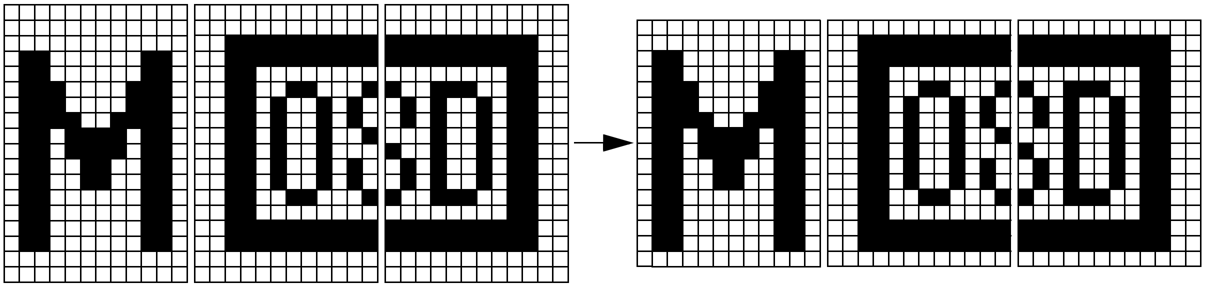
Column 18	B7	b6	b5	b4	b3	b2	b1	b0
	TRIC	FSS	-	SELVCL/DWE	HSP	VSP	VCO1/-	VCO0/-

(SELVCL, VCO1, VCO0 bits are used only for CRT monitor application.)
(DWE bit is used only for LCD monitor application.)

TRIC - Define the driving state of output pins ROUT, GOUT, BOUT and FBKG when OSD is disabled. That is, while OSD is disabled, these four pins will drive low if this bit is set to 1, otherwise these four pins are in high impedance state. The initial value is 0 after power up.

FSS - Font size selection.
= 1 -> 12x18 font size selected.
= 0 -> 12x16 font size selected.

SELVCL - Enable auto detection for horizontal and vertical syncs input edge distortion to avoid unstable Vsync leading mismatch with Hsync signal while the bit is set to "1". The initial value is 0 after power up.



Fonts designed to be 12x18 display

Output display if FSS=0; first and last lines omitted

FIGURE 8. 12x18 and 12x16 Fonts

DWE - Enable double width. When the bit is set to 1, the display of OSD menu can change to half resolution for double character width, and then the number of pixels of each line should be even. The initial value is 0 after power up.

HSP - = 1 -> Accept positive polarity Hsync input.
= 0 -> Accept negative polarity Hsync input.

VSP - = 1 -> Accept positive polarity Vsync input.
= 0 -> Accept negative polarity Vsync input.

VCO1, VCO0 - Select the appropriate curve partitions of VCO frequency to voltage based on HFLB input and horizontal resolution register (HORR). And there are different curve partitions based on different application resister value on pin 3 (pin RP) as below:

(i)R_{RP} = 5.6K ohm:

= (0, 0) -> 6MHz < Pixel rate ≤ 24MHz
= (0, 1) -> 24MHz < Pixel rate ≤ 48MHz
= (1, 0) -> 48MHz < Pixel rate ≤ 96MHz
= (1, 1) -> 96MHz < Pixel rate ≤ 128MHz

(ii)2.2K ohm ≤ R_{RP} ≤ 3.3K ohm:

= (0, 0) -> 6MHz < Pixel rate ≤ 28MHz
= (0, 1) -> 28MHz < Pixel rate ≤ 56MHz
= (1, 0) -> 56MHz < Pixel rate ≤ 112MHz
= (1, 1) -> 112MHz < Pixel rate ≤ 150MHz

Where Pixel rate = VCLK Freq = HFLB Freq * HORR * 12
The initial value is (0, 0) after power up.

Notes :

1. That is, if HORR is specified and RP resister = 3.3K ohm, then (VCO1, VCO0)
   = (0, 0) if 6000/(HORR * 12) < HFLB Freq (KHz) ≤ 28000/(HORR * 12)
   = (0, 1) if 28000/(HORR * 12) < HFLB Freq (KHZ) ≤ 56000/(HORR * 12)
   = (1, 0) if 56000/(HORR * 12) < HFLB Freq (KHZ) ≤ 112000/(HORR * 12)
   = (1, 1) if 112000/(HORR * 12) < HFLB Freq (KHZ) ≤ 150000/(HORR * 12)
2. It is necessary to wait for the PLL to become stable while (i) the HORR register is being changed; (ii) the (VCO1, VCO0) bits is changed; (iii) the horizontal signal (HFLB) is changed.
3. When PLL is unstable, don't write data in any address except Column 15,17,18 of Row 15. If data is written in any other address, a malfunction may occur.

Column 19	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	CSR	CSG	CSB

CSR, CSG, CSB - Define the color of bordering or shadowing on characters. The initial value is (0, 0, 0) after power up.

Column 20	B7	b6	b5	b4	b3	b2	b1	b0
	FSW	-	-	-	-	FSR	FSG	FSB

FSW - Enable full screen self-test pattern and force the FBKG pin output to high to disable video RGB while this bit is set to 1. The color of the self-test pattern is determined by (FSR, FSG, FSB) bits.

FSR, FSG, FSB - Define the color of full screen self-test pattern.

Column 21	B7	b6	b5	b4	b3	b2	b1	b0
	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

WW41, WW40 - Determines the shadow width of the window 4 when WSHD bit of the window 4 is enabled. Please refer to the Table 5 for more details.

TABLE 5. Shadow Width Setting

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width (unit in Pixel)	2	4	6	8

WW31, WW30 - Determines the shadow width of the window 3 when WSHD bit of the window 3 is enabled.

WW21, WW20 - Determines the shadow width of the window 2 when WSHD bit of the window 2 is enabled.

WW11, WW10 - Determines the shadow width of the window 1 when WSHD bit of the window 1 is enabled.

Column 22	B7	b6	b5	b4	b3	b2	b1	b0
	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

WH41, WH40 - Determines the shadow height of the window 4 when WSHD bit of the window 4 is enabled. Please refer to the Table 6 for more details.

TABLE 6. Shadow Height Setting

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height (unit in Line)	2	4	6	8

WH31, WH30 - Determines the shadow height of the window 3 when WSHD bit of the window 3 is enabled.
WH21, WH20 - Determines the shadow height of the window 2 when WSHD bit of the window 2 is enabled.
WH11, WH10 - Determines the shadow height of the window 1 when WSHD bit of the window 1 is enabled.

3.12 Color encoder

The encoder generates the video output to ROUT, GOUT and BOUT by integrating window color, border blackedge, luminance output and color selection output (R, G, B) to form the desired video outputs.

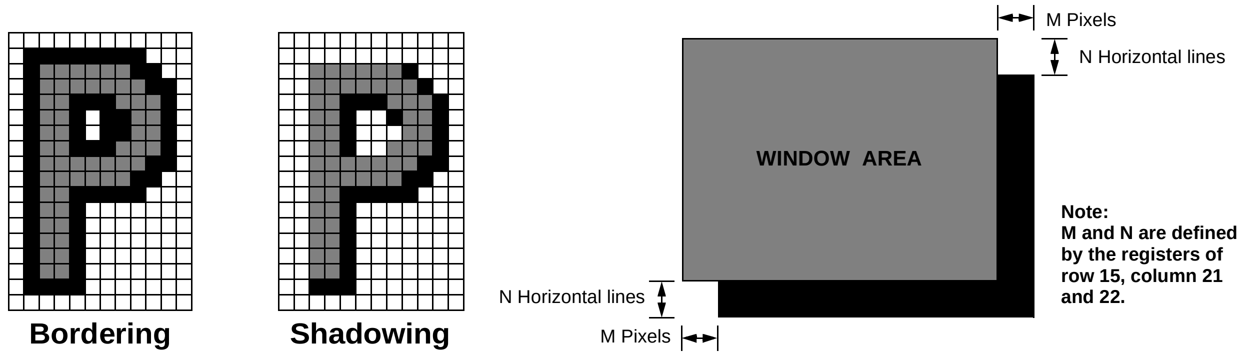


FIGURE 9. Character Bordering and Shadowing and Shadowing on Window

Column 23 ~ column 31 : Reserved.

Notes : The register located at column 31 of row 15 is reserved for the testing. Don't program this byte anytime in normal operation.

ROW 16

Column 0	B7	b6	b5	b4	b3	b2	b1	b0
	-	R1	G1	B1	-	R2	G2	B2

R1, G1, B1 - Define the shadow color of window 1. The initial value is (0, 0, 0) after power up.

R2, G2, B2 - Define the shadow color of window 2. The initial value is (0, 0, 0) after power up.

Column 1	B7	b6	b5	b4	b3	b2	b1	b0
	-	R3	G3	B3	-	R4	G4	B4

R3, G3, B3 - Define the shadow color of window 3. The initial value is (0, 0, 0) after power up.

R4, G4, B4 - Define the shadow color of window 4. The initial value is (0, 0, 0) after power up.

Column 2	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	D2	D1	D0

(This byte is used only for LCD monitor application.)

D2-D0 - These 3 bits define the propagation delay of R, G, B, FBKG and INT output pins to XIN pin. Please refer to Figure 13 and Table 7. The initial value is (0, 0, 0) after power up.

TABLE 7. Output timing to Pixel Clock

Symbol	(D2, D1, D0)	Min.	Typ.	Max.	Unit
t_{pd}	0	2	-	4	ns
	1	3	-	5	ns
	2	4	-	6	ns
	3	5	-	7	ns
	4	6	-	8	ns
	5	7	-	9	ns
	6	8	-	10	ns
	7	9	-	11	ns

Column 3	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	CFONT3	CFONT2	CFONT1	CFONT0

CFONT0 - Enable 1st 8 multi-color fonts.
= 0 -> Character addresses 480 to 487 are connected to standard ROM fonts.
= 1 -> Character addresses 480 to 487 are connected to multi-color ROM fonts.

CFONT1 - Enable 2nd 8 multi-color fonts.
= 0 -> Character addresses 488 to 495 are connected to standard ROM fonts.
= 1 -> Character addresses 488 to 495 are connected to multi-color ROM fonts.

CFONT2 - Enable 3rd 8 multi-color fonts.
= 0 -> Character addresses 496 to 503 are connected to standard ROM fonts.
= 1 -> Character addresses 496 to 503 are connected to multi-color ROM fonts.

CFONT3 - Enable 4th 8 multi-color fonts.
= 0 -> Character addresses 504 to 511 are connected to standard ROM fonts.
= 1 -> Character addresses 504 to 511 are connected to multi-color ROM fonts.

The initial value is (0, 0, 0, 0) after power up.

Column 4	B7	b6	b5	b4	b3	b2	b1	b0
	LCD	-	ID5	ID4	ID3	ID2	ID1	ID0

LCD - OSD application selection.
= 1 -> LCD monitor application selected. The 2nd and 3rd pins will be XIN, NC.
= 0 -> CRT monitor application selected. The 2nd and 3rd pins will be VCO, RP.
After this bit is changed, the whole chip circuit will be reset to default value except this byte. So this bit also can work as software reset bit. The initial value is 0 after power up.

ID5-ID0 - LCD bit identify bits. LCD bit can be updated to 1 only when ID5-ID0 = (0, 1, 0, 1, 0, 1). And LCD bit can be updated to 0 only when ID5-ID0 = (1, 0, 1, 0, 1, 0).

Column 5	B7	b6	b5	b4	b3	b2	b1	b0
	VMEN	-	-	-	-	T2	T1	T0

VMEN - Auto sizing video measurement enable bit. All video measurements commence at the following VFLB pulse after the VMEN bit is set, complete the measurement after one vertical frame. This bit will be self-clear after the video measurement of one vertical frame is completed.

T2-T0 - These 3 bits define the trigger level of RIN, GIN, BIN auto-sizing input pins. The initial value is (0, 0, 0) after power up.
= 0, 0, 0 -> 2.00 +/- 0.1 V
= 0, 0, 1 -> 2.15 +/- 0.1 V
= 0, 1, 0 -> 2.30 +/- 0.1 V
= 0, 1, 1 -> 2.45 +/- 0.1 V
= 1, 0, 0 -> 2.60 +/- 0.1 V
= 1, 0, 1 -> 2.75 +/- 0.1 V
= 1, 1, 0 -> 2.90 +/- 0.1 V
= 1, 1, 1 -> 3.00 +/- 0.1 V

Column 6 ~ column 31 : Reserved.

3.13 Auto sizing video measurement

The auto sizing video measurement module monitors horizontal and vertical flyback pulses and their relationship to video content. In horizontal measurement, the HFLB is the reference signal. As PLL clock is the certain multiple of HFLB frequency, the measurements for HFLB and R,G,BIN are all based on the PLL clock. In vertical measurement, the VFLB pulse is reference signal and the HFLB is the counting clock. HFLB and VFLB have an exact timing relationship to the active raster display on the monitor. When the HFLB, VFLB sync signals and the R,G,BIN video signals (taken from the output of pre-amplifier) are compared, it will feedback to MCU a lot of information about the display size and centering. If back porch is much smaller than front porch, then the video information is too much to the left (or up in the vertical direction). If both front porth and back porth percentage of the total display period is too large, then the display size is too small. MCU can change the display size and center until front and back porches are equal and the porches to active video ratio is correct. Please note that due to the deviation of analog circuits, building a ratio table of correct porches to video for different operating frequencies is needed. And it is recommend that video contrast is set to maximum first for the correct capture of video information.
All these measurements commence at the following VFLB pulse after enabling VMEN bit, complete the measurement after one vertical frame, and then FINISH bit will be set to 1 by hardware, so **after FINISH bit is set to 1 or minimum delay 2 vertical frame time after enabling VMEN bit is needed** to read out the measurement data. The horizontal measurement for R,G,BIN will store the minimum start location and the maximum ending location in one vertical frame into registers. All of the input signals for timing measurement are polarity programmable, so the different phase measurement can be obtained.
Note: (HSP, VSP) bits should be filled in the opposite value of the polarity of HFLB and VFLB input when auto sizing function is work.

Auto sizing video measurement data bytes : read only registers

	B7	b6	b5	b4	b3	b2	b1	b0
Byte 0	FINISH	-	-	-	HSTART MSB			

FINISH : = 1 -> The auto sizing video measurement is finished after enabling VMEN bit.
= 0 -> The auto sizing video measurement is not finished.

b3 ~ b0 : The most significant 4 bits of **HSTART** which represents the distance between the first active edge of R,G,BIN input and reference HFLB trailing edge. See Figure 10.

	B7	b6	b5	b4	b3	b2	b1	b0
Byte 1	HSTART LSB							

b7 ~ b0 : The least significant 8 bits of **HSTART** which represents the distance between the first active edge of R,G,BIN input and reference HFLB trailing edge. See Figure 10.

	B7	b6	b5	b4	b3	b2	b1	b0
Byte 2	-	-	-	-	HEND MSB			

b3 ~ b0 : The most significant 4 bits of **HEND** which represents the distance between the last active edge of R,G,BIN input and reference HFLB trailing edge. See Figure 10.

Byte 3	B7	b6	b5	b4	b3	b2	b1	b0
	HEND LSB							

b7 ~ b0 : The least significant 8 bits of **HEND** which represents the distance between the last active edge of R,G,BIN input and reference HFLB trailing edge. See Figure 10.

Byte 4	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	HACTIVE MSB			

b3 ~ b0 : The most significant 4 bits of **HACTIVE** which represents the HFLB dot distance between 2 reference HFLB sync pulse. See Figure 10.

Byte 5	B7	b6	b5	b4	b3	b2	b1	b0
	HACTIVE LSB							

b7 ~ b0 : The least significant 8 bits of **HACTIVE** which represents the HFLB dot distance between 2 reference HFLB sync pulse. See Figure 10.

Byte 6	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	HPULSE MSB			

b3 ~ b0 : The most significant 4 bits of **HPULSE** which represents the HFLB pulse dot distance. See Figure 10.

Byte 7	B7	b6	b5	b4	b3	b2	b1	b0
	HPULSE LSB							

b7 ~ b0 : The least significant 8 bits of **HPULSE** which represents the HFLB pulse dot distance. See Figure 10.

Byte 8	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	VSTART MSB			

b3 ~ b0 : The most significant 4 bits of **VSTART** which represents the H line distance between the first active line of R,G,BIN input and reference VFLB leading edge. See Figure 10.

Byte 9	B7	b6	b5	b4	b3	b2	b1	b0
	VSTART LSB							

b7 ~ b0 : The least significant 8 bits of **VSTART** which represents the H line distance between the first active line of R,G,BIN input and reference VFLB leading edge. See Figure 10.

Byte 10	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	VEND MSB			

b3 ~ b0 : The most significant 4 bits of **VEND** which represents the H line distance between the last active line of R,G,BIN input and reference VFLB leading edge. See Figure 10.

Byte 11	B7	b6	b5	b4	b3	b2	b1	b0
	VEND							LSB

b7 ~ b0 : The least significant 8 bits of **VEND** which represents the H line distance between the last active line of R,G,BIN input and reference VFLB leading edge. See Figure 10.

Byte 12	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	OVER	VACTIVE MSB			

OVER - = 1 -> The line number counter is overflow.
= 0 -> Not overflow.

b3 ~ b0 : The most significant 4 bits of **VACTIVE** which represents the total H line count between two consecutive VFLB pulses. See Figure 10.

Byte 13	B7	b6	b5	b4	b3	b2	b1	b0
	VACTIVE							LSB

b7 ~ b0 : The least significant 8 bits of **VACTIVE** which represents the total H line count between two consecutive VFLB pulses. See Figure 10.

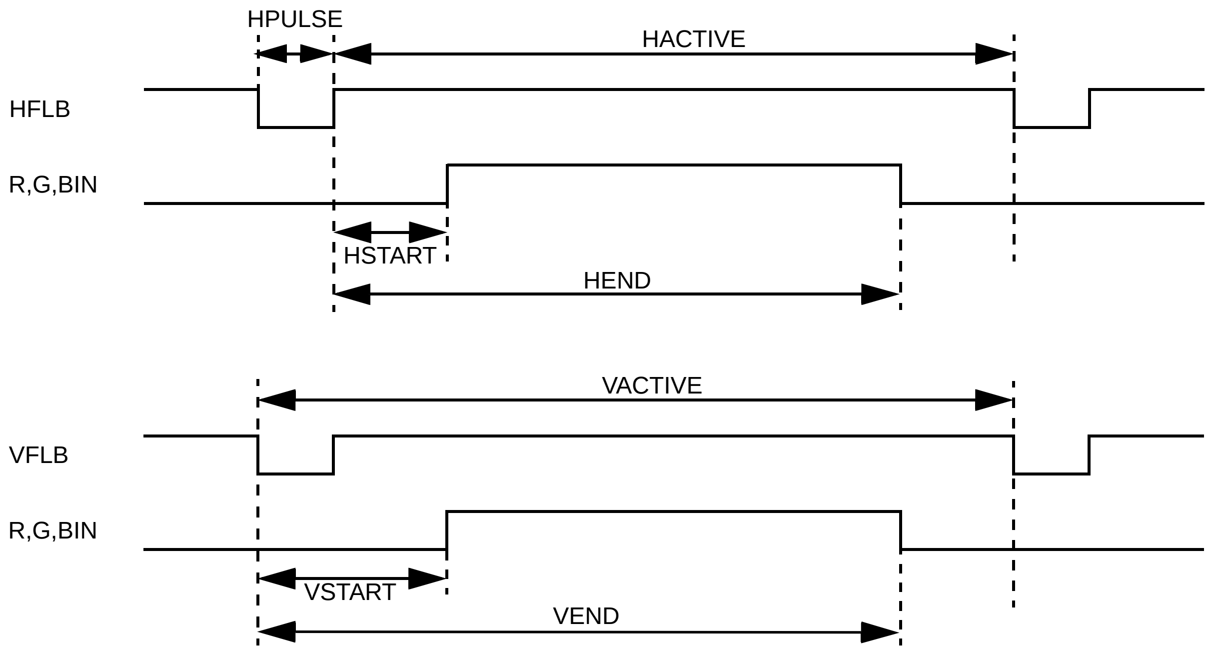


FIGURE 10. Timing Diagram of Auto Sizing Video Measurement

4.0 ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage(VDD,VDDA)	-0.3 to +7 V
Voltage with respect to Ground	-0.3 to VDD+0.3 V
Storage Temperature	-65 to +150 ^{o}C
Ambient Operating Temperature	0 to +70 ^{o}C

5.0 OPERATING CONDITIONS

DC Supply Voltage(VDD,VDDA)	+4.75 to +5.25 V
Operating Temperature	0 to +70 ^{o}C

6.0 ELECTRICAL CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Conditions (Notes)	Min.	Max.	Units
V_{IH}	Input High Voltage (pin hflb, vflb, sda, sck, ssb)	-	0.7 * VDD	VDD+0.3	V
	Input High Voltage (pin rin, gin, bin)	-	TBD	VDD+0.3	V
V_{IL}	Input Low Voltage (pin hflb, vflb, sda, sck)	-	VSS-0.3	0.3 * VDD	V
	Input Low Voltage (pin ssb)	-	VSS-0.3	0.2 * VDD	V
	Input Low Voltage (pin rin, gin, bin)	-	VSS-0.3	TBD	V
V_{OH}	Output High Voltage	I_{OH} > -5 mA	VDD-0.8	-	V
V_{OL}	Output Low Voltage	I_{OL} < 5mA	-	0.5	V
V_{ODH}	Open Drain Output High Voltage	- (For all OD pins, and pulled up by external 5 to 9V power supply)	5	9	V
V_{ODL}	Open Drain Output Low Voltage	5 mA > I_{DOL} (For all OD pins)	-	0.5	V
I_{CC}	Operating Current	Pixel rate=150MHz I_{load} = 0uA	-	25	mA
I_{SB}	Standby Current	Vin = VDD, I_{load} = 0uA	-	12	mA

7.0 SWITCHING CHARACTERISTIC (Under Operating Conditions)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{HFLB}	HFLB input frequency	15	-	150	KHz
f_{VFLB}	VFLB input frequency	-	-	200	Hz
T_r	Output rise time	-	3	-	ns
T_f	Output fall time	-	3	-	ns
t_{BCSU}	SSB to SCK set up time	200	-	-	ns
t_{BCH}	SSB to SCK hold time	100	-	-	ns
t_{DCSU}	SDA to SCK set up time	200	-	-	ns
t_{DCH}	SDA to SCK hold time	100	-	-	ns
t_{SCKH}	SCK high time	500	-	-	ns
t_{SCKL}	SCK low time	500	-	-	ns
$t_{SU:STA}$	START condition setup time	500	-	-	ns
$t_{HD:STA}$	START condition hold time	500	-	-	ns
$t_{SU:STO}$	STOP condition setup time	500	-	-	ns
$t_{HD:STO}$	STOP condition hold time	500	-	-	ns

8.0 TIMING DIAGRAMS

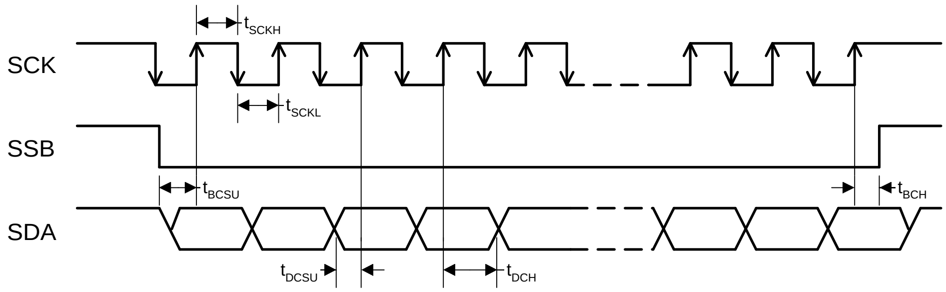


FIGURE 11. Data Interface Timing(SPI)

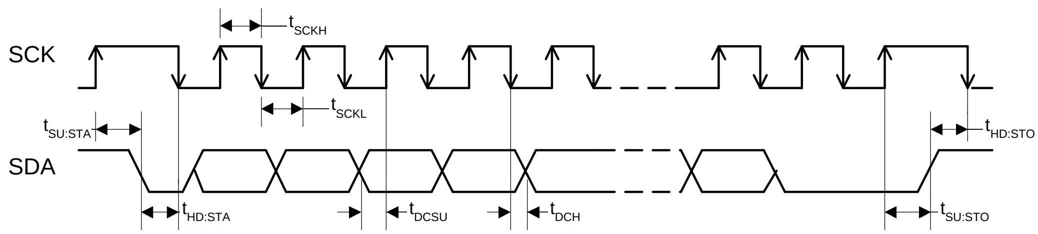


FIGURE 12. Data Interface Timing(I²C)

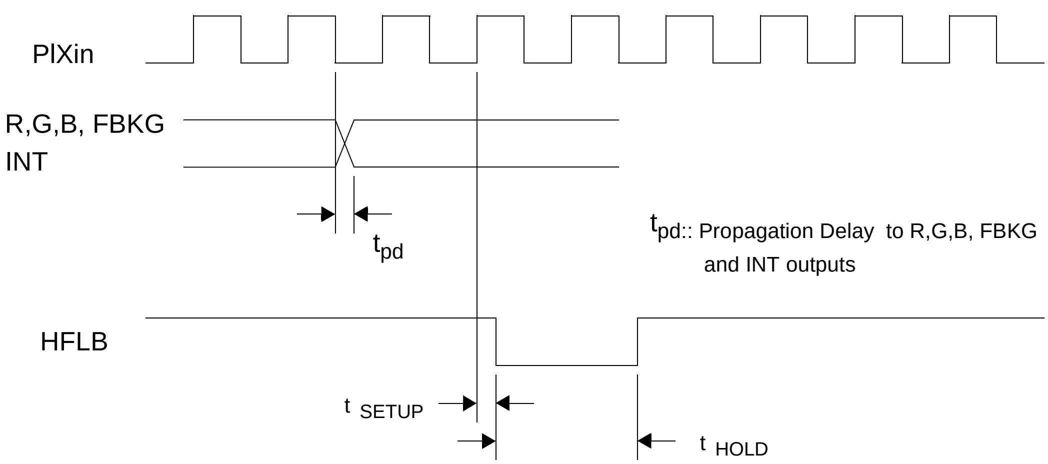
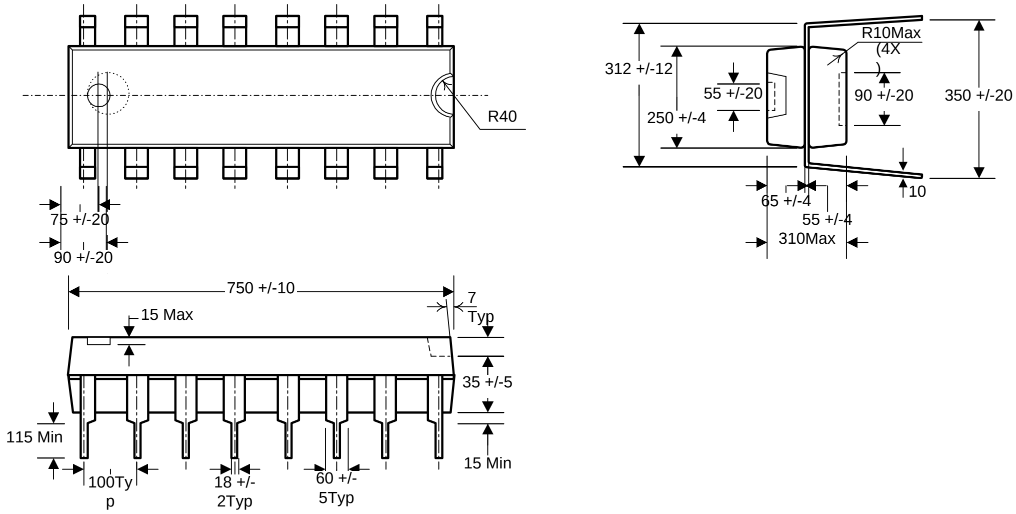


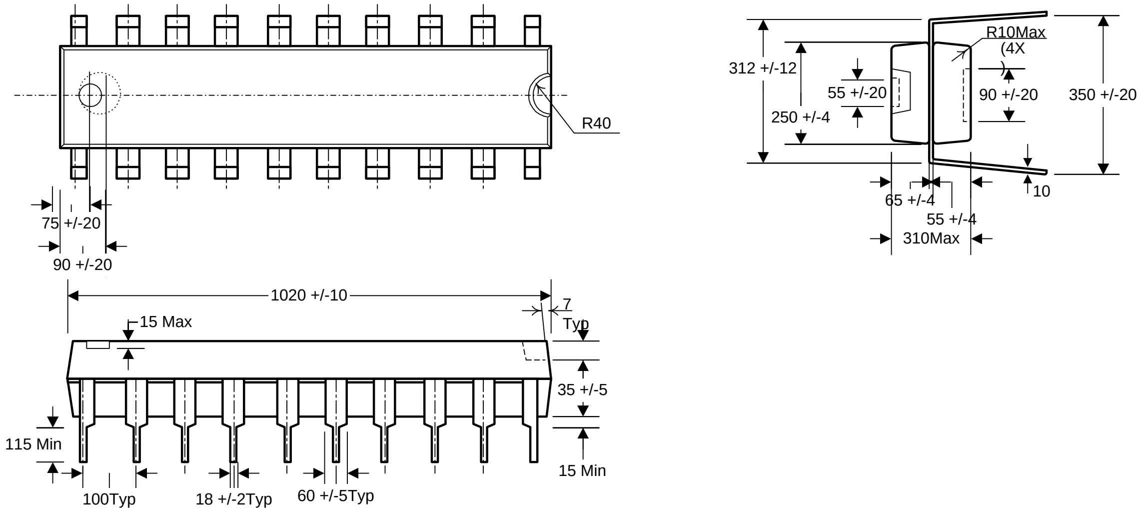
FIGURE 13. Output and HFLB Timing to Pixel Clock

9.0 PACKAGE DIMENSION

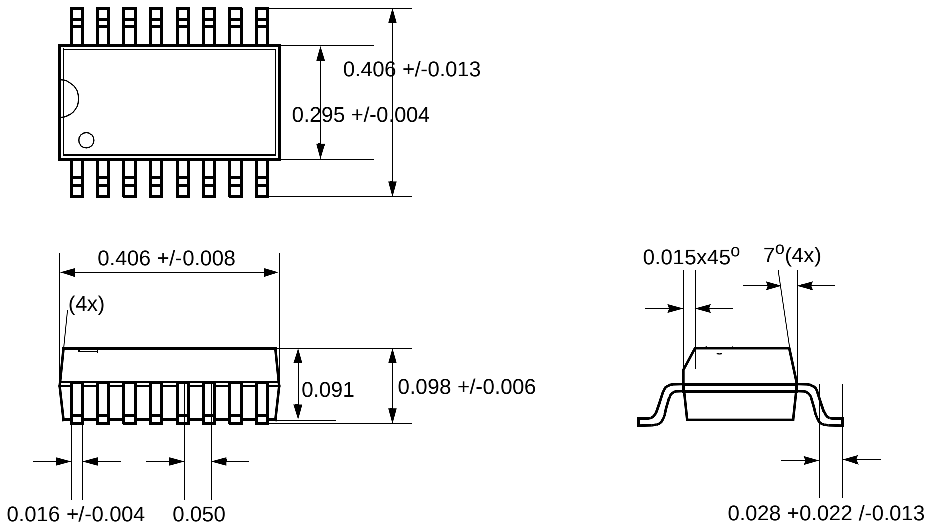
9.1 16 Pin PDIP 300mil



9.2 20 Pin PDIP 300mil



9.3 16 Pin SOP 300mil



9.4 20 Pin SOP 300 mil