# Microprocessor Compatible Monitor Controller

## FEATURES

- Synchronous signal processing for use in green monitor applications.
- Easy command interface for external microprocessor controls.
- D/A converters up to 12V output.
- Built-in self-test pattern generator.
- On-chip clock oscillator allows external TTL level clock signal input.

## GENERAL DESCRIPTION

MTV003 is intended for use in digital-controlled, power-conscious (Green) monitor applications. It integrates 4 major function blocks traditionally implemented in discrete parts and provides an easy interface for microprocessor controls. The functional blocks included in MTV003 are: SYNC processing, D/A converters, self-test pattern generator and command interface.

## BLOCK DIAGRAM

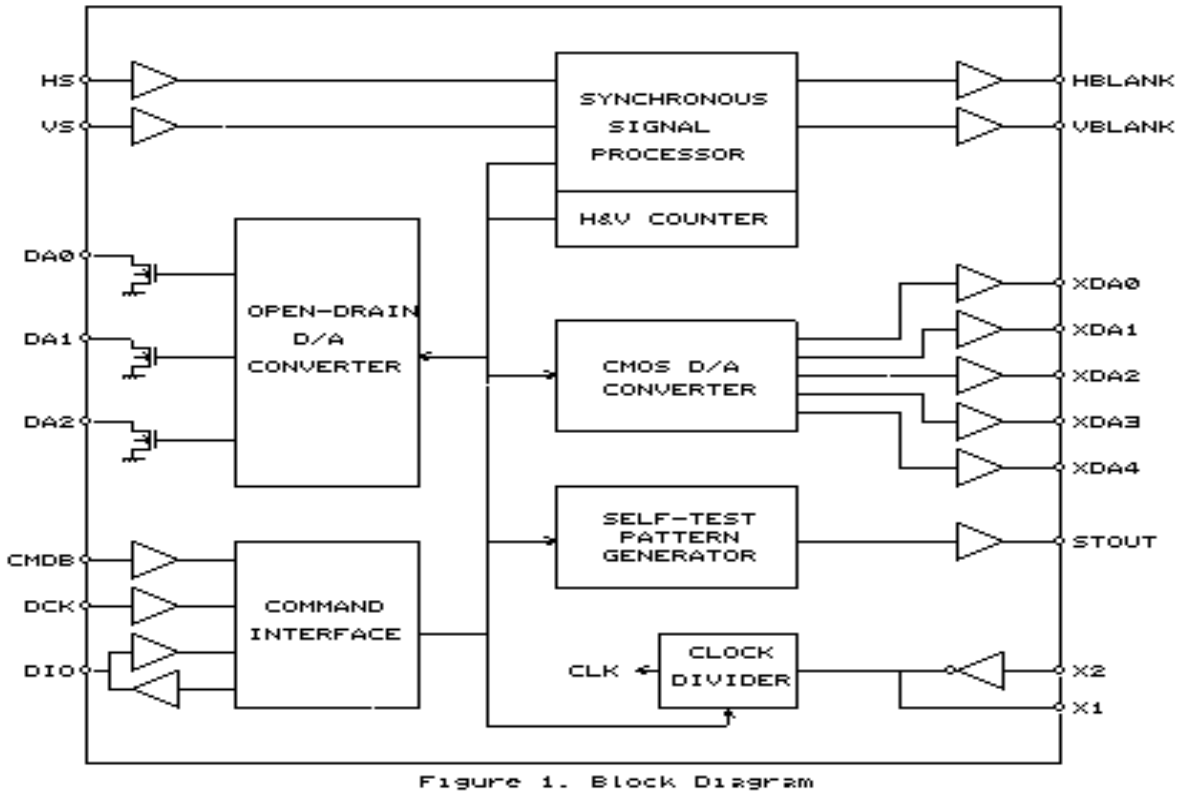
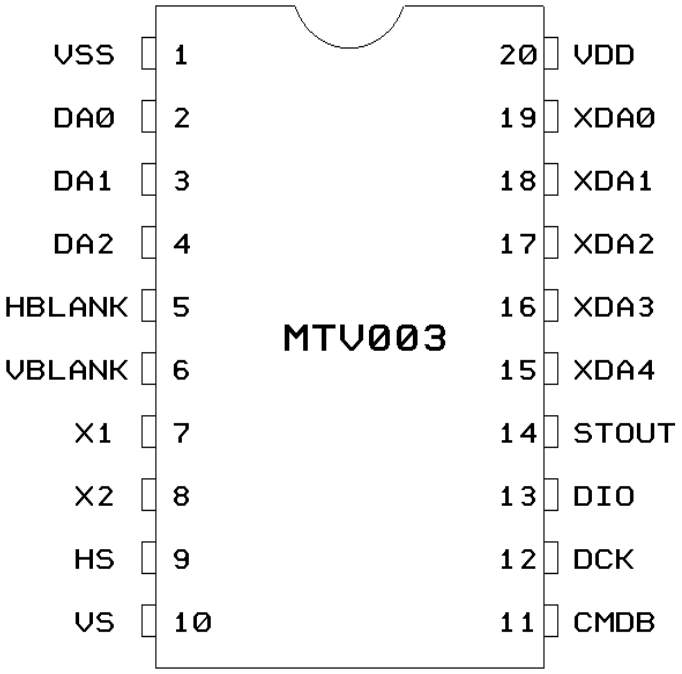



Figure 1. Block Diagram

## 1.0 CONNECTION DIAGRAM

(20 PIN PDIP 300 MIL PACKAGE)




## 2.0 PIN DESCRIPTIONS

| Name | I/O | Pin# | Function |
|---|---|---|---|
| VSS | | 1 | **Ground** (0 V). |
| DA0 | O | 2 | **Open-Drain PWM** (Pulse Width Modulation) **D/A Converter 0**. The output pulse width is programmable by writing data to **Reg10** with 8-bit resolution to control the pulse width duration from 0 to 255/256. The output frequency is 31.25KHz (or15.625KHz). In applications, the external pull-up resistor can be connected to 12V for the desired full-scale output. |
| DA1 | O | 3 | **Open-Drain PWM D/A Converter 1**. **See DA0.** The output pulse width is programmable by **Reg11**. |
| DA2 | O | 4 | **Open-Drain PWM D/A Converter 2**. **See DA0.** The output pulse width is programmable by **Reg12**. |
| HBLANK | O | 5 | **Horizontal Blank**. The pulse width and the delay of HBLANK vs.HS input leading edges are programmable by **Reg7 and Reg6,** respectively. |
| VBLANK | O | 6 | **Vertical Blank**. The output pulse width is programmable by **Reg9**. |
| X1 | I/O | 7 | **Crystal 1**. Used to interface to the oscillator. An 8MHz(or 4MHz) crystal must be connected between this pin and pin X2. An appropriate capacitor to Ground, whose value depends on the specified $C_L$ of the crystal, must be connected. This pin can also be used as a direct input when the external oscillator is used. |

| Name | I/O | Pin# | Function |
|---|---|---|---|
| X2 | O | 8 | **Crystal 2**. **See X1.** An appropriate capacitor to Ground, whose value depends on the specified $C_L$ of the crystal, must be connected. For the external clock source, this pin must be tied to Ground. |
| HS | I | 9 | **Horizontal Sync.** Horizontal synchronous signal input. The input level is TTL compatible with internal 0.2V hysteresis. An internal 50K Ohm pull-up resistor is connected to this pin. |
| VS | I | 10 | **Vertical Sync.** Vertical synchronous signal input. The input level is TTL compatible with internal 0.2V hysteresis. An internal 50K Ohm pull-up resistor is connected to this pin. |
| CMDB | I | 11 | **Command Interface Enabler.** A low active pin which must be forced to low in excess of 16 cycles of DCK for 1 successful access of command interface. It has an internal 50K Ohm pull-up resistor. |
| DCK | I | 12 | **Command Interface Clock.** This pin is used as the timing base for command interface. The address or data portion for the serial in (out) of DIO is recognized by counting the number of DCKs. It has an internal 50K Ohm pull-up resistor. |
| DIO | I/O | 13 | **Command Interface Data.** This pin is a bidirectional pin. A microprocessor can access any internal command registers through the protocol of the address portion followed by the succeeding data portion. It must complete 16 full DCK cycles for a valid access. |
| STOUT | O | 14 | **Self-Test Video Output.** (for self-test mode) This pin is the **video** output pin of the self-test pattern generator. The generator enabler, pattern modes, output band selection and output enabler are programmed by **Reg16**. |
| XDA4 | O | 15 | **CMOS PWM D/A Converter 4. See DA0.** The output pulse width can be programmed by **Reg30**. It is a CMOS type output. |
| XDA3 | O | 16 | **CMOS PWM D/A Converter 3. See DA0.** The output pulse width can be programmed by **Reg29**. It is a CMOS type output. |
| XDA2 | O | 17 | **CMOS PWM D/A Converter 2. See DA0.** The output pulse width can be programmed by **Reg28**. It is a CMOS type output. |
| XDA1 | O | 18 | **CMOS PWM D/A Converter 1. See DA0.** The output pulse width can be programmed by **Reg27**. It is a CMOS type output. |
| XDA0 | O | 19 | **CMOS PWM D/A Converter 0. See DA0.** The output pulse width can be programmed by **Reg26**. It is a CMOS type output. |
| VDD | | 20 | **Positive Power Supply.** +5 volts. 2 decoupling capacitors, 0.1 uF and 100 uF, must be connected to VDD and Ground as close to the device as possible. |

## 3.0 FUNCTIONAL DESCRIPTION

### 3.1 Crystal Oscillator and Clock Generator

The crystal oscillator shall be connected to an 8MHz(or 4MHz) crystal. X1, as shown in Fig.1, can be used as an input source for the external clock or an output clock source to drive the external MCU. All timing specifications are based on the frequency of X1 (or X1 divided by 2).

### 3.2 PWM D/A Converter

There are 2 types of D/A converters with 8-bit resolution: open-drain type (DA0 to DA2) and CMOS type (XDA0 to XDA4). The sampling frequency is 31.25KHz or 15.625KHz, depending on the use of the crystal. The maximum external voltage applied is 12V for the open-drain type, and the output pulse width is programmable

for each converter by setting the corresponding register.

### 3.3 SYNC Processor

The sync processor contains the following functions: polarity detection, presence detection, H-Freq counter, V-Freq counter and sync signal separation for input SYNC sources (HS and VS). It can be programmed to change the detected polarity status and output polarity of SYNC pins (HBLANK and VBLANK) by using the command interface. The timing diagrams of sync processing are shown as Fig. 2 in section 8.0. The internal SYNC signals (Hsync and Vsync) are extracted from different sources according to the following modes of operation.

| | Mode | VS | HS | Comment |
|---|---|---|---|---|
| 1 | Separate(H+V) | present | present | HS = H or H/V sync |
| 2 | Composite(H/V) | not present | present | HS= H/V sync |
| 3 | Suspend | present | not present | - |
| 4 | Off | not present | not present | - |

### 3.4 H-Freq Table

After the "start H-Freq count" command is issued over 10 ms (for 15.7KHz) and HCFF(H-Freq Count Finished Flag) is set **High,** the H-Freq output (HF9 - HF0) is valid. The output value of H-Freq is calculated using the following formula:

output value = $[(1/f_{Hfreq(KHz)})\ x\ 64\ x\ 4000] / 16$

| | H-Freq(KHz) | Output value hexadecimal 11 bits | decimal | Tolerance (%) |
|---|---|---|---|---|
| **1** | 15.7 | 3FB | 1019 | 0.0981354 |
| **2** | 18.7 | 357 | 855 | 0.1169591 |
| **3** | 21.8 | 2DD | 733 | 0.1364256 |
| **4** | 30 | 215 | 533 | 0.1876172 |
| **5** | 31.5 | 1FB | 507 | 0.1972386 |
| **6** | 33.5 | 1DD | 477 | 0.2096436 |
| **7** | 35.5 | 1C2 | 450 | 0.2222222 |
| **8** | 36.8 | 1B2 | 434 | 0.2304147 |
| **9** | 38 | 1A5 | 421 | 0.2375297 |
| **10** | 40 | 190 | 400 | 0.2500000 |
| **11** | 48 | 14D | 333 | 0.3003003 |
| **12** | 50 | 140 | 320 | 0.3125000 |
| **13** | 57 | 118 | 280 | 0.3571428 |
| **14** | 60 | 10A | 266 | 0.3759398 |
| **15** | 64 | 0FA | 250 | 0.4000000 |
| **16** | 100 | 0A0 | 160 | 0.6250000 |

### 3.5 V-Freq Table

After the "start V-Freq count" command is issued over 120 ms (for 50HZ) and VCFF (V-Freq Count Finish Flag) is set **High,** the V-Freq output (VF8 - VF0) is valid. The output value of V-Freq is calculated according to the following formula:

output value = $[(4/f_{Vfreq(Hz)})\ x\ 4000000] / (64 \times 16)$

| | V-Freq(Hz) | Output value hexadecimal 9 bits decimal | | Tolerance (%) |
|---|---|---|---|---|
| 1 | 20 | 30D | 781 | 0.12804 |
| 2 | 56.25 | 115 | 277 | 0.36101 |
| 3 | 59.94 | 104 | 260 | 0.38461 |
| 4 | 60 | 104 | 260 | 0.38461 |
| 5 | 60.32 | 103 | 259 | 0.38610 |
| 6 | 60.53 | 102 | 258 | 0.38759 |
| 7 | 66.67 | 0EA | 234 | 0.42735 |
| 8 | 70.069 | 0DE | 222 | 0.45045 |
| 9 | 70.08 | 0DE | 222 | 0.45045 |
| 10 | 72 | 0D9 | 217 | 0.46082 |
| 11 | 72.378 | 0D7 | 215 | 0.46511 |
| 12 | 72.7 | 0D6 | 214 | 0.46728 |
| 13 | 87 | 0B3 | 179 | 0.55865 |

### 3.6 Command Interface

The command interface contains 3 pins. Each transfer of command is comprised of 16 DCK clock periods. The first 8 DCK clocks are for the address and direction of DIO, and the succeeding 8 DCK clocks are for the data. Each transfer is initiated by setting CMDB **Low**. The CMDB pin must be pulled **High** after data transfer is completed.

- Command Format

B0 - 4 (*ADD4 - 0*) : Address of the registers.
B5 (*W/RB*) : Transfer direction, 1=write, 0=read.
B6 - 7 : Reserved.
B8 - 15 (***DA0 - 7***) : Data input when *W/RB*=1.
(***DA7 - 0***) Data output when *W/RB*=0.

- Register Allocation
a. Read Transfer

| Reg # | Address Portion | | Data Portion | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | ***ADD4-0*** | ***W/RB*** | ***DA7 - 0*** | | | | | | | |
| | **B0 - 4** | **B5** | **B8** | **B9** | **B10** | **B11** | **B12** | **B13** | **B14** | **B15** |
| **Reg0** | 00000 | 0 | $H_{pol}$ | $V_{pol}$ | $HS_{pre}$ | $VS_{pre}$ | $HV_{pre}$ | $H_{sl}$ | $V_{sl}$ | x |
| **Reg1** | 00001 | 0 | x | x | x | x | HCFF | HF10 | HF9 | HF8 |
| **Reg2** | 00010 | 0 | HF7 | HF6 | HF5 | HF4 | HF3 | HF2 | HF1 | HF0 |
| **Reg3** | 00011 | 0 | x | x | x | x | x | x | VCFF | VF8 |
| **Reg4** | 00100 | 0 | VF7 | VF6 | VF5 | VF4 | VF3 | VF2 | VF1 | VF0 |

Table 4

b. Write Transfer

| Reg # | Address Portion | | Data Portion | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | ***ADD4-0*** | ***W/RB*** | ***DA0 - 7*** | | | | | | | |
| | **B0 - 4** | **B5** | **B8** | **B9** | **B10** | **B11** | **B12** | **B13** | **B14** | **B15** |
| **Reg0** | 00000 | 1 | x | x | x | x | x | x | x | x |
| **Reg1** | 00001 | 1 | $V_{pf0}$ | $V_{pf1}$ | $H_{pf0}$ | $H_{pf1}$ | $VB_{pl}$ | $HB_{pl}$ | $HV_{cvs}$ | x |
| **Reg2** | 00010 | 1 | x | x | x | x | x | x | x | x |
| **Reg3** | 00011 | 1 | CLK4M | TEST | x | x | x | x | x | x |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Reg4** | 00100 | 1 | Reserved | | | | | | |
| **Reg5** | 00101 | 1 | Reserved | | | | | | |
| **Reg6** | 00110 | 1 | HBD0 | HBD1 | HBD2 | HBD3 | HBD4 | HBD5 | HBD6 | HBD7 |
| **Reg7** | 00111 | 1 | HBW0 | HBW1 | HBW2 | HBW3 | HBW4 | HBW5 | HBW6 | HBW7 |
| **Reg8** | 01000 | 1 | Reserved | | | | | | |
| **Reg9** | 01001 | 1 | VBW0 | VBW1 | VBW2 | VBW3 | VBW4 | VBW5 | x | VBW7 |
| **Reg10** | 01010 | 1 | $DA0_{b0}$ | $DA0_{b1}$ | $DA0_{b2}$ | $DA0_{b3}$ | $DA0_{b4}$ | $DA0_{b5}$ | $DA0_{b6}$ | $DA0_{b7}$ |
| **Reg11** | 01011 | 1 | $DA1_{b0}$ | $DA1_{b1}$ | $DA1_{b2}$ | $DA1_{b3}$ | $DA1_{b4}$ | $DA1_{b5}$ | $DA1_{b6}$ | $DA1_{b7}$ |
| **Reg12** | 01100 | 1 | $DA2_{b0}$ | $DA2_{b1}$ | $DA2_{b2}$ | $DA2_{b3}$ | $DA2_{b4}$ | $DA2_{b5}$ | $DA2_{b6}$ | $DA2_{b7}$ |
| **Reg13** | 01101 | 1 | Reserved | | | | | | |
| **Reg14** | 01110 | 1 | Reserved | | | | | | |
| **Reg15** | 01111 | 1 | Reserved | | | | | | |
| **Reg16** | 10000 | 1 | STF | RT0 | RT1 | $ST_{bsh}$ | $S_{elft}$ | x | x | x |
| **Reg17** | 10001 | 1 | x | x | x | x | x | x | x | x |
| **Reg18 ~ Reg25** | 10010 ~ 11001 | | Reserved | | | | | | |
| **Reg26** | 11010 | 1 | $XA0_{b0}$ | $XA0_{b1}$ | $XA0_{b2}$ | $XA0_{b3}$ | $XA0_{b4}$ | $XA0_{b5}$ | $XA0_{b6}$ | $XA0_{b7}$ |
| **Reg27** | 11011 | 1 | $XA1_{b0}$ | $XA1_{b1}$ | $XA1_{b2}$ | $XA1_{b3}$ | $XA1_{b4}$ | $XA1_{b5}$ | $XA1_{b6}$ | $XA1_{b7}$ |
| **Reg28** | 11100 | 1 | $XA2_{b0}$ | $XA2_{b1}$ | $XA2_{b2}$ | $XA2_{b3}$ | $XA2_{b4}$ | $XA2_{b5}$ | $XA2_{b6}$ | $XA2_{b7}$ |
| **Reg29** | 11101 | 1 | $XA3_{b0}$ | $XA3_{b1}$ | $XA3_{b2}$ | $XA3_{b3}$ | $XA3_{b4}$ | $XA3_{b5}$ | $XA3_{b6}$ | $XA3_{b7}$ |
| **Reg30** | 11110 | 1 | $XA4_{b0}$ | $XA4_{b1}$ | $XA4_{b2}$ | $XA4_{b3}$ | $XA4_{b4}$ | $XA4_{b5}$ | $XA4_{b5}$ | $XA4_{b7}$ |
| **Reg31** | 11111 | 1 | Reserved | | | | | | |

* The above x may represent any data.

- Command Descriptions

**Reg0** (write) : Begins the H-Freq count. To read the value in the H-Freq registers, the write command (**Reg0)** needs to be issued first.

**Reg0** (read) : The status of polarity, presence and static level for HS and VS.

1. $H_{pol}$, $V_{pol}$ = 1 -> positive, = 0 -> negative.
2. $HS_{pre}$, $VS_{pre}$, HVpre = 1 -> present, = 0 -> not present.
3. $H_{sl}$, $V_{sl}$ = 1 -> high, = 0 -> low.

* HVpre represents the status of the composite (H/V) presence in HS. $H_{sl}$ or $V_{sl}$ is valid only when $HS_{pre}$ or $VS_{pre}$ is not present.

**Reg1** (read) : Hfreq Count Finish flags, Hfreq high bit.

1. HCFF = 1 -> valid, = 0 -> not valid.
2. HF10 - HF8 = 3 high bit of Hfreq.

**Reg1** (write) : Selects the source of VBLANK and controls the polarity status of $H_{pol}$, $V_{pol}$ and SYNC output polarity.

1. $HV_{cvs}$ = 1 -> VBLANK is extracted from HS.
   = 0 -> VBLANK is extracted from VS.
2. $HB_{pl}$ = 1 -> negative HBLANK output, = 0 -> positive HBLANK output.
3. $VB_{pl}$ = 1 -> negative VBLANK output, = 0 -> positive VBLANK output.

* After power-on, $HB_{pl}$ and $VB_{pl}$ shall be initialized to 0.

4. $H_{pf1}$, $H_{pf0}$ = 0,0 or 1,1 -> $H_{pol}$ = x, by auto detection.
   = 0,1 -> force $H_{pol}$ = 1.
   = 1,0 -> force $H_{pol}$ = 0.
5. $V_{pf1}$, $V_{pf0}$ = 0,0 or 1,1 -> $V_{pol}$ = x, by auto detection.

= 0,1 -> force $V_{pol}$ = 1.
= 1,0 -> force $V_{pol}$ = 0.

**Reg 2** (read) : H-Freq low byte.

**Reg 2** (write) : Begins V-Freq count. To read the value in V-Freq registers, the write command (**Reg2)** must be issued first.

**Reg3** (read) : V-Freq Count Finish flag, V-Freq high bit.
1. VCFF = 1 -> valid, = 0 -> not valid.
2. VF8 = the high bit of V-Freq.

**Reg3** (write) : Controls test and clock modes.
1. TEST = 0 -> Normal mode.
= 1 -> **Test mode, not allowed in applications.**
2. CLK4M = 0 -> CLK = X1 divided by 2 (for 8MHz crystal power-on [default]).
= 1 -> CLK = X1 (for 4MHz crystal power-on [default]).

**Reg4** (read) : V-Freq low byte.

**Reg4** (write) : Reserved.

**Reg5** (write) : Reserved.

**Reg6** (write) : Controls the delay of HBLANK output (7 bits).
(HBD7 - 0)
= 10000000 -> Directly bypasses Hsync to output.
= 01000000 -> Min. propagation delay (approximately 300ns).
= 00000000 -> T + 500ns.
= 00000001 -> 2T + 500ns.
= 00111111 -> 64T + 500ns.

**Reg7** (write) : Controls the width of HBLANK output (7 bits).
(HBW7 - 0)
= 10000000 -> Directly bypasses Hsync to output.
= 01000000 -> Min. width (approximately 300ns).
= 00000000 -> T + 500ns.
= 00000001 -> 2T + 500ns.
= 00111111 -> 64T + 500ns.

**Reg8** (write) : Reserved.

**Reg9** (write) : Controls the width of Vblank output (7 bits).
(VBW7 - 0)
= 1-000000 -> Directly bypasses Vsync to output.
= 0-000000 -> Min. width (approximately 8us).
= 0-000001 -> 16 + 8(us).
= 0-111111 -> 16 * 63 + 8(us) = 1.016ms.

**Reg10** (write) : Output pulse width control for DA0.

**Reg11** (write) : Output pulse width control for DA1.

**Reg12** (write) : Output pulse width control for DA2.

**Reg13** (write) : Reserved.

**Reg14** (write) : Reserved.

**Reg15** (write) : Reserved.

**Reg16** (write) : Controls i) enabler, ii) band selection, iii) 4 pattern modes and iv) output enabler for the self-test pattern generator.

| | | |
|---|---|---|
| 1. Selft | = 1 | -> Enables generator. |
| | = 0 | -> Disables generator. |
| 2. STbsh | = 1 | -> 63.5KHz (horizontal) output selected. |
| | = 0 | -> 31.75 KHz (horizontal) output selected. |
| 3. RT1, RT0 | = 0,0 | -> Positive cross-hatch pattern output. |
| | = 0,1 | -> Negative cross-hatch pattern output. |
| | = 1,0 | -> Full white pattern output. |
| | = 1,1 | -> Full black pattern output. |
| 4. STF= 1 | | -> Enables STOUT output. |
| | = 0 | -> Disables STOUT output. |

**Reg17** (write) : Reinitializes all internal registers.

**Reg26** (write) : Output pulse width control for XDA0.

**Reg27** (write) : Output pulse width control for XDA1.

**Reg28** (write) : Output pulse width control for XDA2.

**Reg29** (write) : Output pulse width control for XDA3.

**Reg30** (write) : Output pulse width control for XDA4.

**Reg31** (write) : Reserved.

*1. The above T = 250ns.
2. All D/A converters are centered with a value of ***DA7 - 0***= 10000000, and other registers are initialized with **low** after power-on or a **Reg17** write.
3. The duration of power-on initialization is 200ms and **Reg17** write reinitiation is 2.5ms. No register access is allowed during initialization.

## 4.0 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| DC Supply Voltage (VDD) | -0.3 to 7 V |
| Voltage with respect to Ground: | |
| All pins except VDD and DA0 to DA2 | -0.3 to VDD+ 0.3 V |
| DA0 to DA2 | -0.3 to +13.2 V |
| Storage Temperature | -65 to +150 $^{o}$C |
| Ambient Operating Temperature | 0 to +70 $^{o}$C |

## 5.0 OPERATING CONDITIONS

| | |
|---|---|
| DC Supply Voltage (VDD) | +4.75 V to +5.25 V |
| External D/A Power Supply | +5 V to 12 V |
| Operating Temperature | 0 to +70 $^{o}$C |

## 6.0 ELECTRICAL CHARACTERISTICS (Under Operating Conditions)

| Symbol | Parameter | Conditions (Notes) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | - (for all input pins) | 2.4 | VDD+ 0.3 | V |
| $V_{IL}$ | Input Low Voltage | - (for all input pins) | VSS-0.3 | 0.8 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -500 uA (for pins of HBLANK, VBLANK, DIO, Bout, STOUT, XDA4-0) | 3.0 | - | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 4 mA (see VOH) | - | 0.5 | V |
| $V_{DAOL}$ | Open-Drain D/A Output Low Voltage | IDAOL = 3 mA (for pins of DA2-0) | - | 0.35 | V |
| $V_{DAOH}$ | Open-Drain D/A Output High Voltage | - (for pins of DA2-0, pulled up by external 5 to 12V power supply) | 5 | 12 | V |
| $I_{CC}$ | Maximum Quiescent Supply Current | Vin = VDD, Iout = 0 uA. (all input pins connected to VDD, all output pins without connection) | - | 20 | mA |

## 7.0 SWITCHING CHARACTERISTICS (Under Operating Conditions and X1=8MHz)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{DAO}$ | D/A Converter Output Frequency | - | 31.25 | - | KHz |
| $f_{XTAL}$ | Crystal Frequency | - | 8 | - | MHz |
| $f_{HS}$ | HS Input Frequency | 15 | - | 100 | KHz |
| $f_{VS}$ | VS Input Frequency | 20 | - | 100 | Hz |
| $t_{HIPW}$ | HS Input Pulse Width | 0.5 | - | 6.5 | us |
| $t_{VIPW}$ | VS Input Pulse Width | 25 | - | 2000 | us |
| $t_{HHBD}$ | HSYNC (Rise) to HBLANK Output Delay (programmed by **Reg6**) | 300 | (N+1)xT+500 | 64xT+850 | ns |
| | HSYNC (Rise) to HBLANK Output Delay (bypass HSYNC to HBLANK Output directly) | - | - | 50 | ns |
| $t_{HBW}$ | HBLANK Output Width (programmed by **Reg7**) | 300 | (N+1)xT+500 | 64xT+850 | ns |
| | HBLANK Output Width (bypass HSYNC to HBLANK Output directly) | 0.5 | - | 7 | us |
| $t_{HHBJ}$ | HSYNC to HBLANK Output Jitter | - | - | (+/-) 25 | ns |
| $t_{VBW}$ | VBLANK Output Width (programmed by **Reg9**) | 16 | (Nx16)+8 | 1016 | us |
| | VBLANK Output Width (bypass VSVNC to VBLANK Output directly) | 25 | - | 2000 | us |
| $t_{HVBD}$ | HSYNC to VBLANK Output Delay (H/V mode) | - | 1 H-line | - | - |
| $t_{VVBD}$ | VS to VBLANK Output Delay (H+V mode) | - | - | 50 | ns |
| $t_{VVBJ}$ | VSYNC to VBLANK Output Jitter(H+V mode) | - | - | (+/-) 25 | ns |
| $t_{HVBJ}$ | HSYNC to VBLANK Output Jitter (H/V mode) | - | - | (+/-) 25 | ns |
| $t_{CDSU}$ | CMDB to DCK Setup Time | 200 | - | - | ns |
| $t_{CDH}$ | CMDB to DCK Hold Time | 100 | - | - | ns |
| $t_{DDSU}$ | DIO to DCK Setup Time (write) | 200 | - | - | ns |
| $t_{DDH}$ | DIO to DCK Hold Time(write) | 100 | - | - | ns |
| $t_{DCKH}$ | DCK High Time | 200 | - | - | ns |
| $t_{DCKL}$ | DCK Low Time | 200 | - | - | ns |
| $T_{DDD}$ | DCK to DIO Delay Time(read) | 100 | - | - | ns |

* 1. The above HSYNC is extracted from HS input and VSYNC is extracted from VS, HS input.
* 2. T = 250ns (1/4MHz) is fixed regardless of whether or not an 8(or 4)MHz crystal is used.
* 3. $0 \leq N \leq 63$

## 8.0 TIMING DIAGRAMS

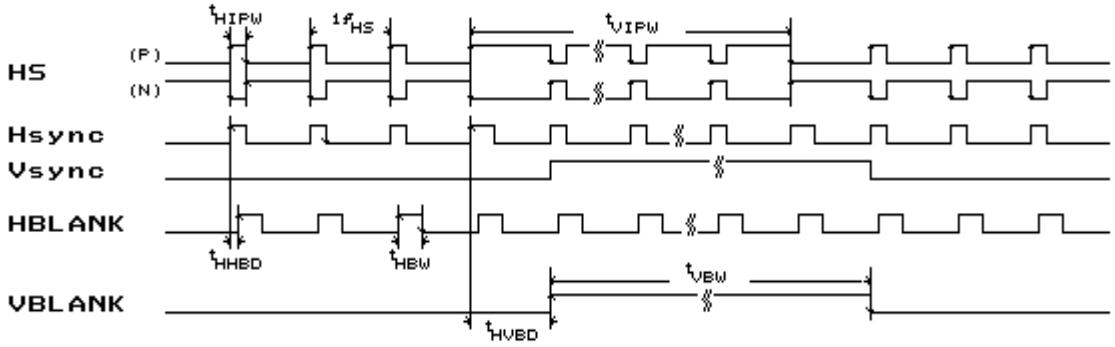



Figure 2. H/V Mode Timing

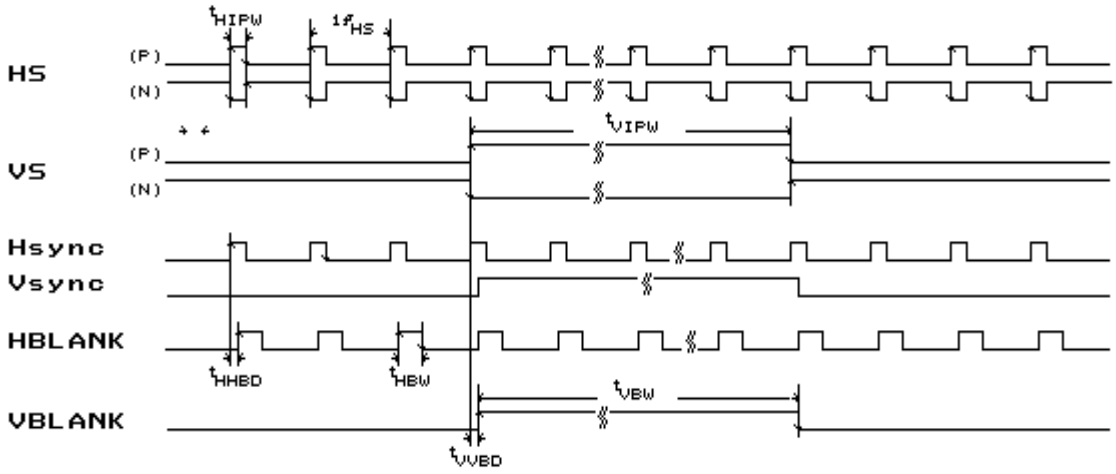



Figure 3. H+V Mode Timing

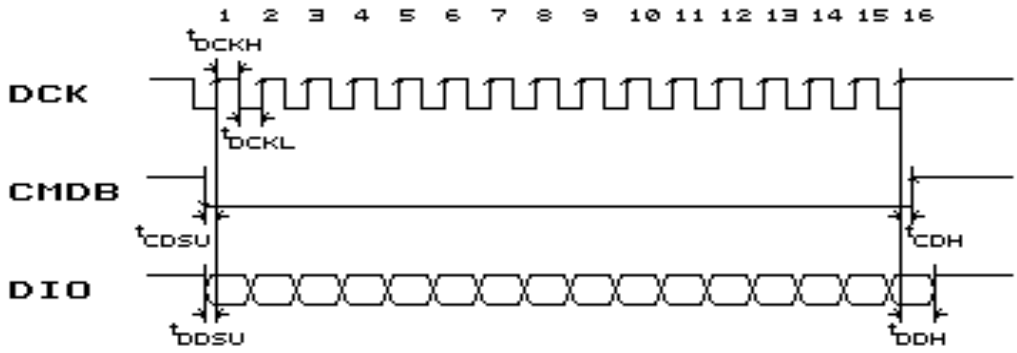



Figure 4. Command Interface Write Timing.

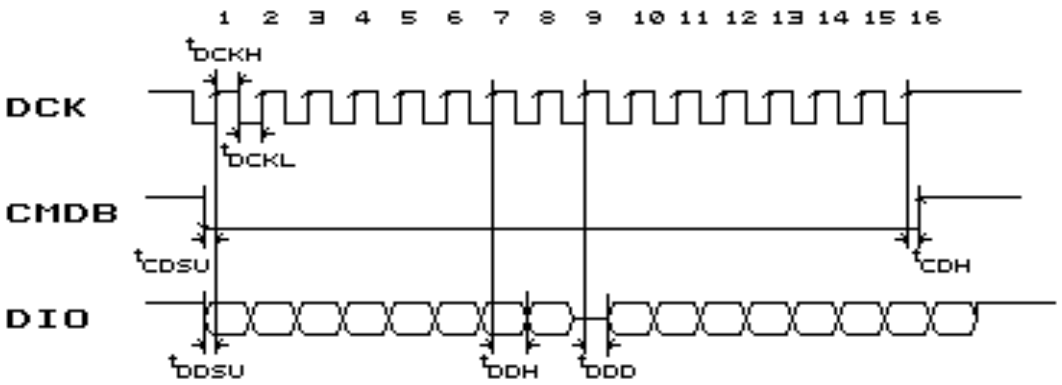



Figure 5. Command Interface Read Timing.

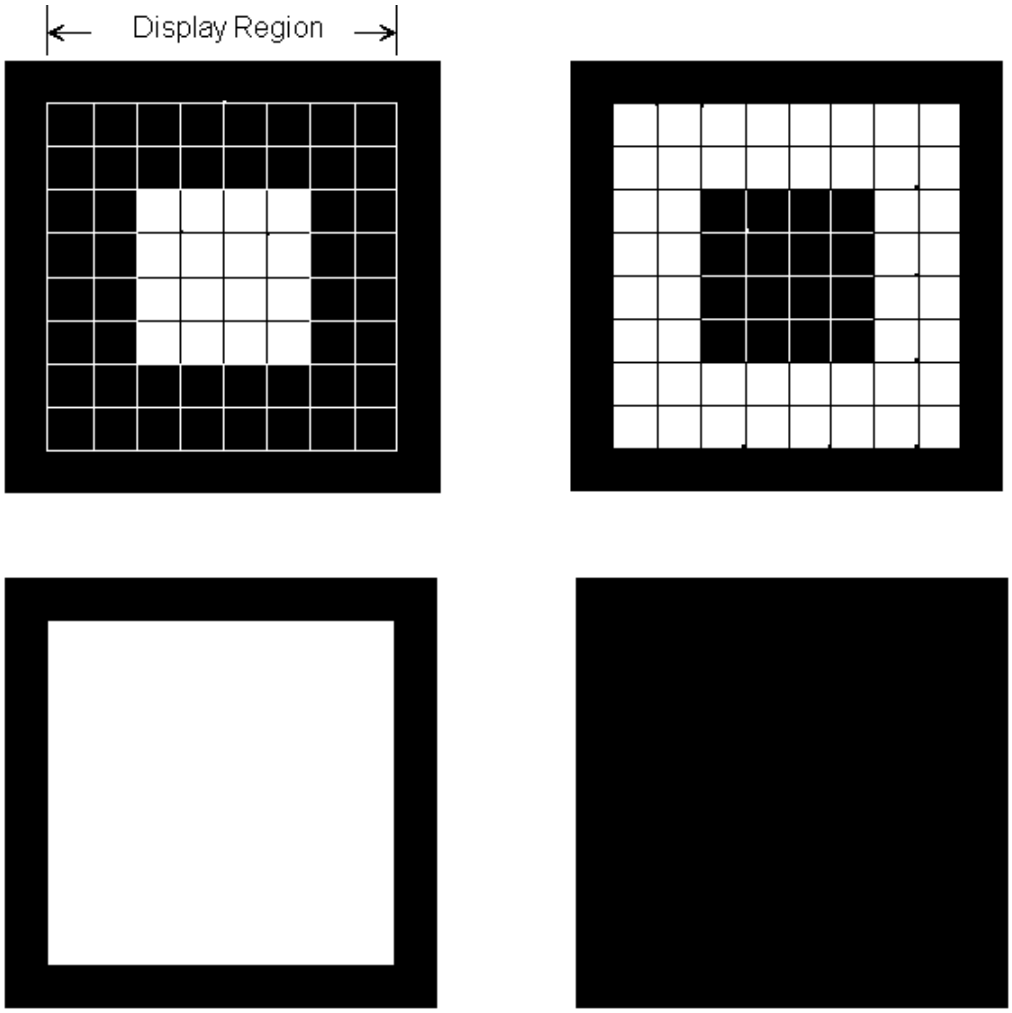
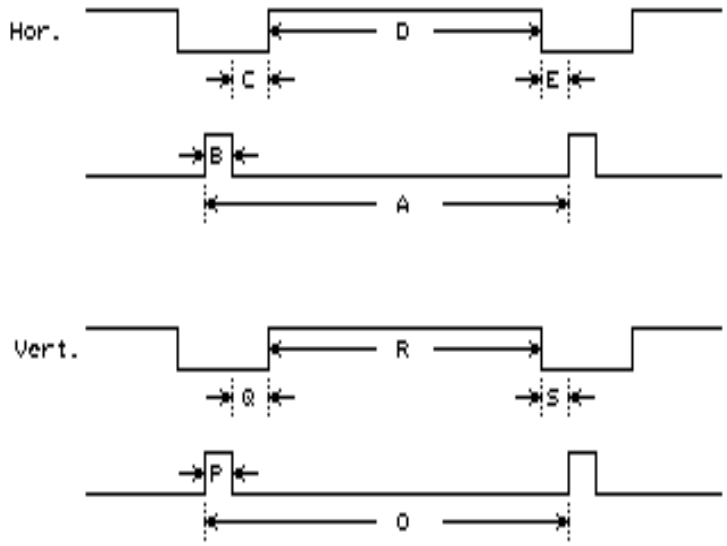



Figure 6. 4 Self-Test Patterns

MTV003 SELF TEST PATTERN TIMING.




| | | A) 63.5KHz, 60Hz | | B) 31.75KHz, 60Hz | |
|---|---|---|---|---|---|
| | | (Absolute time) | (H dots) | (Absolute time) | (H dots) |
| 1. | Hor. total time | us(A)=15.75 | 1280 | us(A)=31.5 | 640 |
| 2. | Hor. active time | us(D)=12.05 | 979.3 | us(D)=24.05 | 488.6 |
| 3. | Hor. F.P. | us(E)=0.2 | 16.25 | us(E)=0.45 | 9 |
| 4. | SYNC pulse width | us(B)=1.5 | 122 | us(B)=3 | 61 |
| 5. | Hor. B.P. | us(C)=2 | 162.54 | us(C)=4 | 81.27 |
| | | | (V lines) | | (V lines) |
| 6. | Vert. total time | ms(O)=16.6635 | 1024 | ms(O)=16.6635 | 480 |
| 7. | Vert. active time | ms(R)=15.6555 | 962 | ms(R)=15.6555 | 451 |
| 8. | Vert. F.P. | ms(S)=0.063 | 3.87 | ms(S)=0.063 | 1.82 |
| 9. | SYNC pulse width | ms(P)=0.063 | 3.87 | ms(P)=0.063 | 1.82 |
| 10. | Vert. B.P. | ms(Q)=0.882 | 54.2 | ms(Q)=0.882 | 25.4 |

* 8 x 8 blocks of cross hatch pattern in display region.

Figure 7. Self-Test Timing