

NL7SB384

Product Preview 1-Bit MiniGate™ Bus Switch

The ON Semiconductor NL7SB384 is a 1-bit MiniGate Bus Switch in ultra-small footprint. The device is TTL compatible when operating between 4.0 and 5.0 Volts. The device exhibits extremely low R_{ON} and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

Features

- $R_{ON} < 4 \Omega$ Typical
- Less Than 0.25 ns - Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL Compatible
- Ultra-Small Packages
- These are Pb-Free Devices

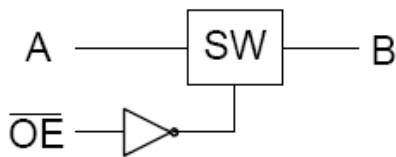


Figure 1. Logic Diagram

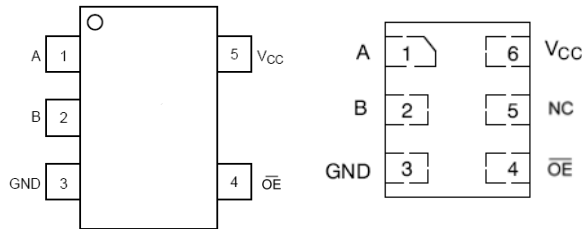


Figure 2. Pinout (Topview)

Pin Descriptions

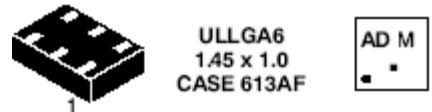
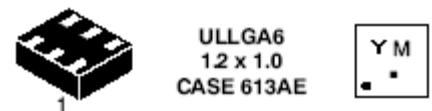
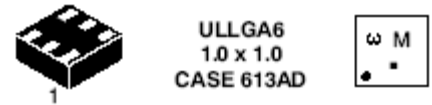
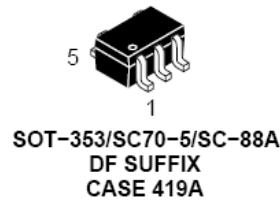
Pin Name	Description
A	Bus A
B	Bus B
\overline{OE}	Bus Switch Enable
NC	No Connect

Truth Table



ON Semiconductor®

<http://onsemi.com>



AD, Y, 3 = Specific Device Code
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimension section.

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Input \overline{OE}	Function
L	B = A
H	Disconnect

Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	Control Pin Input Voltage	-0.5 to +7.0	V
I_{IK}	DC Input Diode Current $V_{IN} < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_{OUT} < GND$	-50	mA
I_O	DC Output Sink Current	128	mA
I_{CC}	DC Supply Current Per Supply Pin	±100	mA
I_{GND}	DC Ground Current per Ground Pin	±100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	150	°C
θ_{JA}	Thermal Resistance	uLLGA6L	TBD
		SC70-5/SC88A-5(Note 1)	350
		TSOP5	200
P_D	Power Dissipation in Still Air at 85 °C	uLLGA6L	TBD
		SC70-5/SC88A-5(Note 1)	150
		TSOP5	200
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
V_{ESD}	ESD Withstand Voltage	Human Body Mode (Note 2)	TBD
		Machine Mode (Note3)	TBD
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 85 °C (Note4)	±500	mA

Stresses exceeding "Maximum Ratings" may damage the device. "Maximum Ratings" are stress ratings only. Functional operation above "Recommended Operating Conditions" is not implied. Extended exposure to stresses above "Recommended Operating Conditions" may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA/ JESD22-A114-A
3. Tested to EIA/ JESD22-A115-A
4. Tested to EIA / JESD78.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.0	5.5	V
V_I	Control Pin Input Voltage (Note 5)	0	5.5	V
V_O	Output Voltage (High or Low State)	0	5.5	V
T_A	Operating Free-Air Temperature	-55	+125	°C
$\Delta t / \Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 5.0 V \pm 0.5 V$	0	100	nS/V

5. Control input may not be left open, it must be tied to high or low logic input voltage level.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = -55°C to +125°C		Unit
				Min	Typ*	Max	Min	Max	
V _{IK}	Clamp Diode Resistance	I _{IN} = -18 mA	4.5					-1.2	V
V _{IH}	High-Level Control Input Voltage		4.0 to 5.5				2.0		V
V _{IL}	Low-Level Control Input Voltage		4.0 to 5.5					0.8	V
R _{ON}	Switch ON Resistance (Note 6)	V _I = 0, I _I = 64 mA I _I = 30 mA	4.5		4 4			7 7	Ω
		V _I = 2.4, I _I = 15 mA	4.5		8		15		
		V _I = 2.4, I _I = 15 mA	4.0		11		20		
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ V _{CC}	5.5					±1.0	μA
I _{OZ}	Off-State Leakage Current	0 ≤ A, B ≤ V _{CC}	5.5					±1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OUT} = 0	5.5					±1.0	μA
ΔI _{CC}	Increase in Supply Current of Control Pin	V _{IN} = 3.4 V	5.5					±1.0	mA

*Typical values are at V_{CC} = 5.0 V and T_A = 25 °C

6. Measured by the voltage drop between A and B pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics (See Figure 3, 4, 5)

Symbol	Parameter	Test Condition	T _A = -55°C to +125°C, C _L = 50 pF, R _U = R _D = 500 Ω				Unit
			V _{CC} = 4.5 - 5.5 V		V _{CC} = 4.0 V		
			Min	Max	Min	Max	
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus (Note 7)	V _I = OPEN		0.25		0.25	ns
t _{PZH} , t _{PZL}	Output Enable Time, \overline{OE} to Bus A, B	V _I = 7 V for t _{PZL} V _I = OPEN for t _{PZH}	1.0	5.2		5.7	ns
t _{PHZ} , t _{PLZ}	Output Disable Time, \overline{OE} to Bus A, B	V _I = 7 V for t _{PLZ} V _I = OPEN for t _{PHZ}	1.0	5.2		5.5	ns

7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

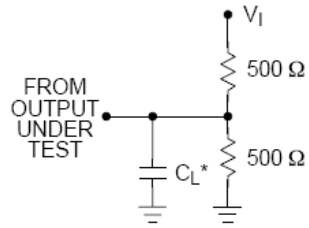
CAPACITANCE (Note 8)

Symbol	Parameter	Conditions	Typ	Max	Unit
C _{IN}	Control Pin Input Capacitance	V _{CC} = 5.0 V	3		pF
C _{IO}	A Port I/O Capacitance	V _{CC} , \overline{OE} = 5.0 V	7		pF
C _{IO}	B Port I/O Capacitance	V _{CC} , \overline{OE} = 5.0 V	5		pF

8. T_A = +25 °C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms

AC Loading and Waveforms



NOTES:

1. Input driven by 50 Ω source terminated in 50 Ω.
 2. C_L includes load and stray capacitance.
- * $C_L = 50$ pF

Figure 3. AC Test Circuit

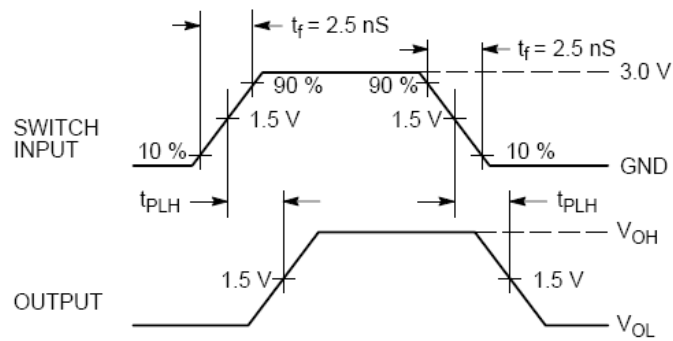


Figure 4. Propagation Delays

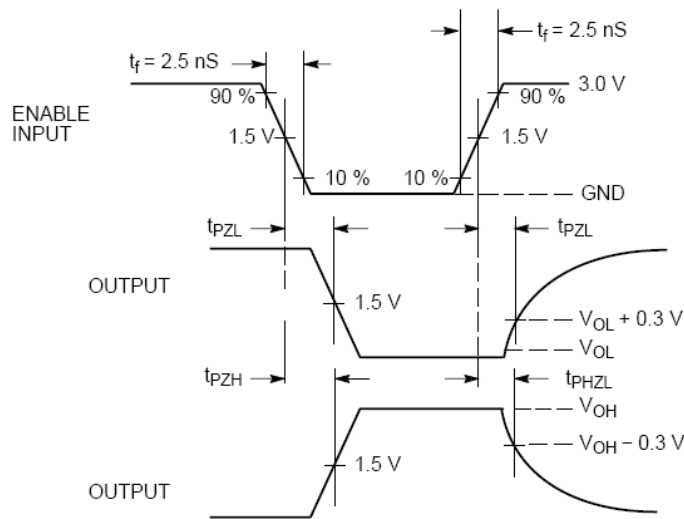


Figure 5. Enable/Disable Delays

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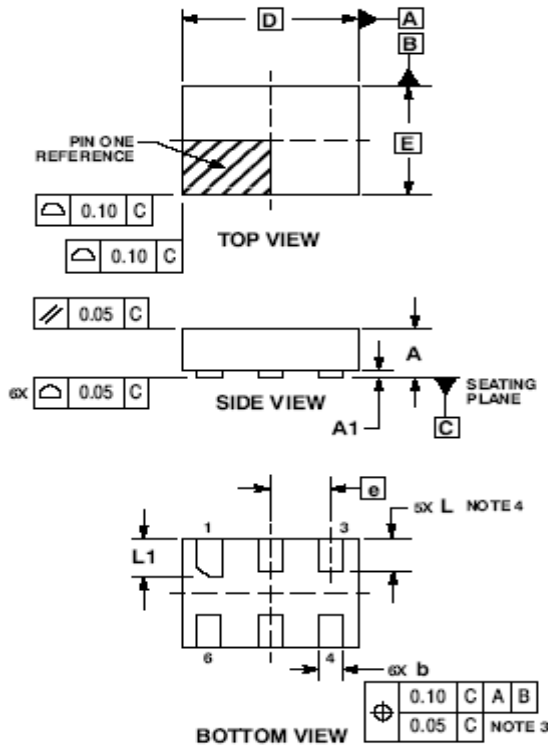
Ordering Information

Device	Package	Shipping[†]
NL7SB384AMX1TCG	ULLGA6 – 0.5 mm Pitch	3000 / Tape & Reel
NL7SB384BMX1TCG	ULLGA6 – 0.4 mm Pitch	3000 / Tape & Reel
NL7SB384CMX1TCG	ULLGA6 – 0.35 mm Pitch	3000 / Tape & Reel
NL7SB384DFT2G	SC88A (5L)	3000 / Tape & Reel
NL7SB384DTT1G	TSOP 5L	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

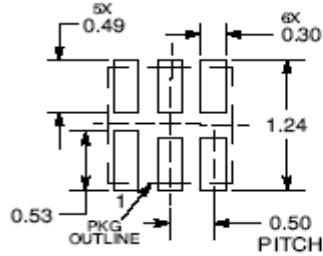
ULLGA6 1.45x1.0, 0.5P
CASE 613AF-01
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
 4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT
SOLDERMASK DEFINED*

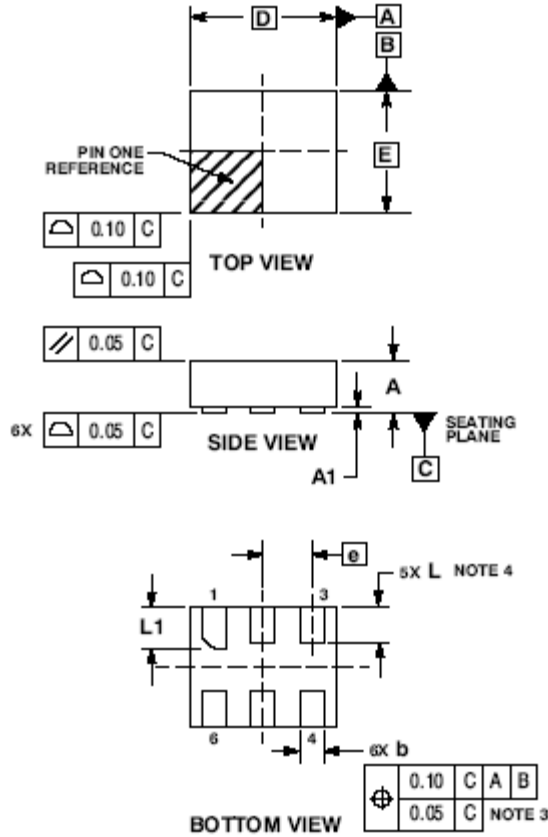


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

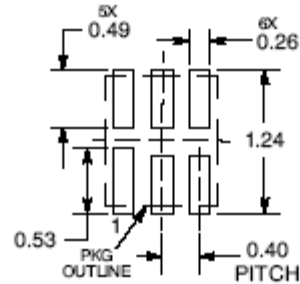
ULLGA6 1.2x1.0, 0.4P
CASE 613AE-01
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
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 4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.35	0.45

MOUNTING FOOTPRINT
SOLDERMASK DEFINED*

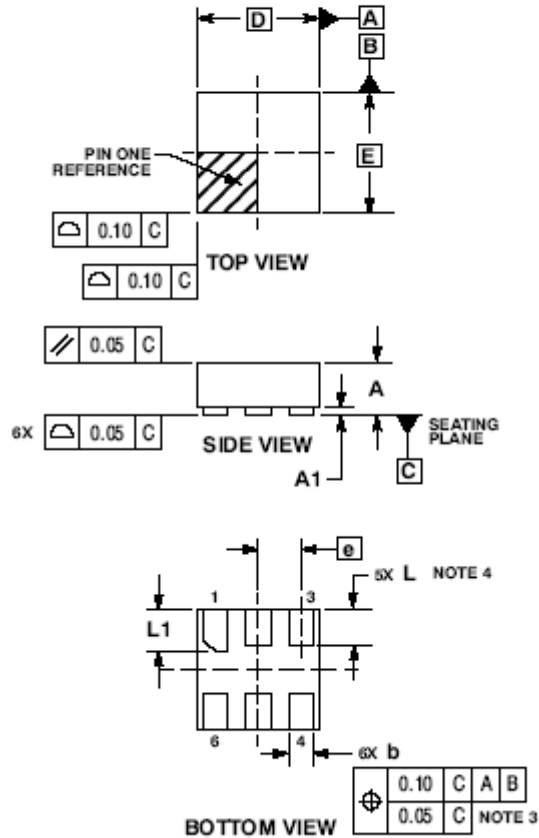


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

ULLGA6 1.0x1.0, 0.35P
CASE 613AD-01
ISSUE A

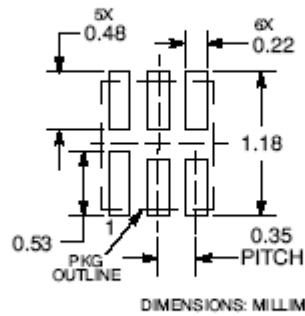


NOTES:

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4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

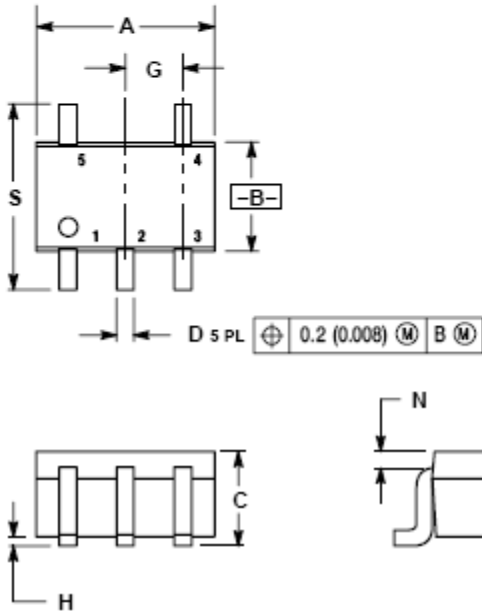
MOUNTING FOOTPRINT
SOLDEMASK DEFINED*



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PACKAGE DIMENSIONS

SC-88A/SOT-353/SC-70
DF SUFFIX
5 LEAD PACKAGE
CASE 419A-02
ISSUE J

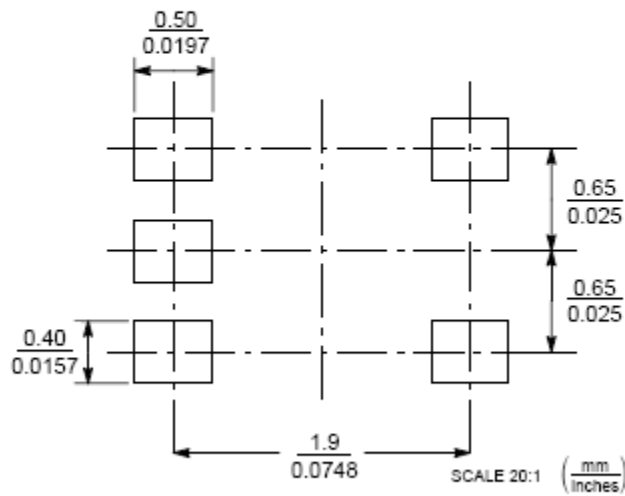


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

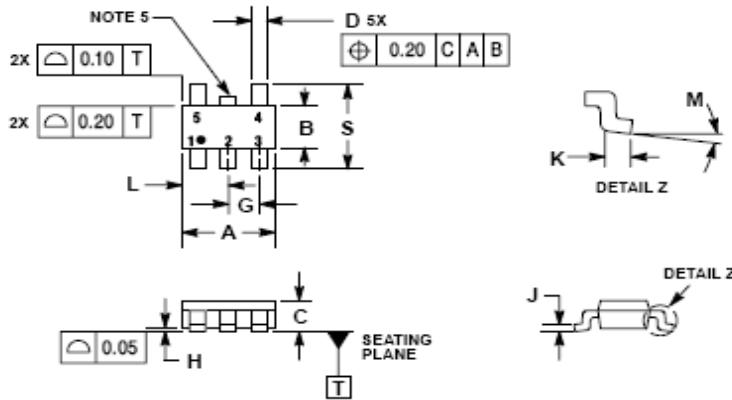
SOLDERING FOOTPRINT*



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PACKAGE DIMENSIONS

TSOP-5
CASE 483-02
ISSUE F

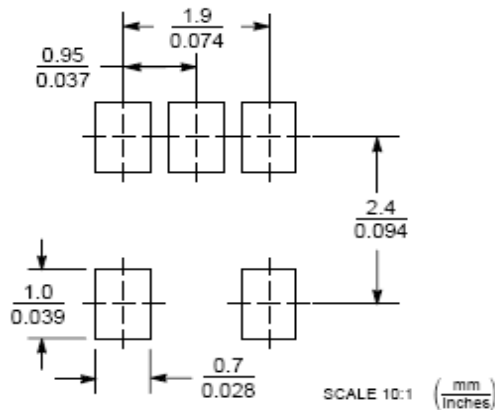


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

MILLIMETERS		
DIM	MIN	MAX
A	3.00	BSC
B	1.50	BSC
C	0.90	1.10
D	0.25	0.50
G	0.95	BSC
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0°	10°
S	2.50	3.00

SOLDERING FOOTPRINT*



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