



Wireless Components

3-Band TV Tuner IC

TUA6030, TUA6032 Version 2.1

Specification July 2001

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|---|---------------------------------|---|
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| Page (in previous Version) | Page (in current Version) | Subjects (major changes since last revision) |
| all | all | Version to V1.1, status to preliminary |
| Product Info | Product Info | Ordering code added. |
| 4-2 | 4-2 | Div. components changed. |
| 4-3 | 4-3 | Div. components changed. |
| 5-2 | 5-2 | Junction temperature and storage temperature +125 °C max. |
| 5-5 | 5-5 | Bus inputs SCL, SDA: $V_{IH} = 2.3 V$. |
| 5-8,5-9, 5-10 | 5-8,5-9, 5-10 | Input conductance, input capacitance corrected. |
| 5-10 | 5-10 | Phase noise @ ± 1 kHz frequency offset deleted. Phase noise, LOW band oscillator: $\Phi_{OSC} = 92$ dBc/Hz min @ ± 10 kHz. Phase noise, MID band oscillator: $\Phi_{OSC} = 92$ dBc/Hz min @ ± 10 kHz. |
| 5-11 | 5-11 | Phase noise @ ± 1 kHz frequency offset deleted. Phase noise, HIGH band oscillator: $\Phi_{OSC} = 87$ dBc/Hz min. |
| 5-14 | 5-14 | Table 5-5, Description of Symbols: CP and OS 'default' added |
| 5-15 | 5-15 | Table 5-5, Test Modes: Normal operation 'default' added. |
| 5-14 | 5-14 | Table 5-5, Description of Symbols: CP and OS 'default' added. |
| 5-15 | 5-15 | Table 5-5, Test Modes: Normal operation 'default' added. |
| 5-16 | 5-16 | Table 5-10, A to D converter levels, footnote 'No erratic codes in the transition' added, Table 5-1, Defaults at power-on reset, Auxiliary byte, bit5 = 1. |
| 5-18, 5-19, 5-20 | 5-18, 5-19, 5-20 | Smith charts added.. |
| div | div | Tbf's replaced . |
| Revision History: Current Version: Data Sheet, V2.0, March 2001 | | |
| Previous Version: Preliminary Data Sheet, V1.1, August 2000 | | |
| all | all | Version to V2.0, preliminary deleted |
| 3-3 | 3-3 | LOW-/MID Oscillator: DC levels corrected |
| 4-2, 4-3 | 4-2, 4-3 | Application circuits modified |
| 5-2 | 5-2 | New definition of thermal properties. |
| 5-6 | 5-6, 5-7 | Saturation Voltages for P0, 2, 3 added |
| 5-11 | 5-11 | AGC take-over point: Min/max values added. Mixer output impedance: Values added |

| | | |
|---|------------|--|
| Revision History: Current Version: Preliminary Data Sheet, V1.1, August 2000 | | |
| 5-11, 5-12 | 5-11, 5-12 | Phase noise corrected |
| 5-16 | 5-16 | Table 5-1, Defaults at power-on reset, Auxiliary byte, bit5 = 1. |
| 5-18 | 5-18 | More telegram examples |
| Revision History: Current Version: Data Sheet, V2.1, July 2001 | | |
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| all | all | Mirror imaged version TUA6032 added |

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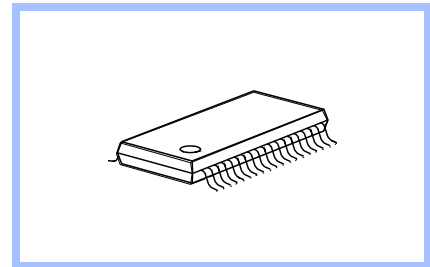
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Product Info

General Description The TUA6030, TUA6032 devices combine a mixer-oscillator block with a digitally programmable phase locked loop (PLL) for use in TV and VCR tuners.

Package



Features General

- Suitable for PAL/NTSC and Digital Video Broadcasting
- Wideband AGC detector for internal tuner AGC
 - 5 programmable take-over points
 - 2 programmable time constants
- Full ESD protection

Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band
- Low impedance mixer input (common base) for MID band
- Low impedance mixer input (common base) for HIGH band
- 2 pin oscillator for LOW band
- 2 pin oscillator for MID band
- 4 pin oscillator for HIGH band

IF-Amplifier

- IF preamplifier with symmetrical 75 Ω output impedance able to drive a SAW filter (500 Ω //40 pF)

PLL

- 4 independent I²C addresses
- I²C bus protocol compatible with 3.3 V and 5V micro-controllers up to 400 kHz
- Short lock-in time
- High voltage VCO tuning output
- 4 PNP ports
- 3 NPN ports
- 1 NPN port/ADC input
- Internal LOW/MID/HIGH band switch
- Lock-in flag
- Programmable reference divider ratio (24, 64, 80, 128)
- Programmable charge pump current

Application

- The IC is suitable for PAL and NTSC tuners in TV- and VCR-sets or set-top receivers for analog TV and Digital Video Broadcasting.
- The AGC stage makes the tuner AGC independent of the Video-IF AGC.

Ordering Information

| Type | Ordering Code | Package |
|---------|------------------------------|------------|
| TUA6030 | Q67037-A1146 (tape and reel) | P-TSSOP-38 |
| TUA6032 | Q67037-Axxxx (tape and reel) | P-TSSOP-38 |

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2 Product Description

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2.1 Overview

The **TUA6030, TUA6032** devices combine a mixer-oscillator block with a digitally programmable phase locked loop (PLL) for use in TV and VCR tuners.

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, an IF amplifier, a reference voltage, and a band switch.

The PLL block with four independently selectable chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1024 MHz in increments of 31.25, 50, 62.5 or 166.7 kHz. The tuning process is controlled by a microprocessor via an I²C bus. The device has 8 output ports, one of them (P6) can also be used as ADC input port. A flag is set when the loop is locked. The lock flag can be read by the processor via the I²C bus.

2.2 Features

General

- Suitable for PAL/NTSC and **Digital Video Broadcasting**
- Wideband AGC detector for internal tuner AGC
 - 5 programmable take-over points
 - 2 programmable time constants
- Full ESD protection

Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band
- Low impedance mixer input (common base) for MID band
- Low impedance mixer input (common base) for HIGH band
- 2 pin oscillator for LOW band
- 2 pin oscillator for MID band
- 4 pin oscillator for HIGH band

IF-Amplifier

- IF preamplifier with symmetrical 75 Ω output impedance able to drive a SAW filter (500 Ω //40 pF)

PLL

- 4 independent I²C addresses
- I²C bus protocol compatible with 3.3 V and 5V micro-controllers up to 400 kHz

- Short lock-in time
- High voltage VCO tuning output
- 4 PNP ports
- 3 NPN ports
- 1 NPN port/ADC input
- Internal LOW/MID/HIGH band switch
- Lock-in flag
- Programmable reference divider ratio (24, 64, 80, 128)
- Programmable charge pump current

2.3 Application

- The IC is suitable for PAL and NTSC tuners in TV- and VCR-sets or cable set-top receivers for analog TV and **D**igital **V**ideo **B**roadcasting.
- The AGC stage makes the tuner AGC independent of the Video-IF AGC.

Recommended band limits in MHz:

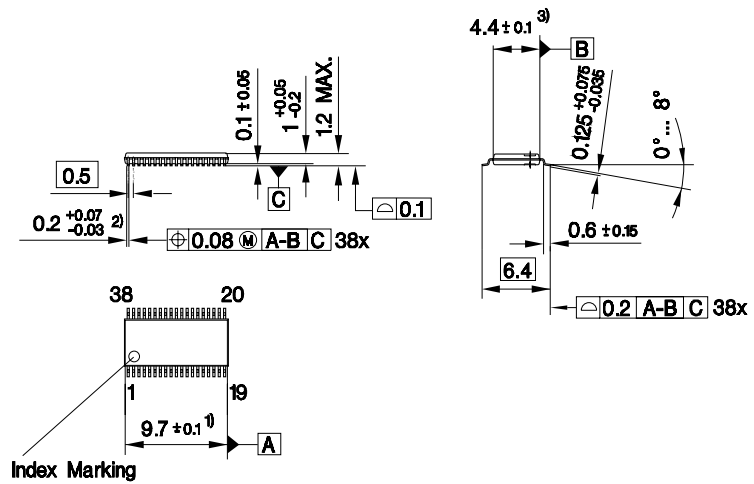
| Table 2-1 NTSC tuners | | | | |
|-----------------------|----------|--------|------------|-----|
| Band | RF input | | Oscillator | |
| | min | max | min | max |
| LOW | 55.25 | 127.25 | 101 | 173 |
| MID | 133.25 | 361.25 | 179 | 407 |
| HIGH | 367.25 | 801.25 | 413 | 847 |

| Table 2-2 PAL tuners | | | | |
|----------------------|----------|--------|------------|--------|
| Band | RF input | | Oscillator | |
| | min | max | min | max |
| LOW | 44.25 | 154.25 | 83.15 | 193.15 |
| MID | 161.25 | 439.25 | 200.15 | 478.15 |
| HIGH | 447.25 | 863.25 | 486.15 | 902.15 |

Note: Tuning margin of ± 3 MHz not included.

2.4 Package Outlines

P-TSSOP-38



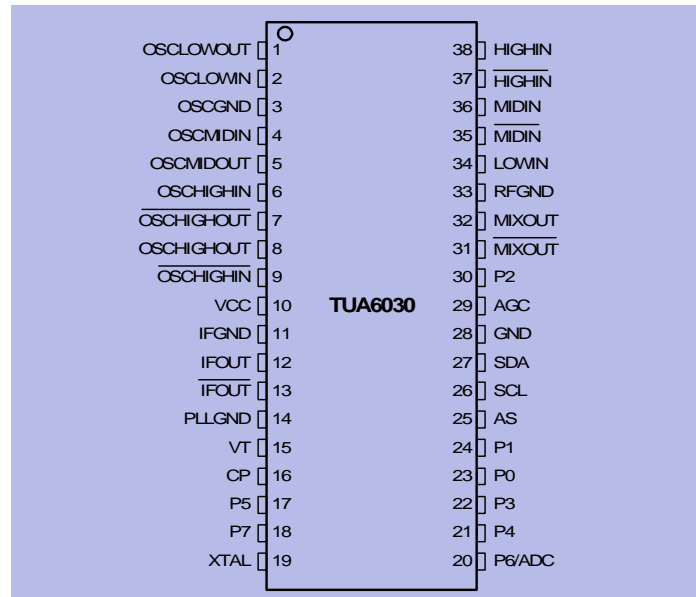
- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion of 0.08 max. per side
- 3) Does not include plastic or metal protrusion of 0.25 max. per side

3 Functional Description

Contents of this Chapter

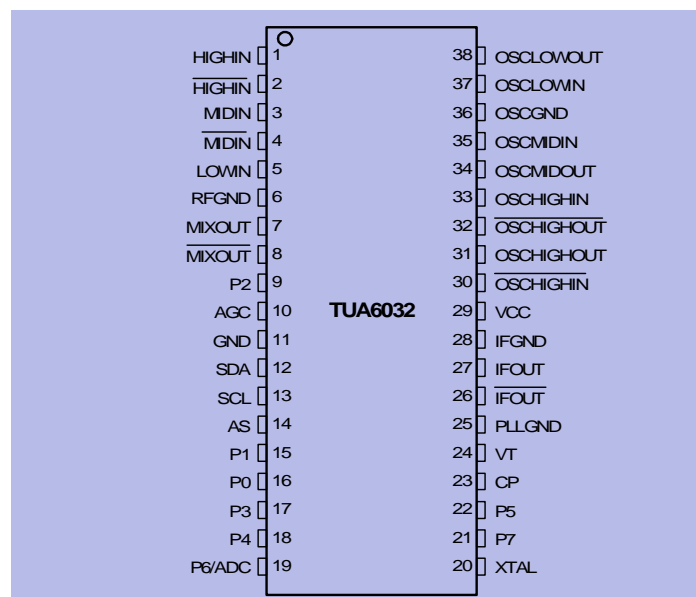
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3.1 Pin Configuration



TUA6030 Pin_config

Figure 3-1 Pin Configuration TUA6030

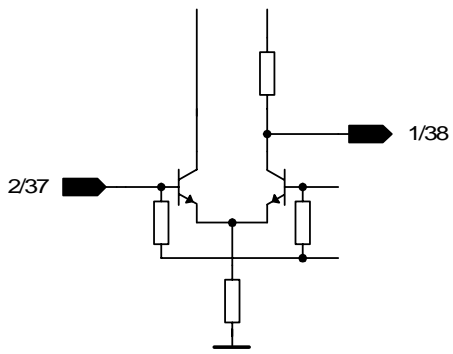
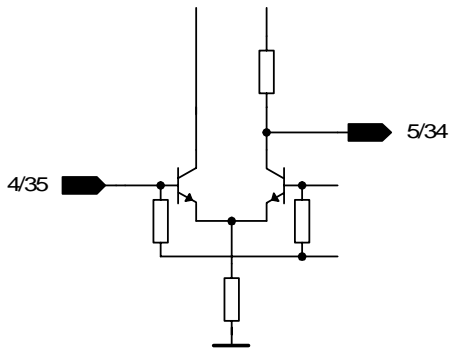


TUA6032 Pin_config

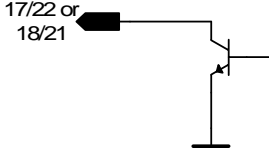

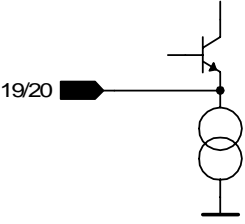
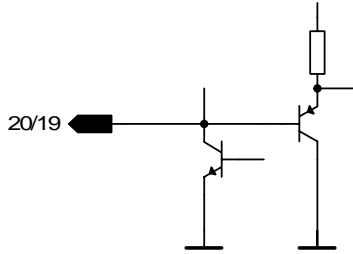
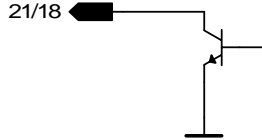



Figure 3-2 Pin Configuration TUA6032

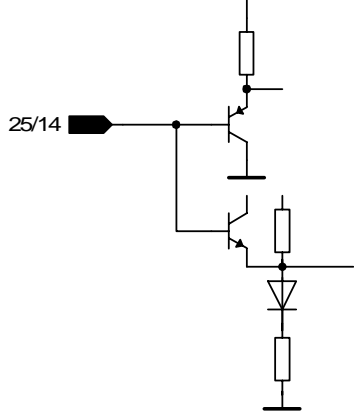
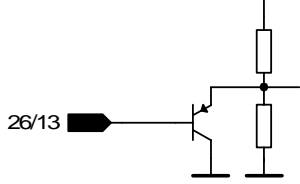
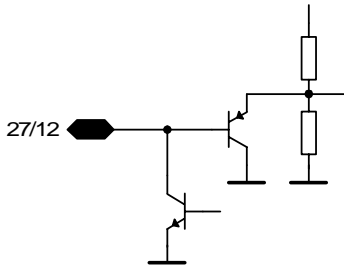
3.2 Pin Definition and Function

Remark: First pin number refers to TUA6030, second to TUA6032

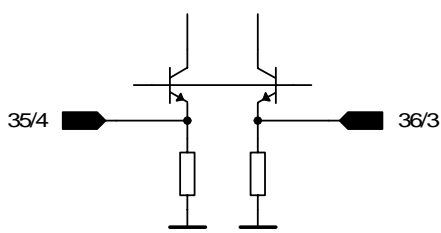
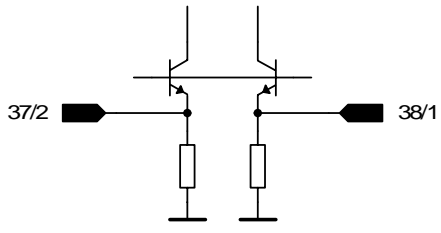
| Table 3-1 Pin Definition and Function | | | | | |
|---------------------------------------|-----------|--|--------------------|-------|-------|
| Pin No. | Symbol | Equivalent I/O-Schematic | Average DC voltage | | |
| | | | LOW | MID | HIGH |
| 1/38 | OSCLOWOUT |  | 2.2 V | | |
| 2/37 | OSCLOWIN | | 1.5 V | | |
| 3/36 | OSCGND | oscillator ground | 0.0 V | 0.0 V | 0.0 V |
| 4/35 | OSCMIDIN |  | | 1.5 V | |
| 5/34 | OSCMIDOUT | | 2.2 V | | |

| Table 3-1 Pin Definition and Function (continued) | | | | | |
|---|-------------------------------|--------------------------|--------------------|-------|-------|
| Pin No. | Symbol | Equivalent I/O-Schematic | Average DC voltage | | |
| | | | LOW | MID | HIGH |
| 6/33 | OSCHIGHIN | | | | 1.8 V |
| 7/32 | $\overline{\text{OSCHIGOUT}}$ | | | | 2.2 V |
| 8/31 | OSCHIGOUT | | | | 2.2 V |
| 9/30 | $\overline{\text{OSCHIGHIN}}$ | | | | 1.8 V |
| 10/29 | VCC | supply voltage | 5.0 V | 5.0 V | 5.0 V |
| 11/28 | IFGND | IF ground | 0.0 V | 0.0 V | 0.0 V |
| 12/27 | IFOUT | | 2.1 V | 2.1 V | 2.1 V |
| 13/26 | $\overline{\text{IFOUT}}$ | | 2.1 V | 2.1 V | 2.1 V |
| 14/25 | PLLGND | PLL ground | 0.0 V | 0.0 V | 0.0 V |
| 15/24 | VT | | VT | VT | VT |
| 16/23 | CP | | 1.9 V | 1.9 V | 1.9 V |

| Table 3-1 Pin Definition and Function (continued) | | | | | |
|---|--------|---|--------------------|-------------------|--------------------------|
| Pin No. | Symbol | Equivalent I/O-Schematic | Average DC voltage | | |
| | | | LOW | MID | HIGH |
| 17/22 | P5 |  | 5 V or V_{CE} | 5 V or V_{CE} | 5 V or V_{CE} |
| 18/21 | P7 |  | 5 V or V_{CE} | 5 V or V_{CE} | 5 V or V_{CE} |
| 19/20 | XTAL |  | 3.3 V | 3.3 V | 3.3 V |
| 20/19 | P6/ADC |  | 5 V or V_{CE} | 5 V or V_{CE} | 5 V or V_{CE} |
| 21/18 | P4 |  | 5 V or V_{CE} | 5 V or V_{CE} | 5 V or V_{CE} |
| 22/17 | P3 |  | n.a. | n.a. | 0 V or $V_{CC} - V_{CE}$ |
| 23/16 | P0 |  | $V_{CC} - V_{CE}$ | n.a. | n.a. |
| 24/15 | P1 |  | n.a. | $V_{CC} - V_{CE}$ | n.a. |

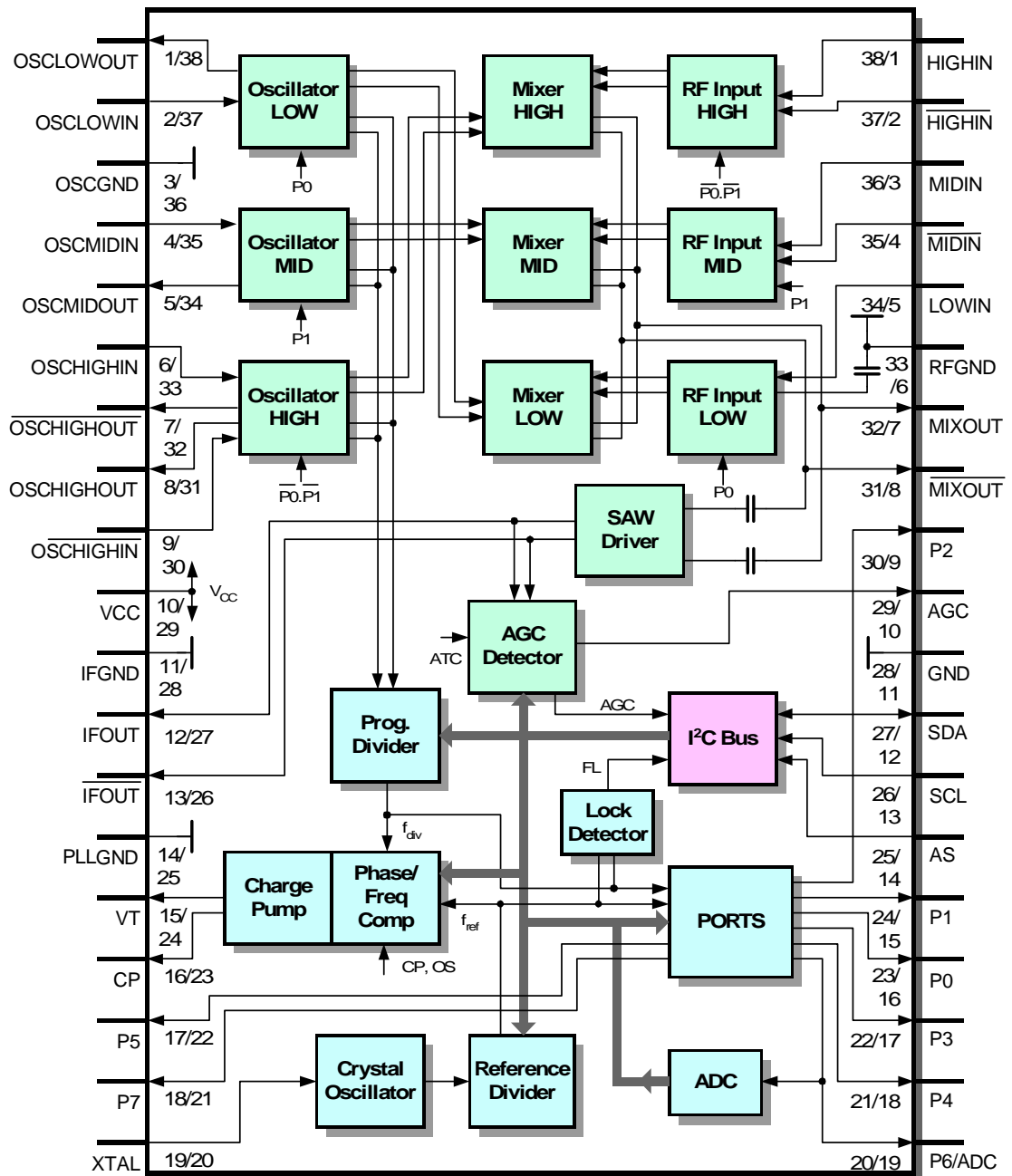
| Table 3-1 Pin Definition and Function (continued) | | | | | |
|---|--------|---|--------------------|----------|----------|
| Pin No. | Symbol | Equivalent I/O-Schematic | Average DC voltage | | |
| | | | LOW | MID | HIGH |
| 25/14 | AS |  | V_{AS} | V_{AS} | V_{AS} |
| 26/13 | SCL |  | n.a. | n.a. | n.a. |
| 27/12 | SDA |  | n.a. | n.a. | n.a. |
| 28/11 | GND | ground | 0.0 | 0.0 | 0.0 |

| Table 3-1 Pin Definition and Function (continued) | | | | | |
|---|--------|--------------------------|--------------------|-------|--------------------------|
| Pin No. | Symbol | Equivalent I/O-Schematic | Average DC voltage | | |
| | | | LOW | MID | HIGH |
| 29/10 | AGC | | 3.0 V | 3.0 V | 3.0 V |
| 30/9 | P2 | | n.a. | n.a. | 0 V or $V_{CC} - V_{CE}$ |
| 31/8 | MIXOUT | | 4.0 V | 4.0 V | 4.0 V |
| 32/7 | MIXOUT | | 4.0 V | 4.0 V | 4.0 V |
| 33/6 | RFGND | IF ground | 0.0 V | 0.0 V | 0.0 V |
| 34/5 | LOWIN | | 1.9 V | | |

| Table 3-1 Pin Definition and Function (continued) | | | | | |
|---|----------------------------|---|--------------------|--------|--------|
| Pin No. | Symbol | Equivalent I/O-Schematic | Average DC voltage | | |
| | | | LOW | MID | HIGH |
| 35/4 | $\overline{\text{MIDIN}}$ |  | | 0.75 V | |
| 36/3 | MIDIN | | | 0.75 V | |
| 37/2 | $\overline{\text{HIGHIN}}$ |  | | | 0.75 V |
| 38/1 | HIGHIN | | | | 0.75 V |

3.3 Block Diagram

Remark: First pin number refers to TUA6030, second to TUA6032



TUA6030_1 BlockDiag

Figure 3-3 Block Diagram

3.4 Circuit Description

3.4.1 Mixer-Oscillator block

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, an IF amplifier, a reference voltage, and a band switch.

Filters between tuner input and IC separate the TV frequency signals into three bands. The band switching in the tuner front-end is done by using three PNP port outputs. In the selected band the signal passes a tuner input stage with a MOSFET amplifier, a double-tuned bandpass filter and is then fed to the mixer input of the IC which has in case of LOW band a high-impedance input and in case of MID or HIGH band a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency which is filtered out at the balanced mixer output pair by means of a parallel tuned circuit. The following IF amplifier is capacitively coupled to the mixer outputs and has a low output impedance to drive the SAW filter directly.

3.4.2 PLL block

The oscillator signal is internally DC-coupled as a differential signal to the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio $N = 256$ through 32767 and is then compared in a digital frequency/phase detector with a reference frequency $f_{ref} = 31.25, 50, 62.5$ or 166.7 kHz. This frequency is derived from an unbalanced, low-impedance 4 MHz crystal oscillator (pin XTAL) divided by 128, 80, 64 or 24. The reference frequencies will be different with a quartz other than 4 MHz.

The phase detector has two outputs which drive two current sources of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source pulses for the duration of the phase difference. In the reverse case the negative current source pulses. If the two signals are in phase, the charge pump output (CP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pull-up resistor at VT and external RC circuitry). The charge pump output is also switched into the high-impedance state if the control bits T2, T1, T0 = 0, 1, 0. Here it should be noted, however, that the tuning voltage can alter over a long period in the high impedance state as a result of self discharge in the peripheral circuitry. VT may be switched off by the control bit OS to allow external adjustments.

If the VCO is not oscillating the PLL locks to a tuning voltage of 33V (V_{TH}).

By means of control bit CP the pump current can be switched between two values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software controlled ports P0 to P7 are general purpose open-collector outputs. The test bits T2, T1, T0 = 1, 0, 0 switch the test signals f_{div} (divided input signal) and f_{ref} (i.e. 4 MHz / 64) to P4 and P5 respectively.

The lock detector resets the lock flag FL if the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, if $FL = 1$, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P * (K_{VCO} / f_{XTAL}) * (C1+C2) / (C1*C2)$$

where I_P is the charge pump current, K_{VCO} the VCO gain, f_{xtal} the crystal oscillator frequency and C_1, C_2 the capacitances in the loop filter (Chapter 4). As the charge pump pulses at i.e. 62.5 kHz (= f_{ref}), it takes a maximum of 16 μ s for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore it takes between 128 and 144 μ s for FL to be set after the loop regains lock.

3.4.3 AGC

The wide-band AGC stage detects the level of the IF output signal and generates an AGC voltage for gain control of the tuner input transistors. The AGC take-over and the time constant are selectable by the I²C bus.

3.4.4 I²C-Bus Interface

Data is exchanged between the processor and the PLL via the I²C bus. The clock is generated by the processor (input SCL). Pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have a hysteresis and a low-pass characteristic, which enhance the noise immunity of the I²C bus.

The data from the processor pass through an I²C bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are high). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes low, while SCL remains high. Stop condition: SDA goes high while

SCL remains high. All further information transfer takes place during SCL = low, and the data is forwarded to the control logic on the positive clock edge.

The table 'Bit Allocation' ([see Table 5-4 Bit Allocation Read / Write on page 39](#)) should be referred to for the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to low (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (address select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte. Appropriate setting of the test bits will decide whether the band-switch byte or the auxiliary byte will be transmitted ([see Table 5-7 Test modes on page 40](#)).

If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists of three bits from the A/D converter, the lock flag and the power-on flag.

Four different chip addresses can be set by an appropriate DC level at pin AS ([see Table 5-6 Address selection on page 40](#)).

While the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA line to low, which would block the bus. The power-on reset flag POR is set at power-on and if V_{CC} falls below 3.2 V. It will be reset at the end of a READ operation.

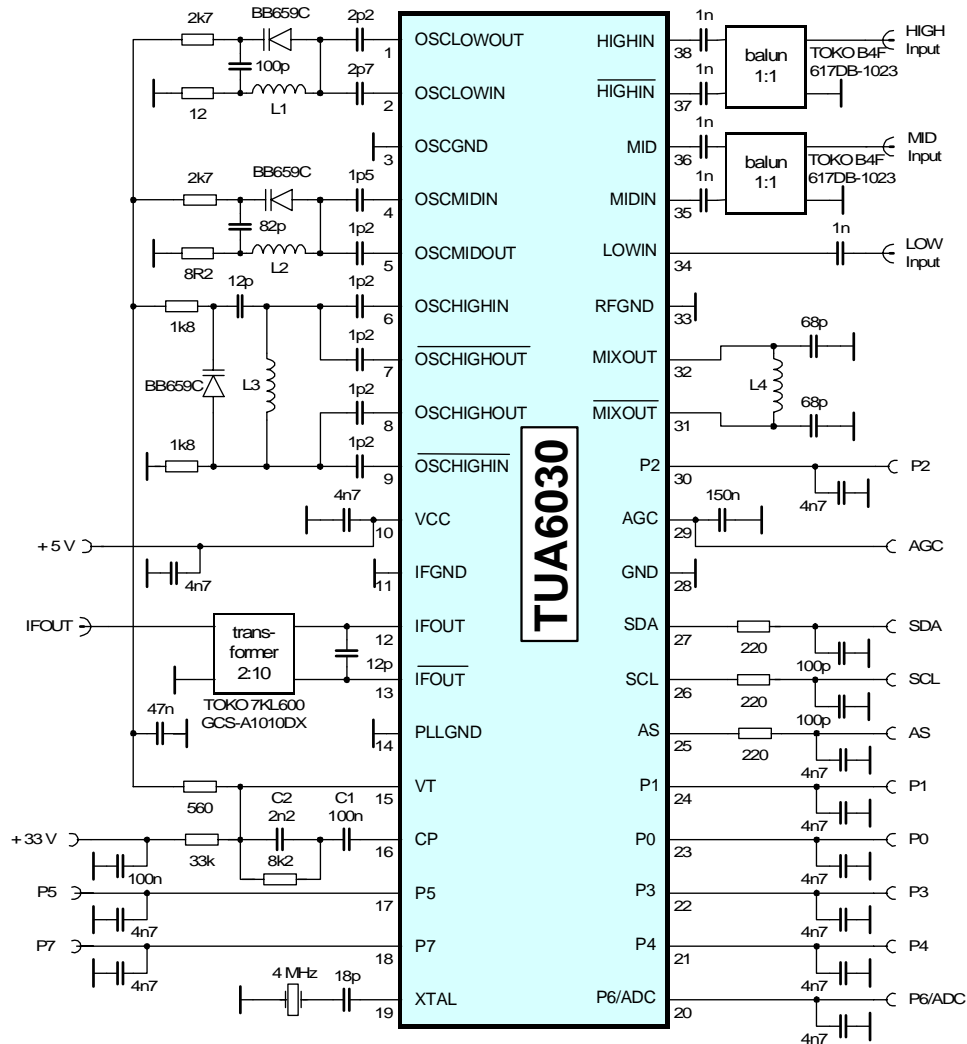
4 Applications

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4.1 Circuits

Remark: Pinning refers to TUA6030



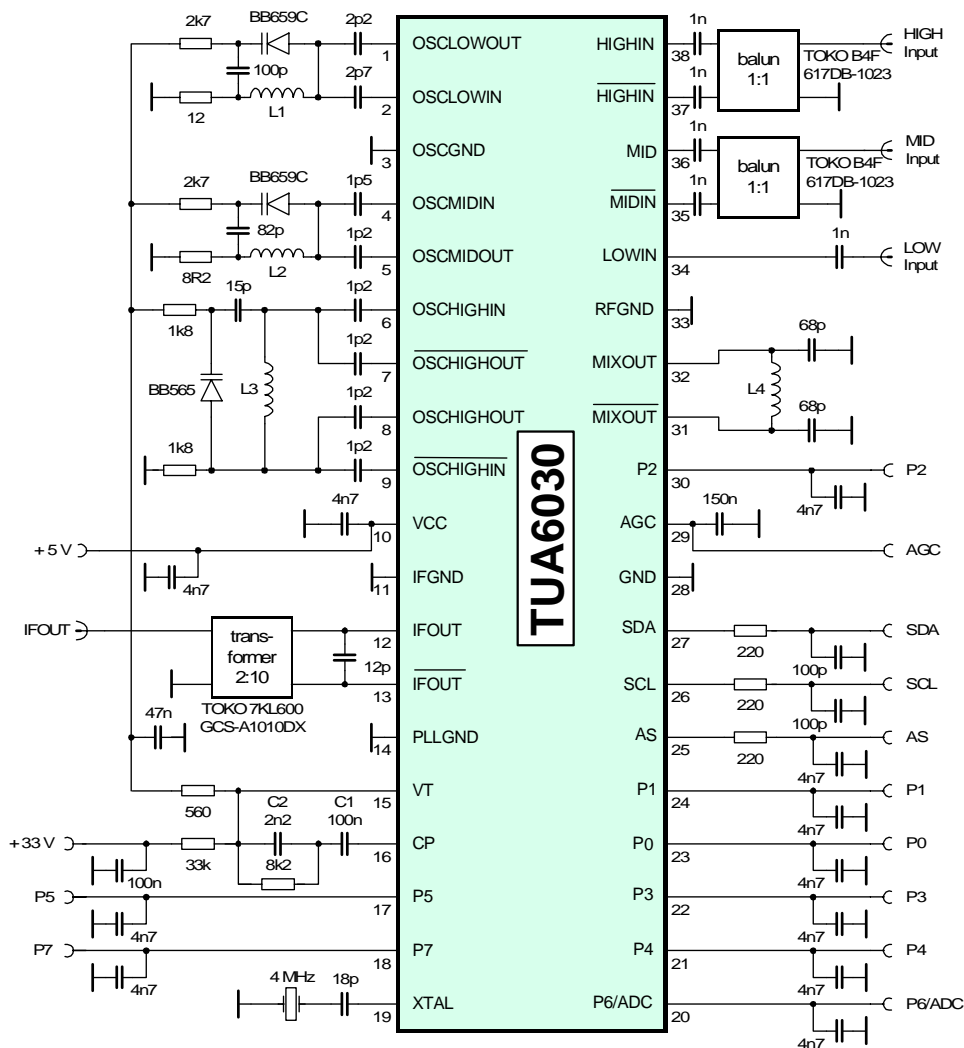
App Circuit Nisc

Figure 4-1 Application Circuit for NTSC

| | Recommended band limits in MHz | | | |
|------|--------------------------------|--------|------------|-----|
| | RF input | | Oscillator | |
| | min | max | min | max |
| LOW | 55.25 | 127.25 | 101 | 173 |
| MID | 133.25 | 361.25 | 179 | 407 |
| HIGH | 367.25 | 801.25 | 413 | 847 |

| | Coils | | |
|----|-------|--------|--------|
| | turns | ∅ | wire ∅ |
| L1 | 8.5 | 3.2 mm | 0.5 mm |
| L2 | 3.5 | 2.5 mm | 0.5 mm |
| L3 | 1.5 | 2.4 mm | 0.5 mm |
| L4 | 12.5 | 3.5 mm | 0.3 mm |

Remark: Pinning refers to TUA6030



App Circuit PAL

Figure 4-2 Application Circuit for PAL

| Recommended band limits in MHz | | | | |
|--------------------------------|----------|--------|------------|--------|
| | RF input | | Oscillator | |
| | min | max | min | max |
| LOW | 44.25 | 154.25 | 83.15 | 193.15 |
| MID | 161.25 | 439.25 | 200.15 | 478.15 |
| HIGH | 447.25 | 863.25 | 486.15 | 902.15 |

| | Coils | | |
|----|-------|--------|--------|
| | turns | ∅ | wire ∅ |
| L1 | 8.5 | 3.2 mm | 0.5 mm |
| L2 | 2.5 | 3 mm | 0.5 mm |
| L3 | 1.5 | 2.4 mm | 0.5 mm |
| L4 | 14.5 | 4 mm | 0.3 mm |

5 Reference

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5.1 Electrical Data

5.1.1 Absolute Maximum Ratings



WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 5-1 Absolute Maximum Ratings, ambient temperature $T_{AMB} = -10^{\circ}\text{C} \dots T_{Amax}$

| Parameter ¹⁾ | Symbol | Limit Values | | Unit | Remarks |
|---|--------------|--------------|-------------------|--------------------|----------------|
| | | min | max | | |
| Supply voltage | V_{CC} | -0.3 | 6 | V | |
| Ambient temperature | T_A | -10 | T_{Amax} 2). | $^{\circ}\text{C}$ | |
| Storage temperature | T_{Stg} | -40 | +125 | $^{\circ}\text{C}$ | |
| Junction temperature | T_J | | +125 | $^{\circ}\text{C}$ | |
| Temperature difference junction to case ³⁾ | T_{JC} | | 2 | K | |
| PLL | | | | | |
| CP | V_{CP} | -0.3 | 3 | V | |
| | I_{CP} | | 1 | mA | |
| Crystal oscillator pin XTAL | V_Q | | 6 | V | |
| | I_Q | -5 | | mA | |
| Bus input/output SDA | V_{SDA} | -0.3 | 6 | V | |
| Bus output current SDA | $I_{SDA(L)}$ | | 10 | mA | open collector |
| Bus input SCL | V_{SCL} | -0.3 | 6 | V | |
| Chip address switch AS | V_{AS} | -0.3 | 6 | V | |
| VCO tuning output (loop filter) | V_{VT} | -0.3 | 35 | V | |

Table 5-1 Absolute Maximum Ratings, ambient temperature $T_{AMB} = -10^{\circ}\text{C} \dots +85^{\circ}\text{C}$ (continued)

| Parameter ^{1.)} | Symbol | Limit Values | | Unit | Remarks |
|--|-------------------|--------------|-----|------|--|
| | | min | max | | |
| NPN port output voltage | $V_{P4, 5, 7}$ | -0.3 | 6 | V | open collector |
| NPN port output current | $I_{P4, 5, 7(L)}$ | -1 | 10 | mA | open collector, $t_{max} = 0.1$ sec. at 5.5 V |
| P6/ADC input/output voltage | $V_{P6/ADC}$ | -0.3 | 6 | V | |
| NPN port output current | $I_{P6/ADC(L)}$ | -1 | 10 | mA | open collector, $t_{max} = 0.1$ sec. at 5.5 V |
| PNP port output voltage | $V_{P0, 1, 2, 3}$ | -0.3 | 6 | V | open collector |
| PNP port output current | $I_{P1(L)}$ | +1 | -25 | mA | open collector, $t_{max} = 0.1$ sec. at 5.5 V |
| PNP port output current | $I_{P0(L)}$ | +1 | -10 | mA | open collector, $t_{max} = 0.1$ sec. at 5.5 V |
| PNP port output current | $I_{P2, 3(L)}$ | +1 | -5 | mA | open collector, $t_{max} = 0.1$ sec. at 5.5 V |
| Total port output current of NPN ports | $\Sigma I_{P(L)}$ | | 40 | mA | $t_{max} = 0.1$ sec. at 5.5 V |
| Total port output current of PNP ports | $\Sigma I_{P(L)}$ | | -40 | mA | $t_{max} = 0.1$ sec. at 5.5 V |
| Mixer-Oscillator | | | | | |
| Mix inputs LOW band | V_{LOW} | -0.3 | 3 | V | |
| Mix inputs MID/HIGH band | $V_{MID/HIGH}$ | | 2 | V | |
| | $I_{MID/HIGH}$ | -5 | 6 | mA | |
| VCO base voltage | V_B | -0.3 | 3 | V | LOW, MID and HIGH band oscillators |
| VCO collector voltage | V_C | | 6 | V | LOW, MID and HIGH band oscillators |
| ESD-Protection ^{4.)} | | | | | |
| all pins | V_{ESD} | | 2 | kV | |

1). All values are referred to ground (pin), unless stated otherwise.

Currents with a positive sign flow into the pin and currents with a negative sign flow out of pin.

2). The maximum ambient temperature depends on the mounting conditions of the package. Any application mounting must guarantee not to exceed the maximum junction temperature of 125 °C. As reference the temperature difference junction to case is given.

3). Referred to top center of package.

4). According to EIA/JESD22-A114-B (HBM in-circuit test), as a single device in-circuit contact discharge test.

5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

| Table 5-2 Operating Range | | | | | | | |
|---|------------|--------------|-------------------|------|-----------------|---|------|
| Parameter | Symbol | Limit Values | | Unit | Test Conditions | L | Item |
| | | min | max | | | | |
| Supply voltage | V_{CC} | +4.5 | +5.5 | V | | | |
| Programmable divider factor | N | 256 | 32767 | | | | |
| LOW mixer input frequency range | f_{MIXV} | 30 | 200 | MHz | | | |
| MID and HIGH band mixer input frequency range | f_{MIXU} | 130 | 900 | MHz | | | |
| LOW oscillator frequency range | f_{OH} | 65 | 250 | MHz | | | |
| MID band oscillator frequency range | f_{OU} | 165 | 530 | MHz | | | |
| HIGH band oscillator frequency range | f_{OU} | 400 | 950 | MHz | | | |
| Ambient temperature | T_{AMB} | -10 | T_{Amax} 1). | °C | | | |

1). see 5.1.1 Absolute Maximum Ratings on page 27

5.1.3 AC/DC Characteristics

Table 5-3 AC/DC Characteristics with $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V}$

| | Symbol | Limit Values | | | Unit | Test Conditions | L | Item |
|---|------------|--------------|-----------|------|---------------|---|---|------|
| | | min | typ | max | | | | |
| Supply | | | | | | | | |
| Supply voltage | V_{CC} | 4.5 | 5 | 5.5 | V | | | |
| Current consumption | I_{VCC} | | 73 | | mA | LOW band | | |
| | I_{VCC} | | 75 | | mA | MID band | | |
| | I_{VCC} | - | 66 | | mA | HIGH band | | |
| Digital Part | | | | | | | | |
| PLL | | | | | | | | |
| Crystal oscillator connections XTAL | | | | | | | | |
| Crystal frequency | f_{XTAL} | 3.2 | 4.0 | 4.48 | MHz | series resonance | | |
| Crystal resistance | R_Q | 25 | | 300 | Ω | series resonance | | |
| Input impedance | Z_Q | -1000 | -1200 | | Ω | $f_{XTAL} = 4\text{ MHz}$ | | |
| Charge pump output CP | | | | | | | | |
| High-level output current | I_{CPH} | | ± 280 | | μA | CP = 1, $V_{CP} = 2\text{ V}$ | | |
| Low-level output current | I_{CPL} | | ± 60 | | μA | CP = 0, $V_{CP} = 2\text{ V}$ | | |
| Tristate current | I_{CPZ} | | +1 | | nA | T2, T1, T0 = 0, 1, 0, $V_{CP} = 2\text{ V}$ | | |
| Output voltage | V_{CP} | 1.0 | | 2.5 | V | loop closed | | |
| Tuning voltage output VT (open collector) | | | | | | | | |
| Leakage current | I_{TH} | | | 10 | μA | $V_{TH} = 33\text{ V}$, OS = 1 | | |
| Output voltage when the loop is closed, (test mode in normal operation) | V_{TL} | 0.4 | | 32.7 | V | OS=0, $R_{Load} = 33\text{ k}\Omega$, tuning supply = 33 V | | |
| I²C-Bus | | | | | | | | |
| Bus inputs SCL, SDA | | | | | | | | |
| High-level input voltage | V_{IH} | 2.3 | | 5.5 | V | | | |
| Low-level input voltage | V_{IL} | 0 | | 1.5 | V | | | |
| High-level input current | I_{IH} | | | 10 | μA | $V_{bus} = 5.5\text{ V}$, $V_{CC} = 0\text{ V}$ | | |
| | I_{IH} | | | 10 | μA | $V_{bus} = 5.5\text{ V}$, $V_{CC} = 5.5\text{ V}$ | | |

Table 5-3 AC/DC Characteristics with $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V}$ (continued)

| | Symbol | Limit Values | | | Unit | Test Conditions | L | Item |
|---|---------------|--------------|------|-----|---------------|---|---|------|
| | | min | typ | max | | | | |
| Low-level input current | I_{IL} | | | 10 | μA | $V_{bus} = 1.5\text{ V}$, $V_{CC} = 0\text{ V}$ | | |
| | I_{IL} | -10 | | | μA | $V_{bus} = 0\text{ V}$, $V_{CC} = 5.5\text{ V}$ | | |
| Bus output SDA (open collector) | | | | | | | | |
| Leakage current | I_{OH} | | | 10 | μA | $V_{OH} = 5.5\text{ V}$ | | |
| Low-level output voltage | V_{OL} | | | 0.4 | V | $I_{OL} = 3\text{ mA}$ | | |
| Low-level output voltage | V_{OL} | | | 0.6 | V | $I_{OL} = 6\text{ mA}$ at 400 kHz | | |
| Edge speed SCL,SDA | | | | | | | | |
| Rise time | t_r | | | 300 | ns | | | |
| Fall time | t_f | | | 300 | ns | | | |
| Clock timing SCL | | | | | | | | |
| Frequency | f_{SCL} | 0 | 100 | 400 | kHz | | | |
| High pulse width | t_H | 0.6 | | | μs | | | |
| Low pulse width | t_L | 1.3 | | | μs | | | |
| Start condition | | | | | | | | |
| Set-up time | t_{susta} | 0.6 | | | μs | | | |
| Hold time | t_{hsta} | 0.6 | | | μs | | | |
| Stop condition | | | | | | | | |
| Set up time | t_{susto} | 0.6 | | | μs | | | |
| Bus free | t_{buf} | 1.3 | | | μs | | | |
| Data transfer | | | | | | | | |
| Set-up time | t_{sudat} | 0.1 | | | μs | | | |
| Hold time | t_{hdat} | 0 | | | μs | | | |
| Input hysteresis SCL, SDA | V_{hys} | | 200 | | mV | | | |
| Pulse width of spikes which are suppressed | t_{sp} | 0 | | 50 | ns | | | |
| Capacitive load for each bus line | C_L | | | 400 | pF | | | |
| PNP port outputs P0, P1, P2, P3 (open collector) | | | | | | | | |
| Output leakage current | $I_{POH0to3}$ | | | -10 | μA | $V_{CC} = 5.5\text{ V}$ | | |
| Output saturation voltage port 0 | V_{PL0} | | 0.25 | 0.4 | V | $I_{POL0} = 10\text{ mA}$ | | |
| Output saturation voltage port 1 | V_{PL1} | | 0.25 | 0.4 | V | $I_{POL1} = 15\text{ mA}$ | | |

Table 5-3 AC/DC Characteristics with $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V}$ (continued)

| | Symbol | Limit Values | | | Unit | Test Conditions | L | Item |
|---|---------------|--------------|------|--------|------------------|--|---|------|
| | | min | typ | max | | | | |
| Output saturation voltage ports 2, 3 | $V_{PL2,3}$ | | 0.25 | 0.4 | V | $I_{POL2,3} = 5\text{ mA}$ | | |
| NPN port outputs P4, P5, P6, P7 (open collector) | | | | | | | | |
| Output leakage current | $I_{POH4to7}$ | | | 10 | μA | $V_{CC} = 5.5$, $V_{Pn4to7} = 6\text{ V}$ | | |
| Output saturation voltage | $V_{PL04to7}$ | | 0.25 | 0.4 | V | $I_{POL4to7} = 5\text{ mA}$ | | |
| ADC input | | | | | | | | |
| ADC input voltage | V_{ADC} | 0 | | 5.5 | V | | | |
| High-level input current | I_{ADCH} | | | 10 | μA | | | |
| Low-level input current | I_{ADCL} | -10 | | | μA | | | |
| Address selection input AS | | | | | | | | |
| High-level input current | I_{ASH} | | | 50 | μA | $V_{ASH} = 5.5\text{ V}$ | | |
| Low-level input current | I_{ASL} | -50 | | | μA | $V_{ASL} = 0\text{ V}$ | | |
| Analog Part | | | | | | | | |
| LOW band mixer mode (P0 = 1, P1 = 0, including IF amplifier) | | | | | | | | |
| RF frequency | f_{RF} | 44.25 | | 170.25 | MHz | picture carrier ¹⁾ . | | |
| Voltage gain | G_V | 23.5 | 26 | 28.5 | dB | $f_{RF} = 44.25\text{ MHz}$, see 5.5.1 on page 46 | | |
| | G_V | 23.5 | 26 | 28.5 | dB | $f_{RF} = 170.25\text{ MHz}$, see 5.5.1 on page 46 | | |
| Noise figure | NF | | 8 | 10 | dB | $f_{RF} = 50\text{ MHz}$, see 5.5.4 on page 47 , see 5.5.3 on page 47 | | |
| Output voltage causing 0.3% of crossmodulation in channel | V_O | 108 | 111 | | dB μV | $f_{RF} = 44.25\text{ MHz}$, see 5.5.6 on page 48 | | |
| | V_O | 108 | 111 | | dB μV | $f_{RF} = 170.25\text{ MHz}$, see 5.5.6 on page 48 | | |
| Output voltage causing 1.1 kHz incidental FM | V_O | 108 | 111 | | dB μV | $f_{RF} = 44.25\text{ MHz}$ ²⁾ . | | |
| | V_O | 108 | 111 | | dB μV | $f_{RF} = 170.25\text{ MHz}$ ²⁾ . | | |
| Local oscillator FM caused by I ² C communication | FM_{I2C} | | | 2.12 | kHz | $f_{RF} = 170.25\text{ MHz}$ ³⁾ . | | |
| 750 Hz Pulling | V_i | 88 | | | dB μV | $f_{RF} = 154.25\text{ MHz}$ ⁴⁾ . | | |
| Channel S02 beat | INT_{S02} | 57 | 60 | | dBc | $V_{RFpix} = 115\text{ dB}\mu\text{V}$ at IF output ⁵⁾ . | | |

Table 5-3 AC/DC Characteristics with $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{V}$ (continued)

| | Symbol | Limit Values | | | Unit | Test Conditions | L | Item |
|--|----------------|--------------|-----|--------|------------------|---|---|------|
| | | min | typ | max | | | | |
| Channel A-5 beat | INT_{A-5} | 57 | 60 | | dBc | $V_{RFpix} = 115\text{ dB}\mu\text{V}$ at IF output ⁶⁾ . | | |
| Channel CH6 color beat | INT_{CH6} | 63 | 66 | | dBc | $V_{RFpix} = 80\text{ dB}\mu\text{V}$ $V_{RFsnd} = 80\text{ dB}\mu\text{V}$ ⁷⁾ . | | |
| RF input level without lock-out | V_i | | | 120 | dB μV | ⁸⁾ . | | |
| Input conductance | g_i | | 1 | | mS | $f_{RF} = 44.25\text{ MHz}$, see 5.4.1 on page 43 | | |
| | g_i | | 1 | | mS | $f_{RF} = 170.25\text{ MHz}$, see 5.4.1 on page 43 | | |
| Input capacitance | C_{MixV} | | 1 | | pF | $f_{RF} = 44.25$ to 170.25 MHz , see 5.4.1 on page 43 | | |
| Mid band mixer mode (P0 = 0, P1 =1, including IF amplifier) | | | | | | | | |
| RF frequency | f_{RF} | 154.25 | | 454.25 | | picture carrier ^{1.)} | | |
| Voltage gain | G_V | 33 | 36 | 39 | dB | $f_{RF} = 154.25\text{ MHz}$, see 5.5.2 on page 46 | | |
| | G_V | 33 | 36 | 39 | dB | $f_{RF} = 454.25\text{ MHz}$, see 5.5.2 on page 46 | | |
| Noise figure (not corrected for image) | NF | | 6 | 8 | dB | $f_{RF} = 154.25\text{ MHz}$, see 5.5.5 on page 48 | | |
| | NF | | 6 | 8 | dB | $f_{RF} = 300\text{ MHz}$, see 5.5.5 on page 48 | | |
| Output voltage causing 0.3% of crossmodulation in channel | V_O | 108 | 111 | | dB μV | $f_{RF} = 154.25\text{ MHz}$, see 5.5.7 on page 49 | | |
| | V_O | 108 | 111 | | dB μV | $f_{RF} = 454.25\text{ MHz}$, see 5.5.7 on page 49 | | |
| Output voltage causing 1.1 kHz incidental FM | V_O | 108 | 111 | | dB μV | $f_{RF} = 154.25\text{ MHz}$ ^{2.)} | | |
| | V_O | 108 | 111 | | dB μV | $f_{RF} = 454.25\text{ MHz}$ ^{2.)} | | |
| Local oscillator FM caused by I ² C communi- cation | FM_{I2C} | | | 2.12 | kHz | $f_{RF} = 454.25\text{ MHz}$ ^{3.)} | | |
| N+5 - 1 MHz pulling | N+5 - 1 MHz | 77 | 80 | | dB μV | $f_{RFw} = 359.25\text{ MHz}$, $f_{OSC} = 398.15\text{ MHz}$, $f_{RFu} = 399.25\text{ MHz}$ ⁹⁾ . | | |

Table 5-3 AC/DC Characteristics with $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{V}$ (continued)

| | Symbol | Limit Values | | | Unit | Test Conditions | L | Item |
|--|-------------------|--------------|-----|--------|------------|--|---|------|
| | | min | typ | max | | | | |
| 750 Hz Pulling | V_i | 78 | | | dB μ V | $f_{RF} = 439.25\text{ MHz}$ ^{4.)} | | |
| RF input level without lock-out | V_i | | | 120 | dB μ V | 8.) | | |
| Input impedance $Z_i = (R_s + j\omega L_s)$ | R_s | | 35 | | Ω | $f_{RF} = 154.25.25\text{ MHz}$, see 5.4.2 on page 43 | | |
| | R_s | | 30 | | Ω | $f_{RF} = 454.25\text{ MHz}$, see 5.4.2 on page 43 | | |
| | L_s | | 5 | | nH | $f_{RF} = 154.25.25\text{ MHz}$, see 5.4.2 on page 43 | | |
| | L_s | | 4.5 | | nH | $f_{RF} = 454.25\text{ MHz}$, see 5.4.2 on page 43 | | |
| HIGH band mixer mode ($P_0 = 0$, $P_1 = 0$, including IF amplifier) | | | | | | | | |
| RF frequency | f_{RF} | 399.25 | | 863.25 | | picture carrier ^{1.)} | | |
| Voltage gain | G_V | 33 | 36 | 39 | dB | $f_{RF} = 407.25\text{ MHz}$, see 5.5.2 on page 46 | | |
| | G_V | 33 | 36 | 39 | dB | $f_{RF} = 863.25\text{ MHz}$, see 5.5.2 on page 46 | | |
| Noise figure (not corrected for image) | NF | | 6 | 8 | dB | $f_{RF} = 407.25\text{ MHz}$, see 5.5.5 on page 48 | | |
| | NF | | 7 | 9 | dB | $f_{RF} = 863.25\text{ MHz}$, see 5.5.5 on page 48 | | |
| Output voltage causing 0.3% of crossmodulation in channel | V_O | 108 | 111 | | dB μ V | $f_{RF} = 407.25\text{ MHz}$, see 5.5.7 on page 49 | | |
| | V_O | 108 | 111 | | dB μ V | $f_{RF} = 863.25\text{ MHz}$, see 5.5.7 on page 49 | | |
| Output voltage causing 1.1 kHz incidental FM | V_O | 108 | 111 | | dB μ V | $f_{RF} = 407.25\text{ MHz}$ ^{2.)} | | |
| | V_O | 108 | 111 | | dB μ V | $f_{RF} = 454.25\text{ MHz}$ ^{2.)} | | |
| Local oscillator FM caused by I ² C communication | FM _{I2C} | | | 2.12 | kHz | $f_{RF} = 863.25\text{ MHz}$ ^{3.)} | | |
| N+5 - 1 MHz pulling | N+5 - 1 MHz | 77 | 80 | | dB μ V | $f_{RFw} = 823.25\text{ MHz}$, $f_{OSC} = 862.15\text{ MHz}$, $f_{RFu} = 862.25\text{ MHz}$ ^{9.)} | | |
| 750 Hz Pulling | V_i | 78 | | | dB μ V | $f_{RF} = 855.25\text{ MHz}$ ^{4.)} | | |

Table 5-3 AC/DC Characteristics with $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{V}$ (continued)

| | Symbol | Limit Values | | | Unit | Test Conditions | L | Item |
|--|---------------------|--------------|-----|-----|------------|---|---|------|
| | | min | typ | max | | | | |
| RF input level without lock-out | V_i | | | 120 | dB μ V | 8.) | | |
| Input impedance $Z_i = (R_s + j\omega L_s)$ | R_s | | 35 | | Ω | $f_{RF} = 407.25\text{ MHz}$, see 5.4.3 on page 44 | | |
| | R_s | | 30 | | Ω | $f_{RF} = 863.25\text{ MHz}$, see 5.4.3 on page 44 | | |
| | L_s | | 5 | | nH | $f_{RF} = 407.25\text{ MHz}$, see 5.4.3 on page 44 | | |
| | L_s | | 4.5 | | nH | $f_{RF} = 863.25\text{ MHz}$, see 5.4.3 on page 44 | | |
| LOW band oscillator, Chapter 4 | | | | | | | | |
| Oscillator frequency | f_{OSC} | 80 | | 210 | MHz | 10.) | | |
| Oscillator frequency shift | $\Delta f_{OSC(V)}$ | | 20 | 70 | kHz | $\Delta V_{CC} = 5\%$ 11.) | | |
| | $\Delta f_{OSC(V)}$ | | 110 | | kHz | $\Delta V_{CC} = 10\%$ 11.) | | |
| Oscillator frequency drift | $\Delta f_{OSC(T)}$ | | 300 | 500 | kHz | $\Delta T = 25\text{ }^{\circ}\text{C}$, with compensation 12.) | | |
| Oscillator frequency drift | $\Delta f_{OSC(t)}$ | | 150 | 250 | kHz | 5 s to 15 min after switch on 13.) | | |
| Phase noise, carrier to noise sideband | Φ_{OSC} | 88 | 92 | | dBc/ Hz | $\pm 10\text{ kHz}$ frequency offset, worst case in frequency range | | |
| Ripple susceptibility of V_P | RSC | 15 | 20 | | mV | $4.75\text{ V} < V_P < 5.25\text{ V}$, worst case in fre- quency range, ripple frequency 500 kHz 14.) | | |
| MID band oscillator, Chapter 4 | | | | | | | | |
| Oscillator frequency | f_{OSC} | 201 | | 493 | MHz | 10.) | | |
| Oscillator frequency shift | $\Delta f_{OSC(V)}$ | | 20 | 70 | kHz | $\Delta V_{CC} = 5\%$ 11.) | | |
| | $\Delta f_{OSC(V)}$ | | 110 | | kHz | $\Delta V_{CC} = 10\%$ 11.) | | |
| Oscillator frequency drift | $\Delta f_{OSC(T)}$ | | 500 | 750 | kHz | $\Delta T = 25\text{ }^{\circ}\text{C}$; with com- pensation 12.) | | |
| Oscillator frequency drift | $\Delta f_{OSC(t)}$ | | 250 | 500 | kHz | 5 s to 15 min after switch on 13.) | | |
| Phase noise, carrier to noise sideband | Φ_{OSC} | 86 | 92 | | dBc/ Hz | $\pm 10\text{ kHz}$ frequency offset, worst case in frequency range | | |

Table 5-3 AC/DC Characteristics with $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V}$ (continued)

| | Symbol | Limit Values | | | Unit | Test Conditions | L | Item |
|--|---------------------|--------------|-----|------|------------|--|---|------|
| | | min | typ | max | | | | |
| Ripple susceptibility of V_P | RSC | 15 | 20 | | mV | 4.75 < VP < 5.25 V, worst case in frequency range, ripple frequency 500 kHz 14.) | | |
| HIGH band oscillator, Chapter 4 | | | | | | | | |
| Oscillator frequency | f_{OSC} | 435 | | 905 | MHz | 10.) | | |
| Oscillator frequency shift | $\Delta f_{OSC(V)}$ | | 20 | 70 | kHz | $\Delta V_{CC} = 5\%$ 11.) | | |
| | $\Delta f_{OSC(V)}$ | | 300 | | kHz | $\Delta V_{CC} = 10\%$ 11.) | | |
| Oscillator frequency drift | $\Delta f_{OSC(T)}$ | | 600 | 1000 | kHz | $\Delta T = 25\text{ }^{\circ}\text{C}$; with compensation 12.) | | |
| Oscillator frequency drift | $\Delta f_{OSC(t)}$ | | 250 | 500 | kHz | 5 s to 15 min after switch on 13.) | | |
| Phase noise, carrier to noise sideband | Φ_{OSC} | 86 | 90 | | dBc/Hz | $\pm 10\text{ kHz}$ frequency offset, worst case in frequency range | | |
| Ripple susceptibility of V_P | RSC | 15 | 20 | | mV | 4.75 < VP < 5.25 V, worst case in frequency range, ripple frequency 500 kHz 14.) | | |
| IF amplifier | | | | | | | | |
| Mixer output impedance $Y_o = G_s + j\omega C_s$ | G_p | | 3 | | mS | at 36 MHz, see 5.4.4 on page 44 | | |
| | C_p | | 4 | | pF | at 36 MHz, see 5.4.4 on page 44 | | |
| IF amplifier output impedance $Z_o = R_s + j\omega L_s$ | R_s | | 65 | | Ω | at 36 MHz, see 5.4.5 on page 45 | | |
| | L_s | | 20 | | nH | at 36 MHz, see 5.4.5 on page 45 | | |
| Rejection at the IF outputs | | | | | | | | |
| Level of divider interferences in the IF signal | INT_{DIV} | | | 20 | dB μ V | 15), worst case | | |
| Crystal oscillator interferences rejection | INT_{XTAL} | 60 | 66 | | dBc | $V_{IF} = 100\text{ dB}\mu\text{V}$, worst case in frequency range 16). | | |
| Reference frequency rejection | INT_{REF} | 60 | 66 | | dBc | $V_{IF} = 100\text{ dB}\mu\text{V}$, worst case in frequency range 17). | | |
| AGC output | | | | | | | | |
| AGC take-over point | AGC_{TOP} | 111 | 112 | 113 | dB μ V | AL2, AL1, AL0 = 0, 1, 0 | | |

Table 5-3 AC/DC Characteristics with $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 5V_C$ (continued)

| | Symbol | Limit Values | | | Unit | Test Conditions | L | Item |
|---|--------------|--------------|-----|------------------------|---------------|---|---|------|
| | | min | typ | max | | | | |
| Source current 1 | AGC_{fast} | 7.2 | 9.0 | 10.8 | μA | | | |
| Source current 2 | AGC_{slow} | 185 | 220 | 264 | nA | | | |
| Peak sink to ground | AGC_{peak} | 80 | 100 | 120 | μA | | | |
| AGC output voltage | V_{AGCmax} | 3.3 | 3.5 | 3.7 | V | maximum level | | |
| AGC output voltage | V_{AGCmin} | 0 | | 0.25 | V | minimum level | | |
| RF voltage range to switch the AGC from active to inactive mode | AGC_{SLIP} | | | 0.5 | dB | | | |
| AGC output voltage | AGC_{RML} | 0 | | 2.9 | V | AGC bit high or AGC active | | |
| AGC output voltage | AGC_{RMH} | 3 | 3.5 | $V_{CC} - 0.5$ or 4 | V | AGC bit low or AGC inactive | | |
| AGC leakage current | AGC_{LEAK} | -50 | | 50 | nA | AL2, AL1, AL0 = 1,1,0 $0 < V_{AGC} < V_{CC}$ | | |
| AGC output voltage | AGC_{OFF} | 3.3 | 3.5 | $V_{CC} - 0.5$ or 4 | V | AL2, AL1, AL0 = 1,1,1 AGC is disabled | | |

■ This value is only guaranteed in lab.

- 1). The RF frequency range is defined by the oscillator frequency range and the intermediate frequency (IF).
- 2). This is the level of the RF unwanted signal (50% amplitude modulated with 1kHz) that causes a 1.1 kHz FM modulation of the local oscillator and thus of the wanted signal; $V_{wanted} = 100\text{ dB}\mu\text{V}$; $f_{unwanted} = f_{wanted} + 5.5\text{ MHz}$.
- 3). Local oscillator FM modulation resulting from I²C communication is measured at the IF output using a modulation analyser with a peak to peak detector $((P_+ + P_-)/2)$ and a post detection filter 30 Hz - 200 kHz. The I²C messages are sent to the tuner in such a way that the tuner is addressed but the content of the PLL registers are not altered. The refresh interval between each data set shall be 20 ms to 1s.
- 4). This is the level of the RF signal (100% amplitude modulated with 11.89 kHz) that causes a 750 Hz frequency deviation on the oscillator signal producing sidebands 30 dB below the level of the oscillator signal.
- 5). Channel S02 beat is the interfering product of f_{RFpix} , f_{IF} and f_{OSC} of channel S02, $f_{BEAT} = 37.35\text{ MHz}$. The possible mechanisms are $f_{OSC} - 2 \times f_{IF}$ or $2 \times f_{RFpix} - f_{OSC}$.
- 6). Channel A-5 beat is the interfering product of f_{RFpix} , f_{IF} and f_{OSC} of channel A-5; $f_{BEAT} = 45.5\text{ MHz}$. The possible mechanisms are: $f_{OSC} - 2 \times f_{IF}$ or $2 \times f_{RFpix} - f_{OSC}$.
- 7). Channel 6 beat is the interfering product of $f_{RFpix} + f_{RFsnd} - f_{OSC}$ of channel 6 at 42 MHz.
- 8). The IF output signal stays stable within the range of the f_{ref} step for a low level RF input up to 120 dB μV .
- 9). N+5 -1 MHz is defined as the input level of channel N+5, at frequency 1 MHz lower, causing FM sidebands 30 dB below the wanted carrier.
- 10). Limits are related to the tank circuit used in the application board (Chapter 4). Frequency bands may be adjusted by the choice of external components.
- 11). The frequency shift is defined as a change in oscillator frequency when the supply voltage varies from $V_{CC} = 5$ to 4.75 V (4.5 V) or from $V_{CC} = 5$ to 5.25 V (5.5 V). The oscillator is free running during this measurement.
- 12). The frequency drift is defined as a change in oscillator frequency if the ambient temperature varies from $T_{amb} = 25$ to 50 °C or from $T_{amb} = 25$ to 0 °C. The oscillator is free running during this measurement.

13). The switch-on drift is defined as a change in oscillator frequency between 5 s and 15 min after switch-on. The oscillator is free running during this measurement.

14). The supply ripple susceptibility is measured in the application board (Chapter 4), using a spectrum analyser connected to the IF output. An unmodulated RF signal is applied to the test board RF input. A sinewave signal with a frequency of 500 kHz is superposed onto the supply voltage (see 5.5.8 on page 49). The amplitude of this ripple is adjusted to bring the 500 kHz sidebands around the IF carrier to a level of 53.5 dBc referred to the carrier.

15). This is the level of divider interferences close to the IF frequency. For example channel S3: $f_{OSC} = 158.15$ MHz, $1/4 f_{OSC} = 39.5375$ MHz. Divider interference is measured with the application board (Chapter 4). All ground pins are connected to a single ground plane under the IC. The LOWIN input must be left open (i.e. not connected to any load or cable). The MIDIN and HIGHIN inputs are connected to a hybrid. The measured level of divider interference are influenced by layout, grounding and port decoupling. The measurement results between various applications and the reference board could vary as much as 10 dB.

16). Crystal oscillator interference means the 4 MHz sidebands caused by the crystal oscillator. The rejection has to be greater than 60 dB for an IF output of 100 dB μ V.

17). The reference frequency rejection is the level of reference frequency sidebands (e.g. 62.5 kHz) related to the carrier. The rejection has to be greater than 60 dB for an IF output of 100 dB μ V.

5.2 Programming

Table 5-4 Bit Allocation Read / Write

| Name | Byte | Bits | | | | | | | | Ack |
|------------------------------|------|------|------|------|------|------|------|------|-----------|-----|
| | | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB | |
| Write Data | | | | | | | | | | |
| Address Byte | ADB | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R/ W=0 | A |
| Divider Byte 1 | DB1 | 0 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | A |
| Divider Byte 2 | DB2 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | A |
| Control byte | CB | 1 | CP | T2 | T1 | T0 | RSA | RSB | OS | A |
| Bandswitch byte | BB | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | A |
| Auxiliary byte ¹⁾ | AB | ATC | AL2 | AL1 | AL0 | 0 | 0 | 0 | 0 | A |
| Read data | | | | | | | | | | |
| Address byte | ADB | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R/ W=1 | A |
| Status byte | SB | POR | FL | 1 | 1 | AGC | A2 | A1 | A0 | A |

1). AB replaces BB when T2, T1, T0 = 0, 1, 1, see [Table 5-7 Test modes on page 40](#)

Table 5-5 Description of Symbols

| Symbol | Description |
|----------------|--|
| A | Acknowledge |
| MA0, MA1 | Address selection bits, see Table 5-6 Address selection on page 40 |
| N14 to N0 | programmable divider bits: $N = 2^{14} \times N14 + 2^{13} \times N13 + \dots + 2^3 \times N3 + 2^2 \times N2 + 2^1 \times N1 + N0$ |
| CP | charge pump current bit: bit = 0: charge pump current = 60 μ A bit = 1: charge pump current = 280 μ A (default) |
| T0, T1, T2 | test bits, see Table 5-7 Test modes on page 40 |
| RSA, RSB | reference divider bits, see Table 5-8 Reference divider ratios on page 40 |
| OS | tuning amplifier control bit: bit = 0: enable V_T bit = 1: disable V_T (default) |
| P0, P1, P2, P3 | PNP ports control bits bit = 0: Port is inactive, high impedance state (default) bit = 1: Port is active, $V_{OUT} = V_{CC} - V_{CESAT}$ |
| P4, P5, P6, P7 | NPN ports control bits bit = 0: Port is inactive, high impedance state (default) bit = 1: Port is active, $V_{OUT} = V_{CESAT}$ |
| ATC | AGC time constant bit bit = 0: $I_{AGC} = 220nA$; $\Delta t = 2s$ with $C = 160nF$ (default) bit = 1: $I_{AGC} = 9\mu A$; $\Delta t = 50ms$ with $C = 160nF$ |

Table 5-5 Description of Symbols

| | |
|---------------|---|
| AL0, AL1, AL2 | AGC take-over point bits |
| POR | Power-on reset flag; POR =1 at power-on |
| FL | PLL lock flag bit = 1: loop is locked |
| AGC | internal AGC flag. AGC=1 when internal AGC is active (level below 3V) |
| A0, A1, A2 | digital output of the 5-level ADC |

Table 5-6 Address selection

| Voltage at AS | MA1 | MA0 |
|--------------------------------|-----|-----|
| (0 to 0.1) * V _{CC} | 0 | 0 |
| open circuit | 0 | 1 |
| (0.4 to 0.6) * V _{CC} | 1 | 0 |
| (0.9 to 1) * V _{CC} | 1 | 1 |

Table 5-7 Test modes

| Mode | T2 | T1 | T0 |
|--|----|----|----|
| Normal operation | 0 | 0 | 0 |
| Normal operation (default) | 0 | 0 | 1 |
| CP is in high-impedance state | 0 | 1 | 0 |
| byte AB will follow (otherwise byte BB will follow) | 0 | 1 | 1 |
| P4 = f _{div} output, P5 = f _{ref} output | 1 | 0 | 0 |
| not in use | 1 | 0 | 1 |
| not in use | 1 | 1 | 0 |
| not in use | 1 | 1 | 1 |

Table 5-8 Reference divider ratios

| Reference divider ratio | f _{ref} ¹⁾ | RSA | RSB |
|-------------------------|--------------------------------|-----|-----|
| 80 | 50 kHz | 0 | 0 |
| 128 | 31.25 kHz | 0 | 1 |
| 24 | 166.7 kHz | 1 | 0 |
| 64 | 62.5 kHz | 1 | 1 |

1). With a 4 MHz quartz

Table 5-9 AGC take-over point

| IF output level, symmetrical mode | Remark | AL2 | AL1 | AL0 |
|-----------------------------------|---------------------|-----|-----|-----|
| 115 dB μ V | | 0 | 0 | 0 |
| 115 dB μ V | | 0 | 0 | 1 |
| 112 dB μ V | default mode at POR | 0 | 1 | 0 |
| 109 dB μ V | | 0 | 1 | 1 |
| 106 dB μ V | | 1 | 0 | 0 |

Table 5-9 AGC take-over point

| | | | | |
|----------------|------------------------------|---|---|---|
| 103 dB μ V | | 1 | 0 | 1 |
| $I_{AGC} = 0$ | External AGC ¹⁾ . | 1 | 1 | 0 |
| 3.5 V | Disabled ²⁾ . | 1 | 1 | 1 |

1). The AGC detector is disabled. Both the sinking and sourcing current from the IC is disabled. The AGC output goes into a high impedance state and an external AGC source can be connected in parallel and will not be influenced.

2). The AGC detector is disabled and $I_{AGC} = 9 \mu A$.

Table 5-10 A to D converter levels ¹⁾.

| Voltage at ADC | A2 | A1 | A0 |
|--------------------------|----|----|----|
| (0 to 0.15) * V_{CC} | 0 | 0 | 0 |
| (0.15 to 0.3) * V_{CC} | 0 | 0 | 1 |
| (0.3 to 0.45) * V_{CC} | 0 | 1 | 0 |
| (0.45 to 0.6) * V_{CC} | 0 | 1 | 1 |
| (0.6 to 1) * V_{CC} | 1 | 0 | 0 |

1). No erratic codes in the transition

Table 5-11 Defaults at power-on reset

| Name | Byte | Bits | | | | | | | |
|-----------------|------|------|------|------|------|------|------|------|-------|
| | | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB |
| Write Data | | | | | | | | | |
| Address Byte | ADB | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R/W=0 |
| Divider byte 1 | DB1 | 0 | X | X | X | X | X | X | X |
| Divider byte 2 | DB2 | X | X | X | X | X | X | X | X |
| Control byte | CB | 1 | 1 | 0 | 0 | 1 | X | X | 1 |
| Bandswitch byte | BB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Auxiliary byte | AB | 0 | 0 | 1 | 0 | | | | |

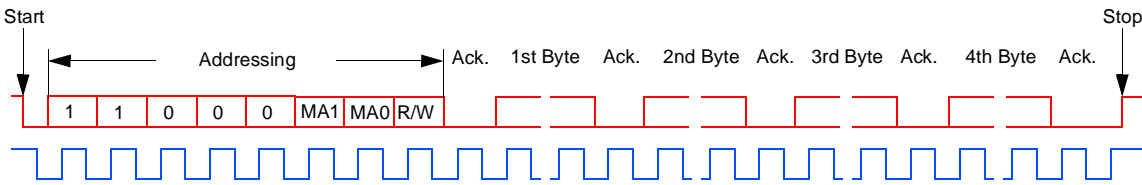
Table 5-12 Internal band selection

| Band | Mixer | Oscillator |
|----------------------|------------------------------------|--------------------|
| LOW | $P0.\overline{P1}$ ¹⁾ . | $P0.\overline{P1}$ |
| MID | $P1.P0$ | $P1.P0$ |
| HIGH ²⁾ . | $\overline{P0.P1}$ | $\overline{P0.P1}$ |

1). Means: (P0 AND NOT P1); that is: LOW mixer is switched on if (P0=1 and P1=0)

2). The HIGH band is selected by default

5.3 I²C Bus Timing Diagram



Telegram examples:

- Start-ADB-DB1-DB2-CB-BB-Stop
- Start-ADB-DB1-DB2-CB-AB-Stop
- Start-ADB-CB-BB-DB1-DB2-Stop
- Start-ADB-CB-AB-DB1-DB2-Stop
- Start-ADB-DB1-DB2-DB1-DB2-Stop
- Start-ADB-DB1-DB2-Stop
- Start-ADB-CB-BB-Stop
- Start-ADB-CB-AB-Stop
- Start-ADB-CB-BB-CB-AB-Stop
- Start-ADB-CB-AB-CB-BB-Stop

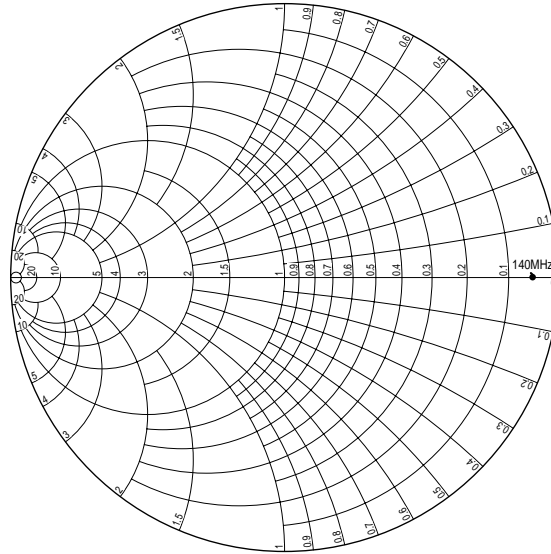
Abbreviations:

- Start= start condition
- ADB= address byte
- DB1= prog. divider byte 1
- DB2= prog. divider byte 2
- CB= Control byte
- BB= Bandswitch byte
- AB= Auxiliary byte
- Stop= stop condition

5.4 Electrical Diagrams

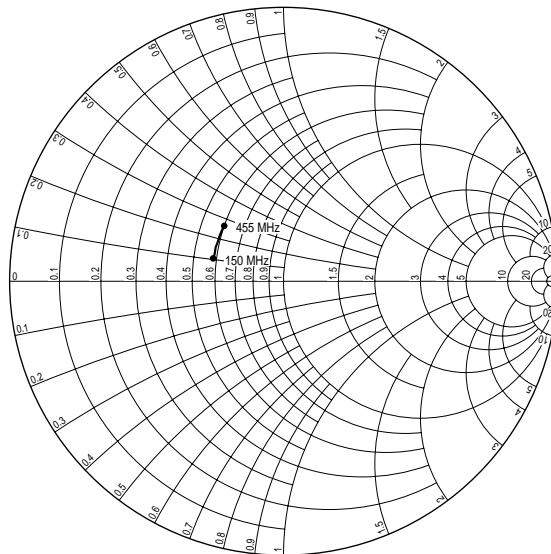
5.4.1 Input admittance (S11) of the LOW band mixer (40 to 140 MHz)

$$Y_0 = 20\text{mS}$$



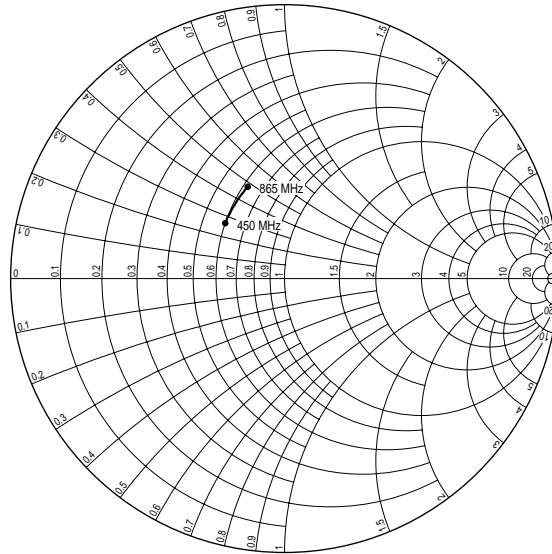
5.4.2 Input impedance (S11) of the MID band mixer (150 to 455 MHz)

$$Z_0 = 50\ \Omega$$



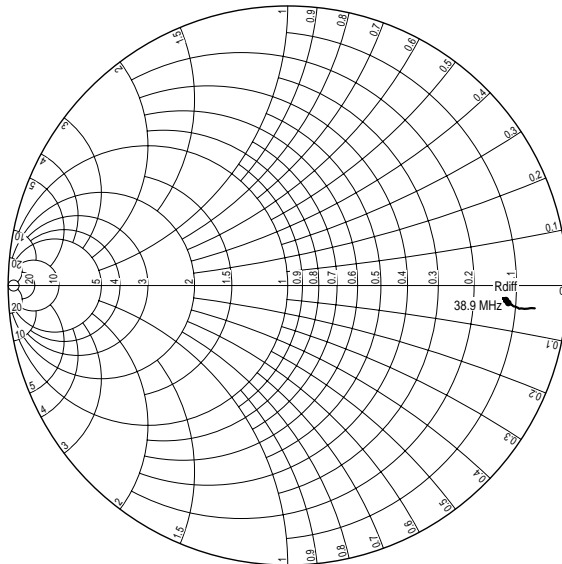
5.4.3 Input impedance (S11) of the HIGH band mixer (450 to 865 MHz)

$Z_0 = 50 \Omega$



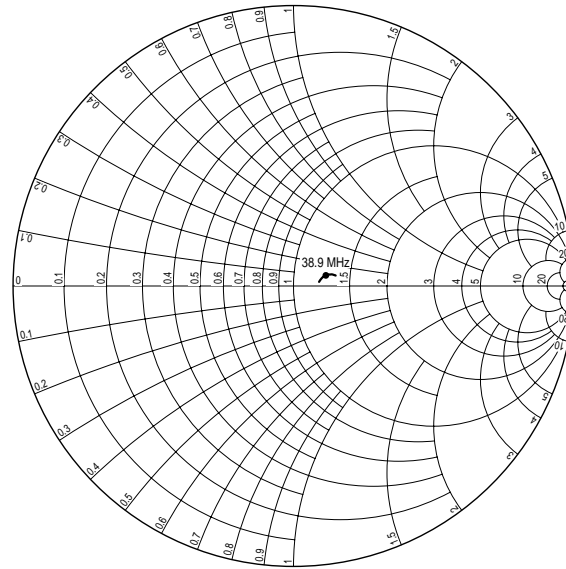
5.4.4 Output admittance (S22) of the of the Mixer output (30 to 50 MHz)

$Y_0 = 20\text{mS}$



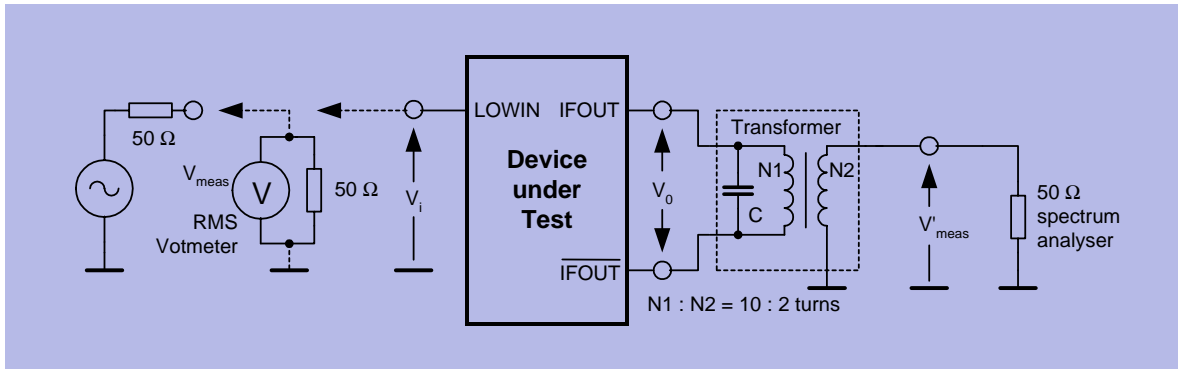
5.4.5 Output impedance (S22) of the IF amplifier (30 to 50 MHz)

$$Z_0 = 50 \Omega$$



5.5 Measurement Circuits

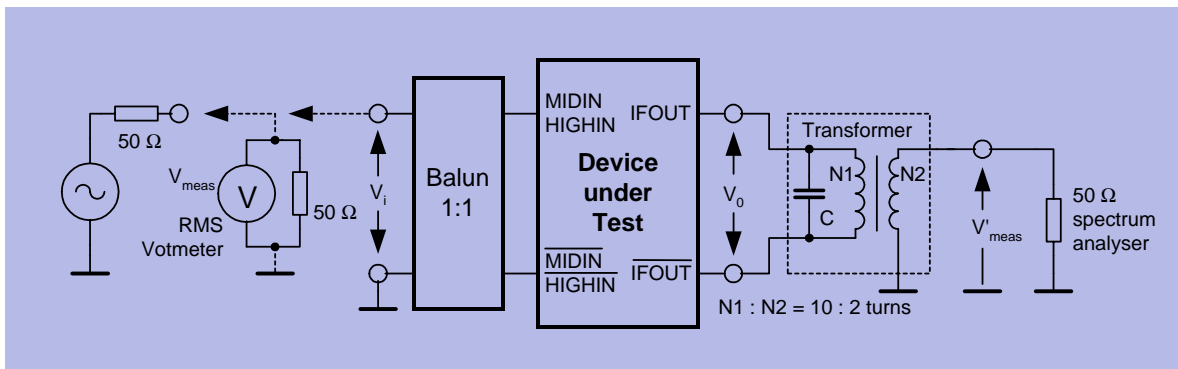
5.5.1 Gain (G_V) measurement in LOW band



GVHF

- $Z_i \gg 50 \Omega \Rightarrow V_i = 2 \times V_{meas} = 80 \text{ dB}\mu\text{V}$
- $V_i = V_{meas} + 6\text{dB} = 80 \text{ dB}\mu\text{V}$
- $V_0 = V'_{meas} + 16 \text{ dB}$ (transformer ratio N1:N2 and transformer loss)
- $G_V = 20 \log(V_0 / V_i)$

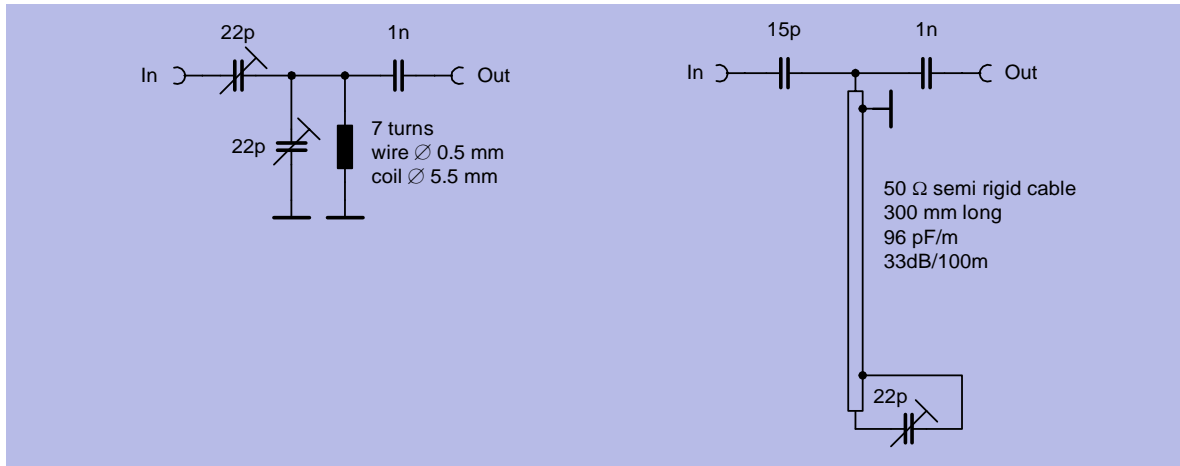
5.5.2 Gain (G_V) measurement in MID and HIGH bands



GUHF3

- $V_i = V_{meas} = 70 \text{ dB}\mu\text{V}$
- $V_0 = V'_{meas} + 16 \text{ dB}$ (transformer ratio N1:N2 and transformer loss)
- $G_V = 20 \log(V_0 / V_i) + 1 \text{ dB}$ (1 dB = insertion loss of balun)

5.5.3 Matching circuit for optimum noise figure in LOW band



NFM

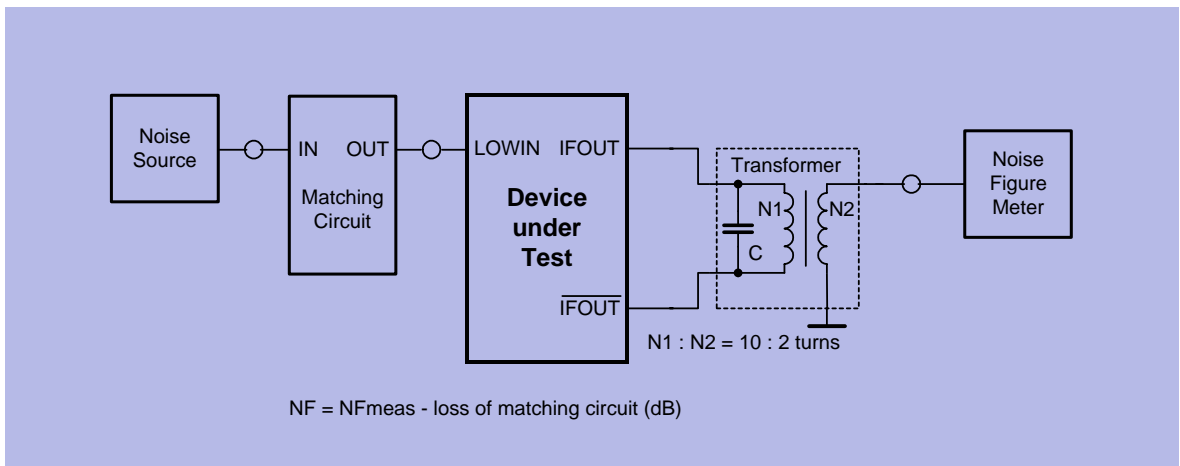
For $f_{RF} = 50 \text{ MHz}$

- loss = 0 dB
- image suppression = 16 dB

For $f_{RF} = 150 \text{ MHz}$

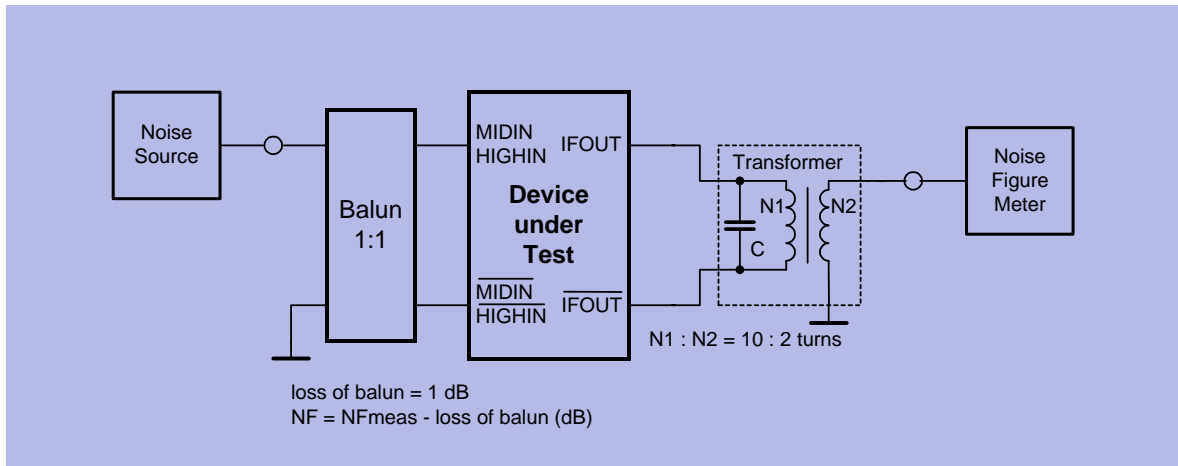
- loss = 1.3 dB
- image suppression = 13 dB

5.5.4 Noise figure (NF) measurement in LOW band



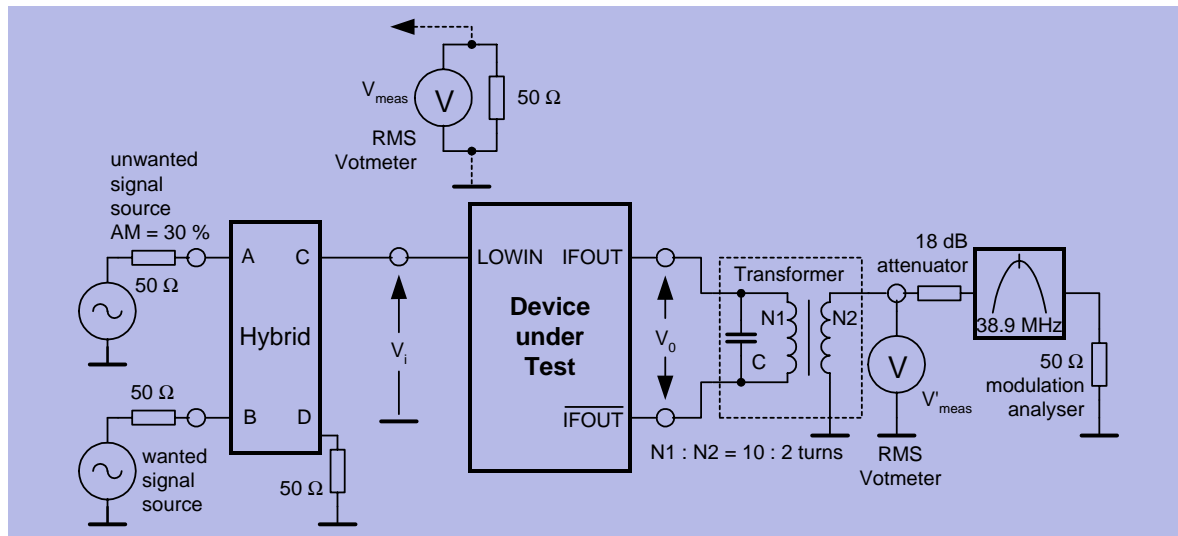
NFVHF

5.5.5 Noise figure (NF) measurement in MID and HIGH bands



NFUHF3

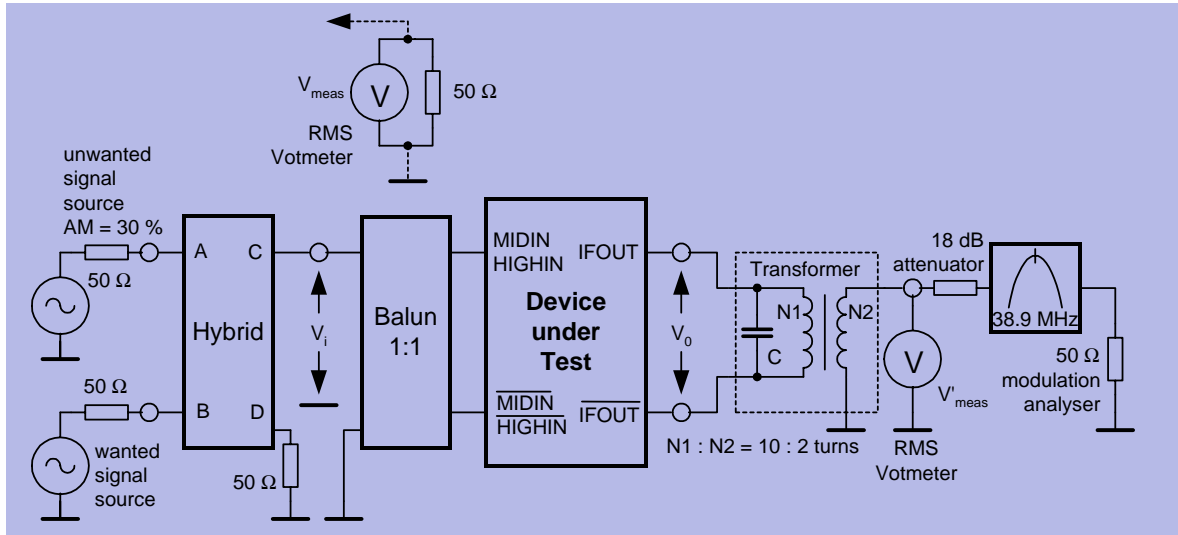
5.5.6 Cross modulation measurement in LOW band



XVHF

- $Z_i \gg 50 \Omega \Rightarrow V_i = 2 \times V_{meas}$
- $V'_{meas} = V_0 - 16 \text{ dB}$ (transformer ratio N1:N2 and transformer loss)
- wanted output signal at f_{pix} , $V_0 = 100 \text{ dB}\mu\text{V}$
- unwanted output signal at f_{snd}

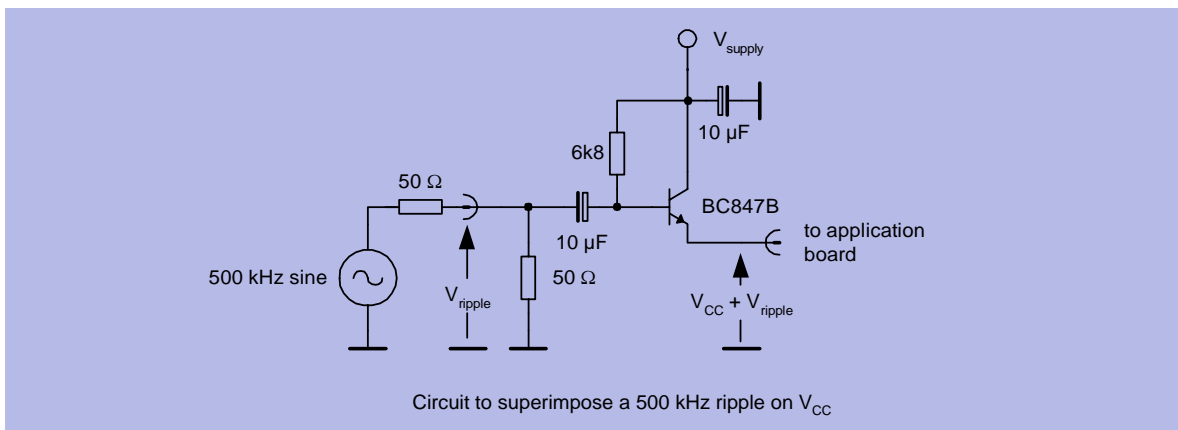
5.5.7 Cross modulation measurement in MID and HIGH bands



XUHF3

- $V'_{meas} = V_0 - 16 \text{ dB}$ (transformer ratio $N1:N2$ and transformer loss)
- wanted output signal at f_{pix} , $V_0 = 100 \text{ dB}\mu\text{V}$
- unwanted output signal at f_{snd}

5.5.8 Ripple susceptibility measurement



RIP