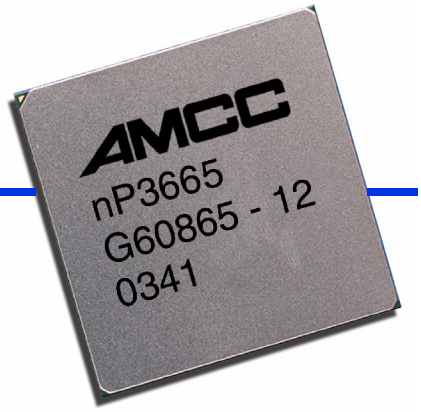


nP3665

OC-24/2GE Network Processor for Mobile Infrastructure

Applications

- Up to OC-24 line cards in mobile infrastructure including Node B, RNC, SGSN/GGSN, and MGW

Features

Supports OC-24 Traffic

- nP^5 Technology
- Mix and match Gigabit Ethernet, POS, and ATM traffic

Proven nPcore Architecture

- One nPcore at up to 700 MHz optimized for network processing
- Single-stage, single-image programming model
- High-speed RLDRAM-II memory interface for payload and context storage
- Per-flow metering and statistics for millions of flows

Integrated Traffic Manager

- Per-flow queuing and scheduling
- Sophisticated, fine-grained scheduling algorithms

Standards-Compliant Interfaces

- 2 GE with Integrated MAC
- OIF SPI-3
- ATM Forum UTOPIA-2

Benefits

- Best processing and power performance of its peers
- High integration for significant form factor, cost, and power savings
- Hardware-based Traffic Manager for guaranteed performance
- Software compatibility with previous generation nP devices
- Simple programming model for rapid development and quick time-to-market

The nP3665 integrated network processor is a derivative of the nP3700 family that expands AMCC's nP^5™ technology to lower speed, cost-sensitive mobile infrastructure applications. Developed over several generations of traffic management and network processor products, nP^5 unites the flexibility of the industry's highest performance network processing nPcore with the most widely deployed and mature traffic management technology. This unique combination enables developers to deliver extremely fine-grained control of subscriber traffic, without impacting the ability to perform complex protocol inter-working at media speeds. The nP3665 is designed from the ground up to provide software compatibility with the earlier generations of AMCC Network Processors. The single-stage programming model dramatically simplifies software development and troubleshooting for quickest time-to-market.

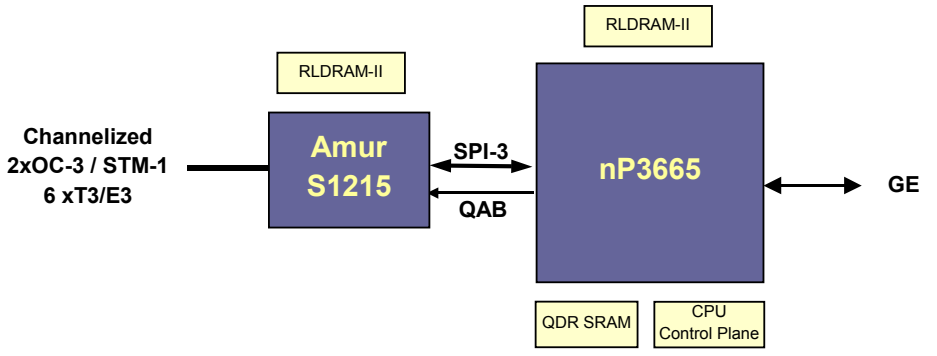
Industry Leading Integration and Performance

The nP3665 is an OC-24/2GE network processing and traffic management solution. In addition to high-performance packet processing and fine-grained traffic management, the nP3665 includes specialized coprocessors that perform classification, policing, and coherent database management for unparalleled line-rate performance. The device is offered in different speed grades to provide a range of performance and cost options tuned to the application.

Rapid Application Development

AMCC's nPsoft™ development environment speeds the development, debugging, and delivery of feature-rich, wire-speed, Layer 2-7 applications by combining the simplified nPcore™ programming model of all AMCC NPUs with open, layered nPsoft Services, advanced development tools, rich reference application libraries, and both simulation and real hardware-based development systems.

Because the nP3665 allows easy API access to on-chip coprocessors for complex tasks, customer differentiating features can be created faster and with fewer lines of code.



Example nP3665 Application

nP3665

nP3665 Highlights

Interfaces

- Flexible combination of cell and packet Line Interfaces:
  - OIF SPI-3 (8/32-bit modes)
  - ATM Forum UTOPIA-2,16-bit, 50 MHz
  - Up to two GE ports with integrated MAC
- Combined with Amur/Tigris devices, supports deeply Channelized HDLC/ATM applications up to 622 Mbps aggregate bandwidth: T3/E3, T1/E1, nxDS0, and so on
- External Memory Interfaces:
  - ECC supported on all external memories
  - Shared Payload and Context memories in RLDRAM-II bank (1x36, 2x18, 4x9 configurations) operating at up to 300 MHz
  - Shared ingress CSM/Flow database in QDR SRAM memory bank (1x18 or 2x9 configurations) operating at up to 250 MHz
- External Search Interface
  - Compliant with NPF
  - Backward compatibility mode with existing TCAMs
- CPU Interfaces: PowerPC and Fast Ethernet
- Debug port
- JTAG port

High Performance nPcore

- One nPcore at up to 700 MHz
- 30% relative performance increase compared to nP3700 (Instruction/packet)

Typical Power Dissipation[1]

- @400 MHz: 3.6 W
- @550 MHz: 3.9 W
- @700 MHz: 4.2 W

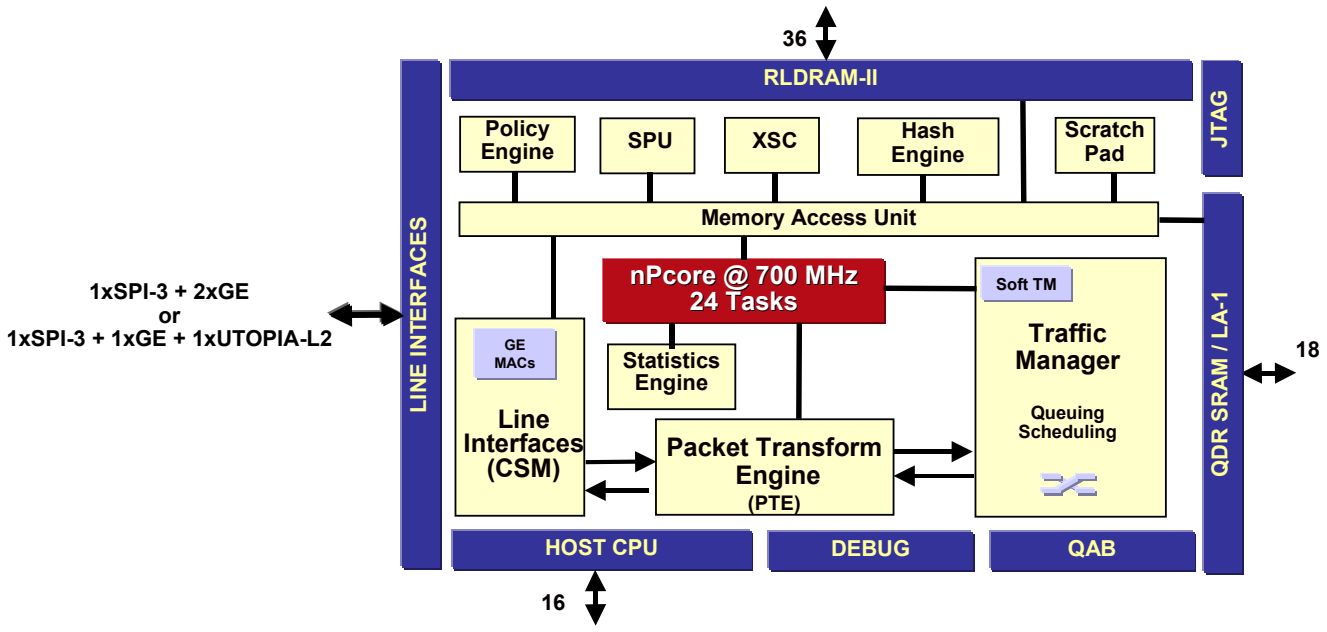
Integrated Coprocessors

- Policy Engine for efficient packet classification
- Special Purpose Unit (SPU) for per-flow policing
- Hashing Unit
- On-Chip Debugger (OCD)

Integrated Traffic Manager

- Hierarchical Traffic Manager with fine-grained flow-based traffic management
- Leverages field-proven nPX5710 and nPX5720 technology

1. See the *nP3665 Application Note — Power and Board Space Requirements (nP 2006-0030)* for more information.



nP3665 Block Architecture

nPcore Architecture

AMCC's software programmable nPcores are built from the ground up for both packet- and cell-based networking data-plane operations. The nP3665 supports up to OC-24 / 2-Gbps operation utilizing one nPcore with 24 separate tasks which are all available for either ingress or egress processing. The nPcore implements zero-cycle task switching and zero-cycle branching for enhanced performance.

The nPcore is surrounded by on-chip coprocessing engines to accelerate sophisticated network processing functions, such as packet classification, route and context searching, statistics gathering, metering, policing, and packet transformations. The nPcore, in combination with these on-chip coprocessing engines, implements a Network Instruction Set Computing (NISC) Architecture. This NISC architecture dramatically reduces the number of lines of code required to implement many advanced networking tasks.

A key addition to the fifth generation of NISC architecture is the exception channel processing that provides flexibility in handling packets that require increased processing time. This exception channel handles special packets through a secondary path, without affecting the deterministic line-rate performance of the regular packets in the primary path. Another key addition to the fifth generation architecture is the Channel Service Memory that enables deep channelization in the line interfaces at all packet sizes and can handle very large bursts in the incoming traffic without affecting line-rate performance.

Single-Stage, Single-Image Programming

AMCC's nPcore architecture implements a simple single-stage programming model. In this model, each cell or packet is processed in its entirety, from start to finish, by a single task in the nPcore. With this single-stage model, the entire data flow algorithm can be created as a single complete software program, just as it would be on a non-multiprocessor system, allowing the same program image to be executed identically by each task of the nPcore. This approach greatly simplifies programming while optimizing performance.

Traffic Management

The traffic management block in the nP3665 leverages AMCC's expertise and technology from the nPX5700 family of traffic managers.

The nP3665 implements a hierarchical scheduling architecture to provide multiple levels of bandwidth provisioning and per-subscriber guarantees. This hierarchy consists of the following logical levels: flow, pipe, subport, and port.

Additionally, the nP3665 expands the nP3700 Traffic Manager hierarchy to support subflow Classes of Service functionality, providing a fifth level of scheduling hierarchy for additional service-level QoS flexibility. Minimum and maximum bandwidth control can be configured on multiple levels. WFQ and Strict Priority scheduling algorithms are also implemented by the traffic management block. For ATM applications, non-real-time and real-time CBR and VBR connections can be configured for a desired subset of flows.

The nP3665 Traffic Manager is implemented in hardware for guaranteed performance, unlike software-based traffic managers that eat into the available instruction budget.

Input Admission Control

Sophisticated cell and packet admission controls are configurable in the nP3665. This includes execution of standard discard mechanisms such as WRED, EPD, and TPD in hardware, or the option to perform variations in software.

Application Software

The nP3665 application software includes AAL2, AAL5, IPv4, and IPv6 for mobile infrastructure access applications.

nP3665

Specifications

Network Processing

Configurations

- Flexible POS and ATM system interfaces
  - One SPI-3 (8- or 32-bit) providing OC-12 speed-up to/from external devices
  - Up to 48 channels on the SPI-3 interface
  - One ATM Forum UTOPIA-2 interface
  - Up to two GE ports with built-in MAC and GMII/TBI interfaces
  - 10/100 Ethernet Interface for Line or Host CPU
- Supports 1xGE to 1x UTOPIA-2 configuration
- Supports SPI-3 to 2xGE
- Deep Channelization support to AMCC Tigris/Amur
  - Allows fractional T3/E3, T1/E1 and nxDS0 logical channels

nPcore Performance

- One nPcore running at 400 MHz, 550 MHz, or 700 MHz
- 24 tasks
- 128 KB instruction space, 32K instructions
- Dynamic Task Allocation
- Zero Cycle Task Switching

Integrated Coprocessors

- Policy Engine — Efficient packet classification
- SPU — Data coherency
  - Enables Single and Dual Leaky Bucket and Token Bucket policing on cells and frames, MEF-compliant policing
- Hash Engine — Programmable engine to accelerate table lookups
  - Programmable Polynomial (for example, CRC generation)
- Statistics Engine
  - Programmable Statistics Collection

Traffic Management

- Standard Discard Mechanisms
  - WRED
  - Dynamic queue limits
  - EPD and CLP marking
- Payload memory requirements
  - Up to 2 million cells of storage
  - RLDRAM-II
- Supports DiffServ
- Per-flow queuing and scheduling
  - 128K ingress and egress flows
    - Strict Priority, Min, WRR
    - Rate-shaping (CBR, VBR)
  - Up to eight sub-flow Classes of Service provide an additional level of scheduling hierarchy
  - 2K pipes
    - Rate-shaping, Strict Priority, Min, Weight, Max
  - 512 subports
    - Min, Max, WRR

nPsoft Development Environment

nPsoft Services

- Simplified multiprocessor programming model
- Powerful NPU and CPU software and messaging framework
- nPkernel NPU operating system
- Open APIs, tracking standards

nP Workbench-3665

- Software development system
- Modular interfaces

nPsoft Application Libraries

- Reference source code for WAN and LAN protocols

nPsoft Toolkit

- Code development tools
- Graphical simulators
- Customizable debugger
- Performance analysis

Product Availability

- Part Number: nP3665PB*x-yyy*
  - *x*: C – Commercial, I – Industrial
  - *yyy*: 400 – 400 MHz, 550 – 550 MHz, 700 – 700 MHz
- Commercial and Industrial Temperature Rating
- Availability: Now

AMCC

215 Moffett Park Drive
Sunnyvale, CA 94089
P 858 450 9333
F 858 450 9885
www.amcc.com

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