



nP3750

5-Gbps Network Processor with Integrated Traffic Manager

Features

Supports 5-Gbps Traffic

- nP⁵ Technology
- Mix and match Gigabit Ethernet, POS, and ATM traffic
- Standalone or as a line card in a larger system

Proven nPcore Architecture

- 3 nPcores at 700 MHz optimized for network processing
- Single-stage single-image programming model
- High-speed RLD RAM-II memory interfaces for payload and context storage
- Per-flow metering and statistics for millions of flows

Integrated Traffic Manager

- Per-flow queuing and scheduling
- Sophisticated, fine-grained scheduling algorithms

Standards-Compliant Interfaces

- Integrated GE MACs (GMII)
- OIF SPI-3, OIF SPI-4 Phase 2

Applications

- VoIP/media Gateways
- DSLAM
- Core, Edge Routers
- WLAN ENterprise access
- L4-L7 Applications

Benefits

- High integration: Significant form factor, cost, and power savings
- Hardware-based Traffic Manager for guaranteed performance
- Software compatibility with nP32xx, nP345x, nP36xx, nP37xx, and nP7250
- Simple programming model for rapid development and quick time-to-market
- Software portability

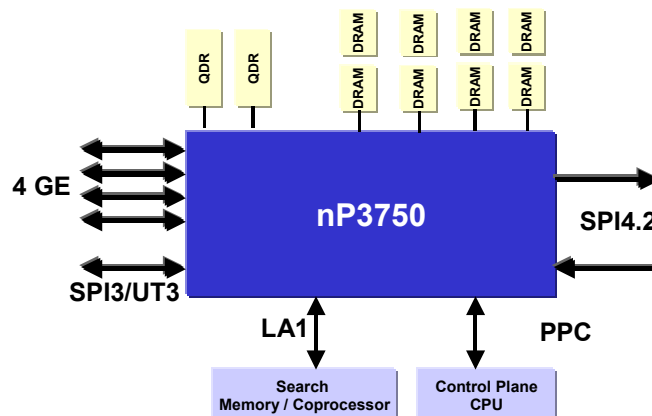
The nP3750 integrated network processor is a derivative of the nP3700 family, the first network processor family to incorporate the latest nP⁵™ technology. Developed over several generations of traffic management and network processor products, nP⁵ unites the flexibility of the industry's highest performance network processing nPcore with the most widely deployed and mature traffic management technology. This unique combination enables developers to deliver extremely fine-grained control of subscriber traffic, without impacting the ability to perform complex protocol inter-working at media speeds. The nP3750 is designed from the ground up to provide software compatibility with the earlier generations of AMCC Network Processors. The single-stage programming model dramatically simplifies software development and troubleshooting and enables quickest time-to-market.

Industry Leading Integration and Performance

The nP3750 is an Ethernet-focused version of the nP3700 5-Gbps network processor. In addition to high-performance packet processing and fine-grained traffic management, the nP3750 includes four embedded Ethernet MACs, specialized coprocessors that perform classification, policing, and coherent database management for unparalleled line-rate performance. The nP3750 supports high-performance memory interfaces such as RLD RAM-II and QDR-II SRAM. The devices are offered in different speed grades to provide a range of performance and cost options tuned to the application.

Rapid Application Development

AMCC's nPsoft™ development environment speeds the development, debugging, and delivery of feature-rich, wire-speed, Layer 2-7 applications by combining the simplified nPcore™ programming model of all AMCC NPUs with open, layered nPsoft Services, advanced development tools, rich reference application libraries, and both simulation and real hardware-based development systems. Because the nP3750 allows easy API access to on-chip coprocessors for complex tasks, customer differentiating features can be created faster and with fewer lines of code.



nP3750 Interface Diagram

nP3750

nP3750 Highlights

Interfaces

- Line Interfaces – cell and packet

	SPI-3/UT-3	GE	SPI-4.2
nP3750	1	4	1

- Fabric Interface: OIF SPI-4 Phase 2
 - 800 MHz
- External Memory Interfaces: RLD RAM II memory controllers
 - Payload Memory: Two banks of 36-bit RLD RAM II operating at up to 250 MHz (32 Gbps with ECC)

- Context Memory: Two banks of 36-bit RLD RAM II operating at up to 250 MHz (32 Gbps with ECC)
- Channel Service Memory: One bank of 36-bit QDR-II SRAM operating at up to 250 MHz
- Flow Database Memory: Two banks of 18-bit QDR-II SRAM operating at up to 250 MHz
- CPU Interfaces: PowerPC and Gigabit Ethernet
- External Search Interface
 - Compliant with NPF
 - Backward compatibility mode with existing TCAMs
- Debug port
- JTAG port

High Performance nPcore

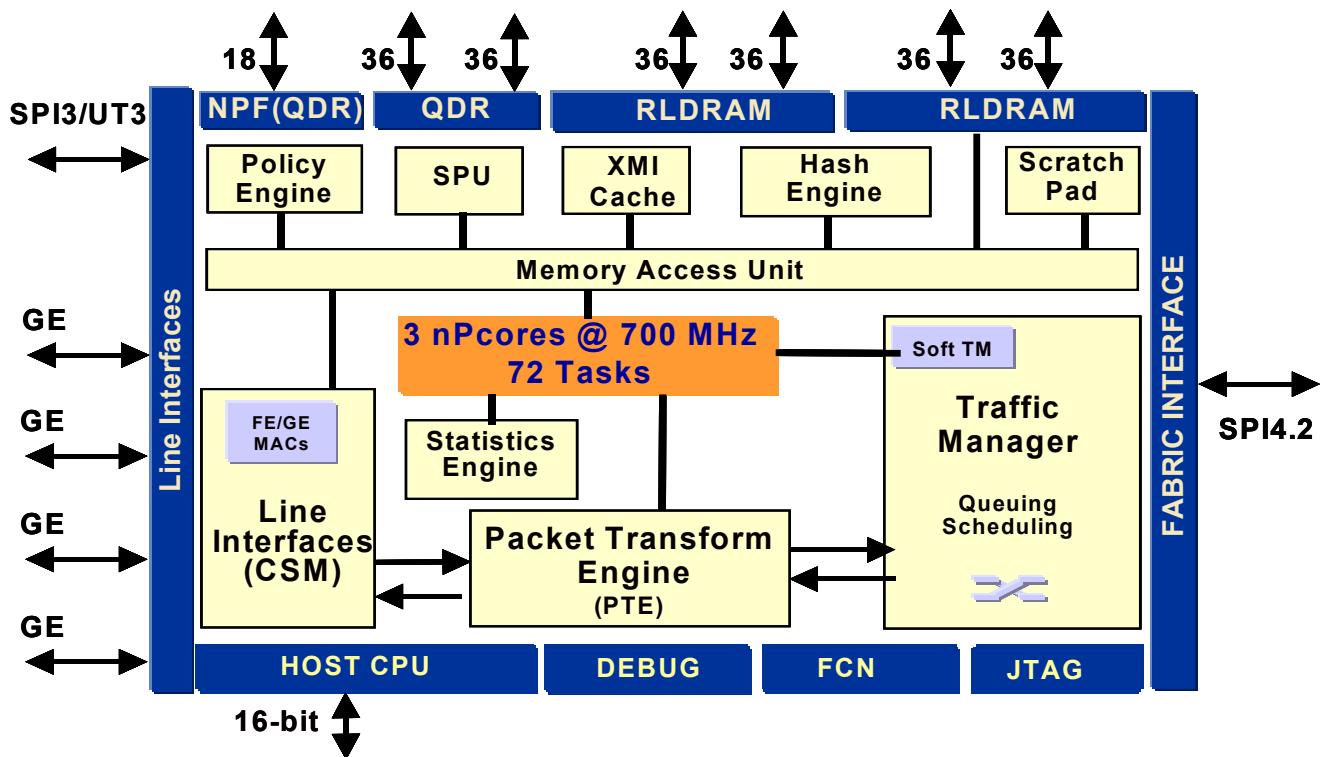
- Three nPcores at up to 700 MHz

Integrated Coprocessors

- Policy Engine for efficient packet classification
- Special Purpose Unit (SPU) for per-flow policing
- Hashing Unit
- On-Chip Debugger (OCD)

Integrated Traffic Manager

- Hierarchical Traffic Manager with fine-grained flow-based traffic management
- Leverages field-proven nPX5710 and nPX5720 technology



nP3750 Block Diagram

nPcore Architecture

AMCC's software programmable nPcores are built from the ground up for both packet- and cell-based networking data plane operations. The nP3750 supports 5-Gbps full-duplex operation utilizing a cluster of three nPcores. Each nPcore has 24 separate tasks, yielding a total of 72, which are all available for either ingress or egress processing. The nPcores implement zero-cycle task switching and zero-cycle branching for enhanced performance.

The nPcores are surrounded by on-chip coprocessing engines to accelerate sophisticated network processing functions, such as packet classification, route and context searching, statistics gathering, metering, policing, and packet transformations. The nPcores, in combination with these on-chip coprocessing engines, implement Network Instruction Set Computing (NISC) Architecture. This NISC architecture dramatically reduces the number of lines of code required to implement many advanced networking tasks.

A key addition to the nP37xx architecture is the exception channel processing that provides flexibility in handling packets that

require increased processing time. This exception channel handles special packets through a secondary path, without affecting the deterministic line-rate performance of the regular packets in the primary path. The addition of a special preprocessor, the Channel Service Module (CSM), offers a store-and-forward capability to nP37xx architecture. The CSM is able to buffer incoming traffic according to the level of channelization of the line interfaces. A sizable CSM buffer absorbs very large bursts in the incoming traffic without data losses.

Single-Stage, Single-Image Programming

AMCC's nPcore architecture implements a simple single-stage programming model. In this model each cell or packet is processed in its entirety, from start to finish, by a single task in a single nPcore. With this single-stage model, the entire data flow algorithm can be created as a single complete software program, just as it would be on a non-multiprocessor system, allowing the same program image to be executed identically by each task on each nPcore. This approach greatly simplifies programming while optimizing performance.

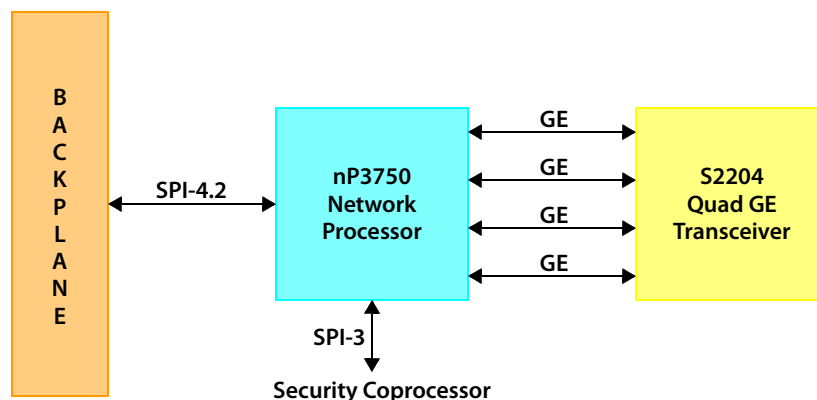
Traffic Management

The traffic management block in the nP3750 leverages AMCC's expertise and technology from the nPX5700 family of traffic managers.

The nP3750 implements a hierarchical scheduling architecture to provide multiple levels of bandwidth provisioning and per-subscriber guarantees. This hierarchy consists of four logical levels: flow, pipe, subport and port. Minimum and maximum bandwidth control can be configured on multiple levels. WFQ and Strict Priority scheduling algorithms are also implemented by the traffic management block. For ATM applications, non-real-time and real-time CBR and VBR connections can be configured for a desired subset of flows.

Input Admission Control

Sophisticated cell and packet admission controls are configurable in the nP3750. This includes execution of standard discard mechanisms such as WRED, EPD, and TPD in hardware or the option to perform variations in software.



WLAN Enterprise Access Appliance Solution

nP3750

Specifications

Network Processing

Configurations

- POS and ATM
 - 4xGE, SPI-3, SPI-4.2
 - Any type of OC-*n* channelization
 - Flexible bandwidth allocation
For example, Full-duplex OC-48, OC-12 plus 12xOC-3
- Ethernet
 - 10/100/1000 Ethernet Interface for Line or Host CPU
 - Flexible bandwidth provisioning per user/per CoS
 - Dynamic bandwidth reuse
 - Highly granular flow control

nPcore Performance

- Three nPcores running at up to 700 MHz
- 24 tasks per nPcore, total 72 tasks
- 64 KB instruction space, 16K instructions
- Dynamic Task Allocation
- Zero Cycle Task Switching

Integrated Coprocessors

- Policy Engine — Efficient packet classification
- SPU — Data coherency
 - Enables Single and Dual Leaky Bucket and Token Bucket policing on cells and frames
- Hash Engine — Programmable engine to accelerate table lookups
 - Programmable Polynomial (for example, CRC generation)
- Statistics Engine
 - Atomic Programmable Statistics Collection

Traffic Management

- Standard Discard Mechanisms
 - WRED
 - Dynamic queue limits
 - EPD and CLP marking
- Payload memory requirements
 - Up to 2 million cells of storage
 - RLDRAM-II
- Supports DiffServ
- Per-flow queuing and scheduling:
 - 128K ingress and egress flows
 - Strict Priority, Min, WRR
 - Rate-shaping (CBR, VBR)
 - Up to 64K flows may participate in Flow Priority Queue grouping where four egress flows are scheduled within the group according to pre-assigned weight
 - 4K pipes
 - Strict Priority, Min, Weight, Max, XON/XOFF
 - 512 subports
 - Min, Max, WRR, XON/XOFF
 - 64 subport groups
 - Max bandwidth capping, XON/XOFF

nPsoft Development Environment

nPsoft Services

- Simplified multiprocessor programming model
- Powerful NPU and CPU software and messaging framework
- nPkernel NPU operating system
- Open APIs, tracking standards

nP Workbench-3750

- Software development system
- Modular interfaces

nPsoft Application Libraries

- Reference source code for WAN and LAN protocols

nPsoft Toolkit

- Code development tools
- Graphical simulators
- Customizable debugger
- Performance analysis

Product Availability

- Part Number: nP3750PBx-yyy (x: C – Commercial, I – Industrial, yyy: 700 – 700 MHz)
- Availability: Now
- Commercial and Industrial Temperature Rating



215 Moffett Park Drive
Sunnyvale, CA 94089
P 858 450 9333
F 858 450 9885
www.amcc.com

For technical support, please call 1-800-840-6055 or 858-535-6517, or email support@amcc.com.

AMCC reserves the right to make changes to its products, its datasheets, or related documentation, without notice and warrants its products solely pursuant to its terms and conditions of sale, only to substantially comply with the latest available datasheet. Please consult AMCC's Term and Conditions of Sale for its warranties and other terms, conditions and limitations. AMCC may discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information is current. AMCC does not assume any liability arising out of the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others. AMCC reserves the right to ship devices of higher grade in place of those of lower grade.

AMCC SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

AMCC is a registered trademark of Applied Micro Circuits Corporation. PowerPC and the PowerPC logo are registered trademarks of IBM Corporation. All other trademarks are the property of their respective holders. Copyright © 2006 Applied Micro Circuits Corporation. All Rights Reserved.

NP3750PBx_PB_v1.1_20060428