

MOS FIELD EFFECT TRANSISTOR NP36P04SDG

SWITCHING P-CHANNEL POWER MOSFET

DESCRIPTION

The NP36P04SDG is P-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
NP36P04SDG-E1-AY Note		Tana 0500 n/mal		
NP36P04SDG-E2-AY Note	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK)	

Note Pb-free (This product does not contain Pb in external electrode.)

FEATURES

Super low on-state resistance

 $R_{\text{DS(on)1}}$ = 17.0 m Ω MAX. (VGs = -10 V, ID = -18 A)

 $R_{\text{DS(on)2}}$ = 23.5 m Ω MAX. (VGs = -4.5 V, ID = -18 A)

• Low input capacitance

Ciss = 2800 pF TYP.

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

VDSS	-40	V
Vgss	∓20	V
D(DC)	∓36	А
D(pulse)	∓108	А
P _{T1}	56	W
Pt2	1.2	W
Tch	175	°C
Tstg	-55 to +175	°C
las	26	А
Eas	67	mJ
	VGSS ID(DC) ID(pulse) PT1 PT2 Tch Tstg IAS	VGSS ∓20 Ib(DC) ∓36 Ib(pulse) ∓108 PT1 56 PT2 1.2 Tch 175 Tstg -55 to +175 IAS 26

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

<R>

2. Starting T_{ch} = 25°C, V_{DD} = -20 V, R_G = 25 Ω , V_{GS} = $-20 \rightarrow 0$ V

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	2.68	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	125	°C/W

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The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.



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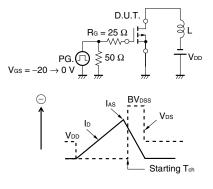
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Idss	V _{DS} = -40 V, V _{GS} = 0 V			-10	μA
Gate Leakage Current	lgss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	Vds = Vgs, Id = -250 <i>µ</i> A	-1.0	-1.6	-2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = -10 V, I _D = -18 A	12	23		S
Drain to Source On-state Resistance Note	RDS(on)1	Vgs = -10 V, Id = -18 A		12.5	17.0	mΩ
	RDS(on)2	V _{GS} = -4.5 V, I _D = -18 A		15.4	23.5	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V,		2800		pF
Output Capacitance	Coss	V _{GS} = 0 V,		450		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		280		pF
Turn-on Delay Time	td(on)	V _{DD} = -20 V, I _D = -18 A,		8		ns
Rise Time	tr	V _{GS} = -10 V,		10		ns
Turn-off Delay Time	td(off)	Rg = 0 Ω		250		ns
Fall Time	tr			140		ns
Total Gate Charge	QG	$V_{DD} = -32 V,$		55		nC
Gate to Source Charge	Q _{GS}	V _{GS} = -10 V,		7		nC
Gate to Drain Charge	QGD	I⊳ = –36 A		15		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I⊧ = –36 A, V₀s = 0 V		0.95	1.5	V
Reverse Recovery Time	trr	I⊧ = –36 A, V₀s = 0 V,		44		ns
Reverse Recovery Charge	Qrr	di/dt = −100 A/ <i>µ</i> s		51		nC

ELECTRICAL CHARACTERISTICS (TA = 25°C)

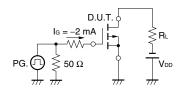
Note Pulsed test PW \leq 350 μ s, Duty Cycle \leq 2%

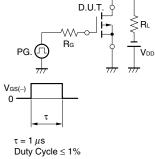
TEST CIRCUIT 1 AVALANCHE CAPABILITY

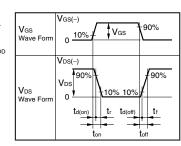
TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

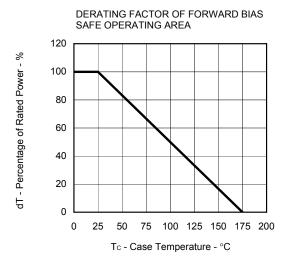


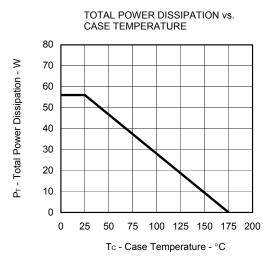




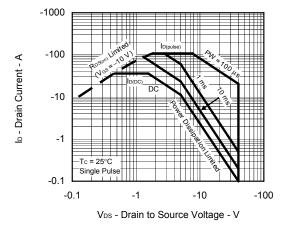
Data Sheet D19074EJ2V0DS

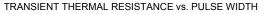
TYPICAL CHARACTERISTICS (TA = 25°C)

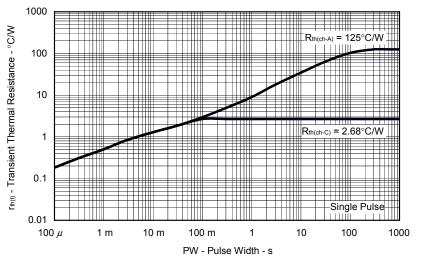




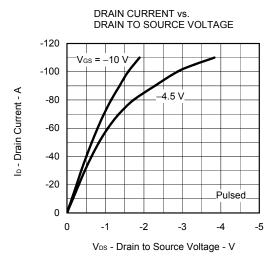




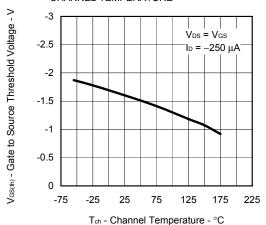


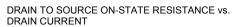


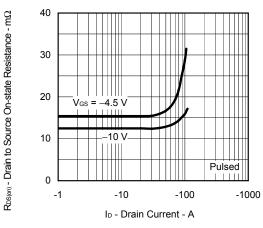
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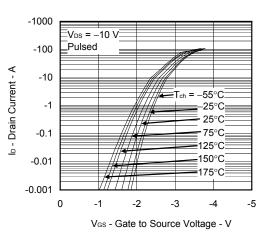






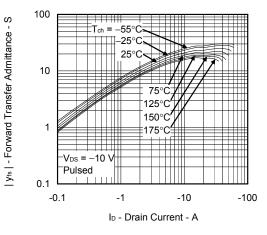


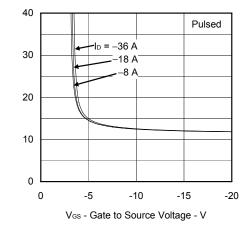




FORWARD TRANSFER CHARACTERISTICS

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT





DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

4

Data Sheet D19074EJ2V0DS

 $R_{DS(on)}$ - Drain to Source On-state Resistance - m Ω



10

1

-0.1

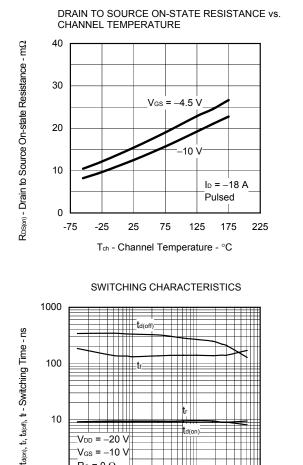
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ID - Drain Current - A

VDD = -20 V

V_{GS} = -10 V

 $R_G = 0 \Omega$

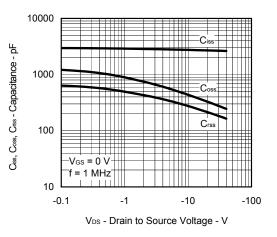


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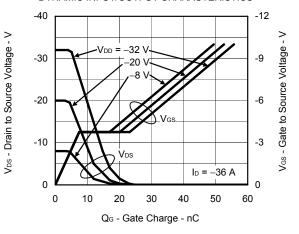
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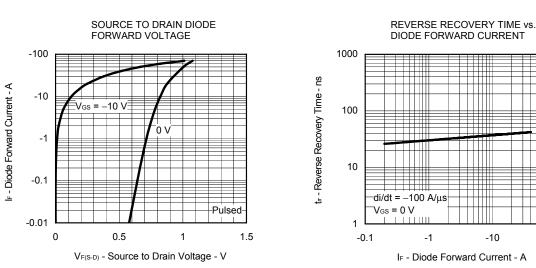
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CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS





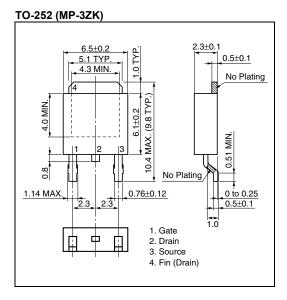
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Data Sheet D19074EJ2V0DS

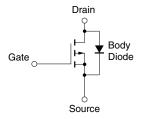
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-10

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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