DATA SHEET

MOS FIELD EFFECT TRANSISTOR
NP36N055HLE, NP36N055ILE, NP36N055SLE

SWITCHING
N-CHANNEL POWER MOSFET

DESCRIPTION

These products are N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

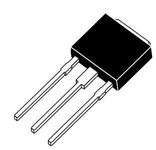
- Channel temperature 175 degree rated
- Super low on-state resistance
  $R_{DS(on)1}$ = 13 mΩ MAX. (V_{GS} = 10 V, I_D = 18 A)
  $R_{DS(on)2}$ = 16 mΩ MAX. (V_{GS} = 5 V, I_D = 18 A)
- Low C_{iss} : C_{iss} = 2900 pF TYP.
- Built-in gate protection diode

★ ORDERING INFORMATION

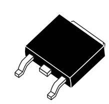
PART NUMBER	PACKAGE
NP36N055HLE	TO-251 (JEITA) / MP-3
NP36N055ILE Note	TO-252 (JEITA) / MP-3Z
NP36N055SLE	TO-252 (JEDEC) / MP-3ZK

Note Not for new design.

(TO-251)



(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	55	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±36	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±144	A
Total Power Dissipation (T_A = 25°C)	P_T	1.2	W
Total Power Dissipation (T_C = 25°C)	P_T	120	W
Single Avalanche Current Note2	I_{AS}	36 / 33	A
Single Avalanche Energy Note2	E_{AS}	12 / 108	mJ
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to + 175	°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 → 0 V (See Figure 4.)

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.25	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	°C/W

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Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

Document No. D14156EJ4V0DS00 (4th edition)
Date Published July 2005 NS CP(K)
Printed in Japan

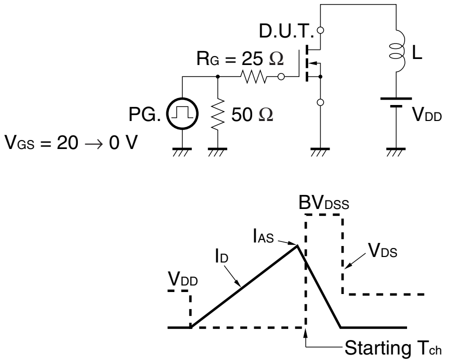
The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

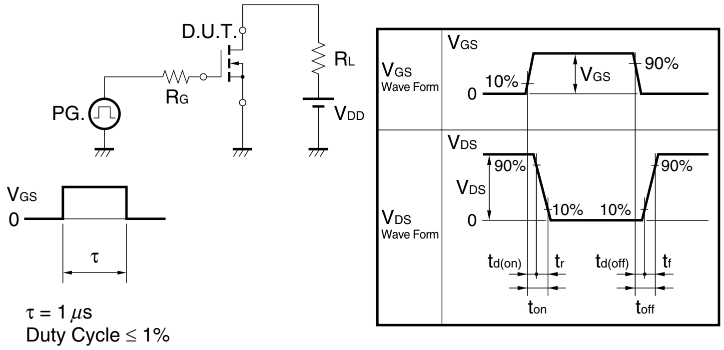
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5	2	2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = 10 V, I_D = 18 A	11	23		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 18 A		10	13	mΩ
	$R_{DS(on)2}$	V_{GS} = 5 V, I_D = 18 A		12	16	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.5 V, I_D = 18 A		13	18	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V		2900	4400	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		370	560	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		180	330	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 28 V, I_D = 18 A		22	48	ns
Rise Time	t_r	V_{GS} = 10 V		14	36	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 1 Ω		69	140	ns
Fall Time	t_f			12	29	ns
Total Gate Charge	Q_{G1}	V_{DD} = 44 V, V_{GS} = 10 V, I_D = 18 A		53	80	nC
	Q_{G2}	V_{DD} = 44 V		30	45	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 5 V		9		nC
Gate to Drain Charge	Q_{GD}	I_D = 18 A		15		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 36 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 36 A, V_{GS} = 0 V		42		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		60		nC

Note Pulsed

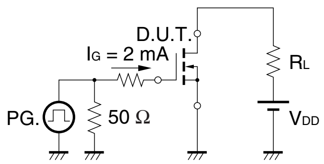
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

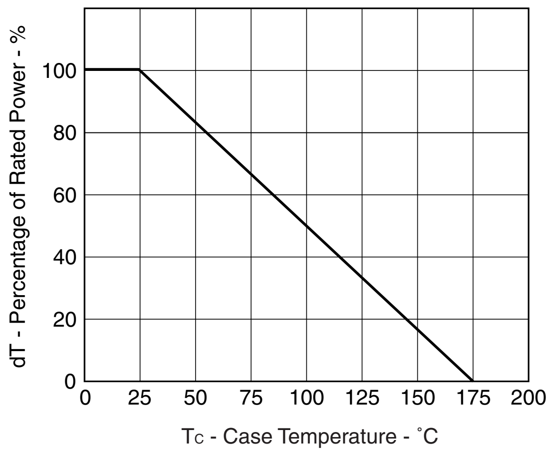


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

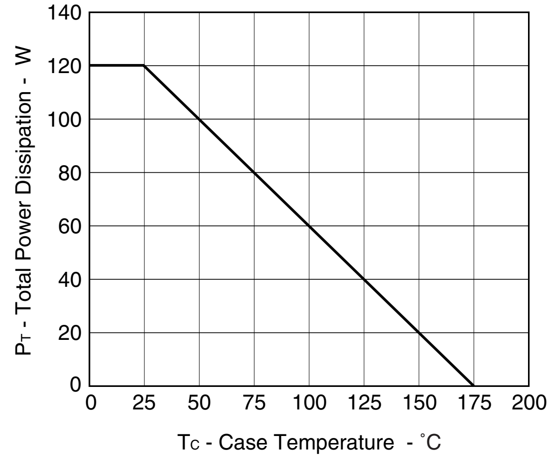


Figure3. FORWARD BIAS SAFE OPERATING AREA

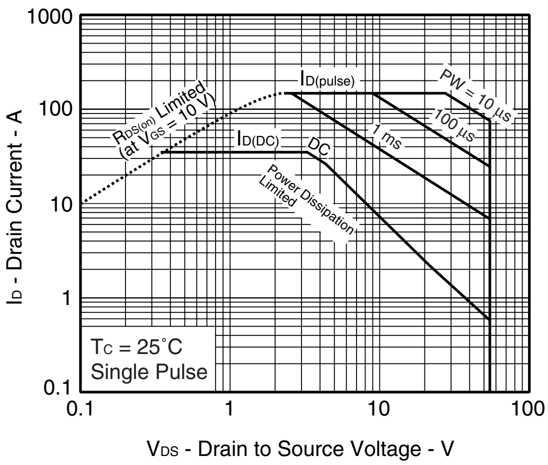


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

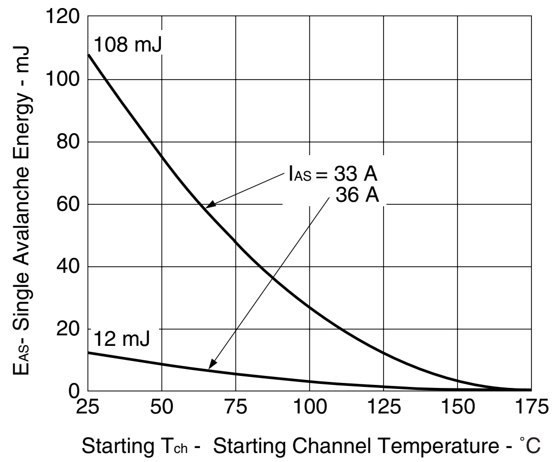
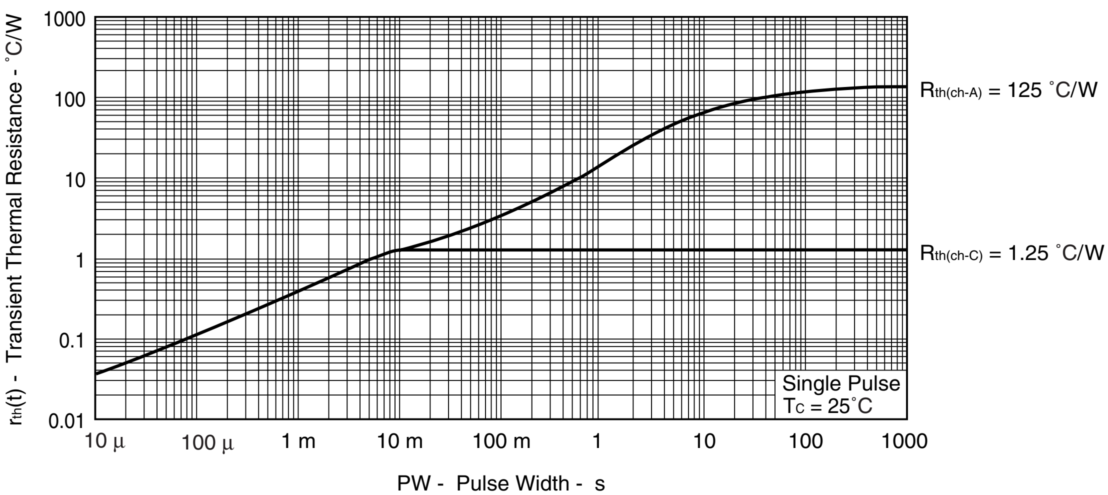


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



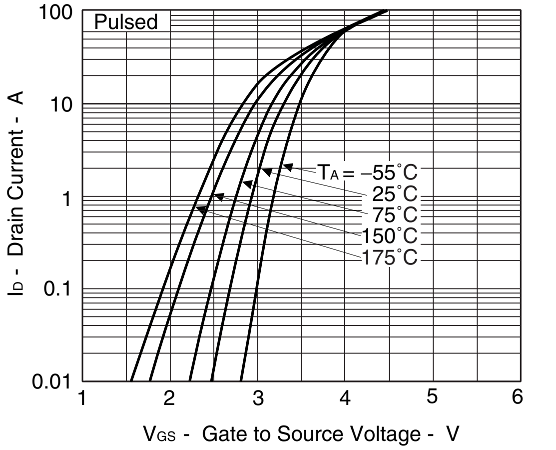


Figure6. FORWARD TRANSFER CHARACTERISTICS

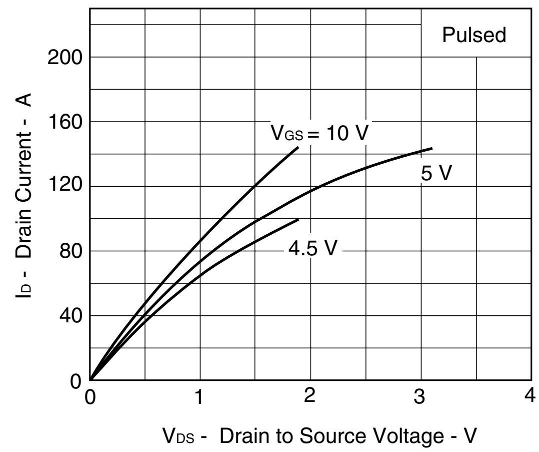


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

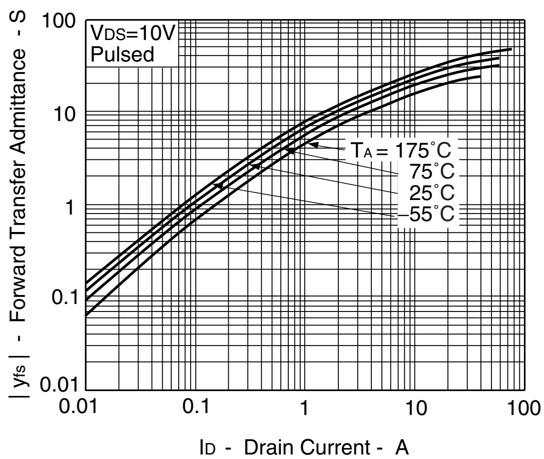


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

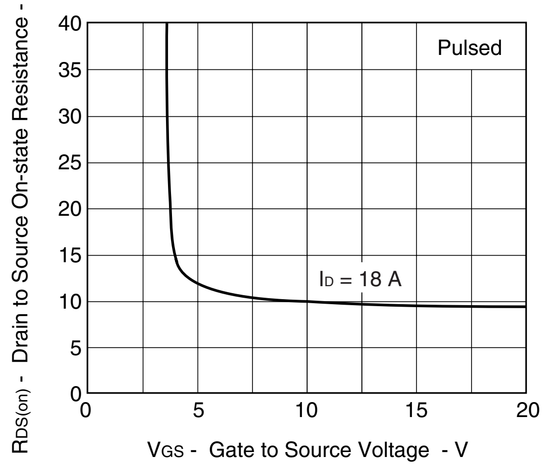


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

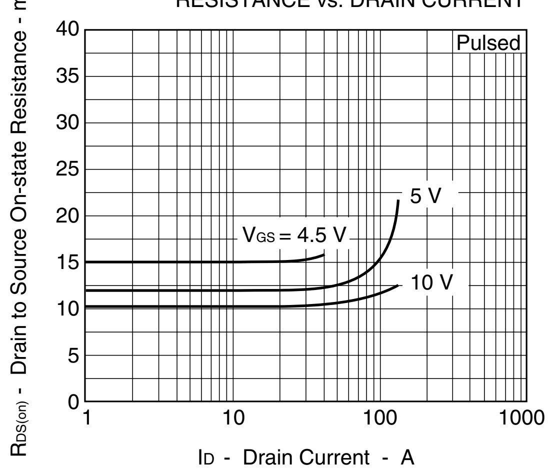


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

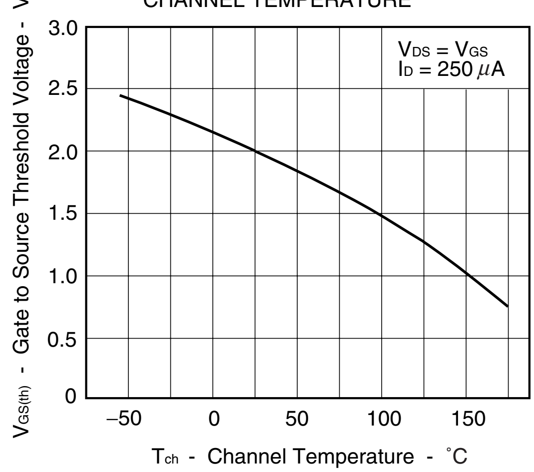


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

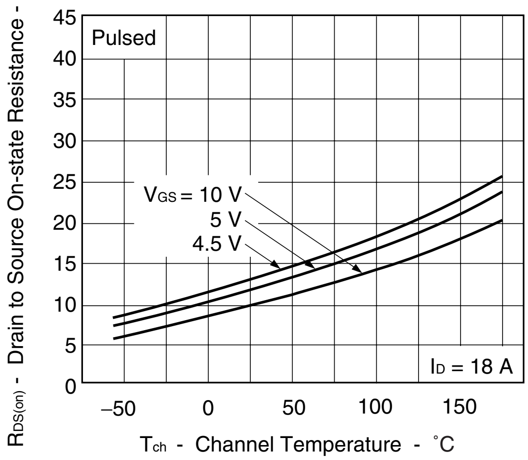


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

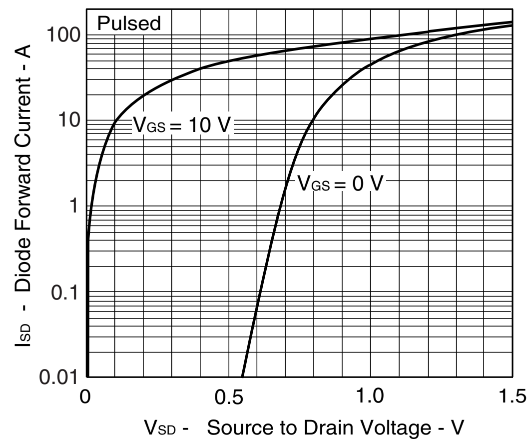


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

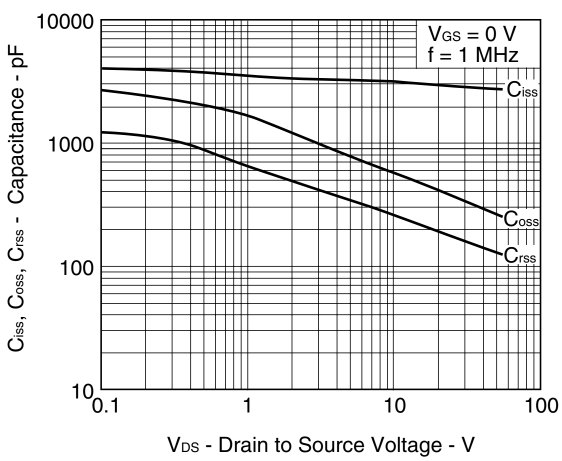


Figure15. SWITCHING CHARACTERISTICS

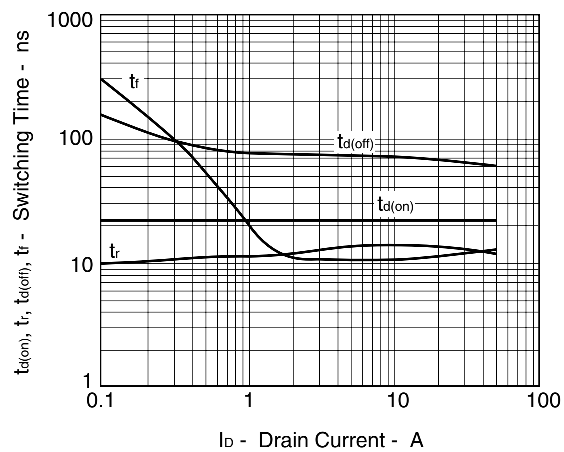


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

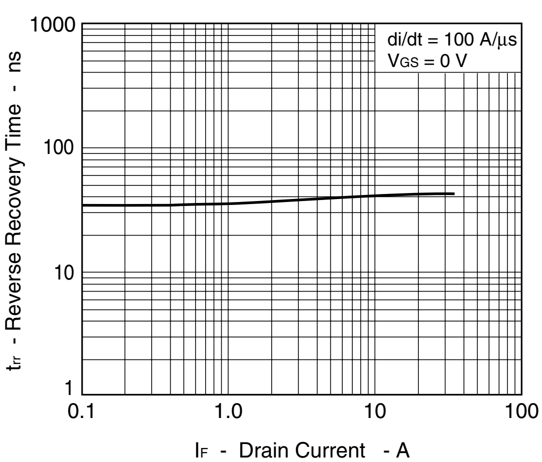
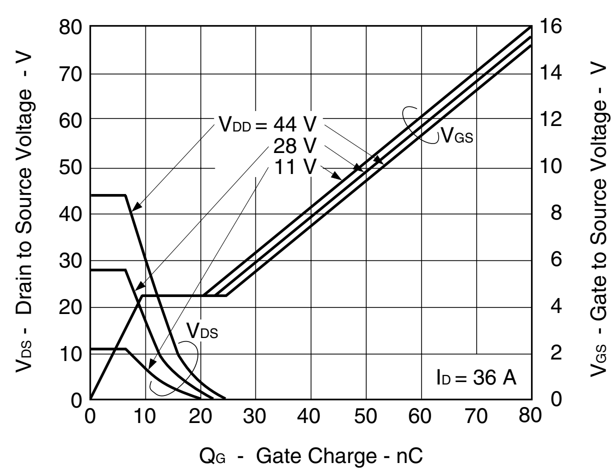
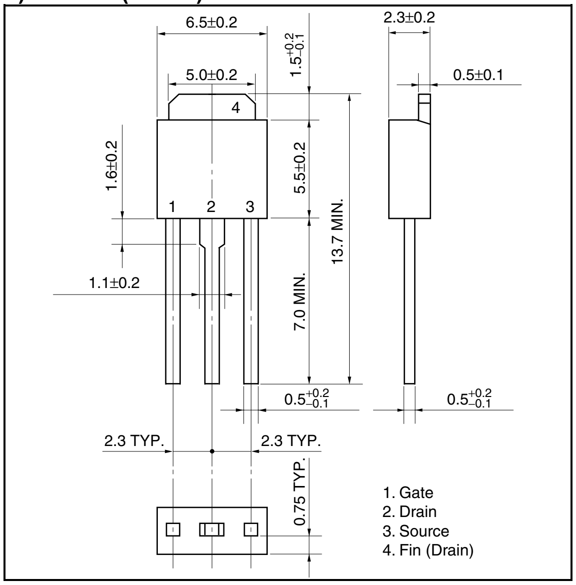


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

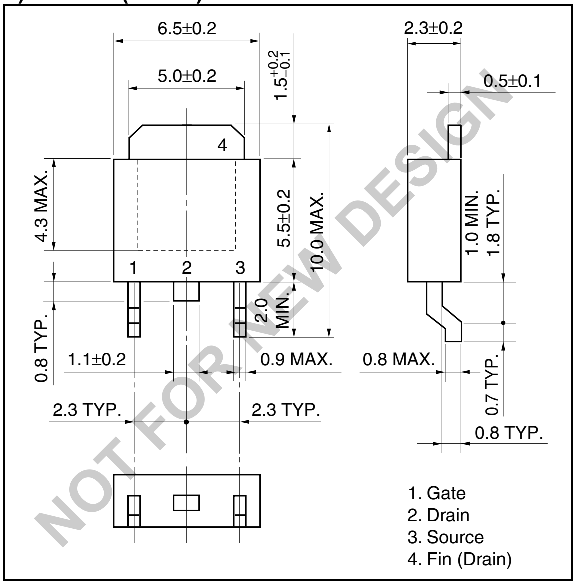


★ PACKAGE DRAWINGS (Unit: mm)

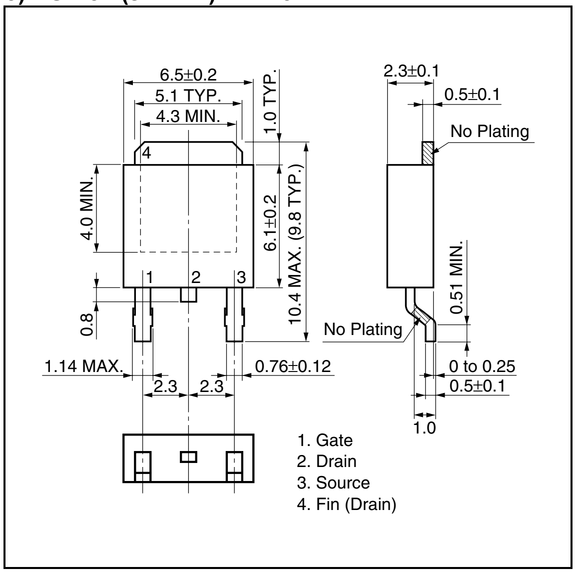
1) TO-251 (JEITA) / MP-3



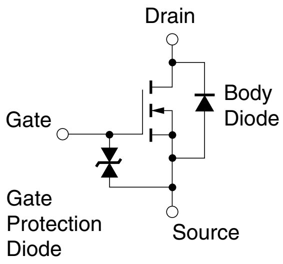
2) TO-252 (JEITA) / MP-3Z



3) TO-252 (JEDEC) / MP-3ZK



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

M8E 02. 11-1