

MOS FIELD EFFECT TRANSISTOR

NP34N055SHE

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The NP34N055SHE is N-channel MOS Field Effect Transistor designed for high current switching applications.

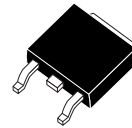
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP34N055SHE	TO-252 (MP-3ZK)

FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance
 $R_{DS(on)} = 19 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 17 \text{ A)}$
- Low C_{iss} : $C_{iss} = 1600 \text{ pF TYP.}$
- Built-in gate protection diode

(TO-252)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	55	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 34	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 136	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	88	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	34/27/10	A
Single Avalanche Energy ^{Note2}	E_{AS}	11/72/100	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$ (Refer to **Figure 4.**)

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.70	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

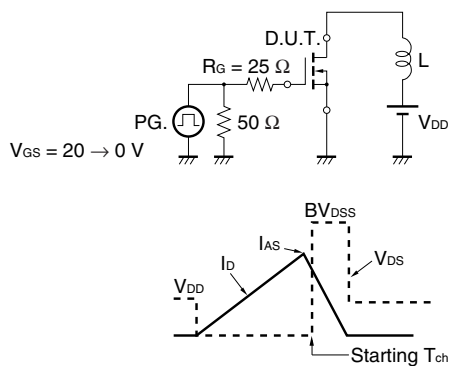
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

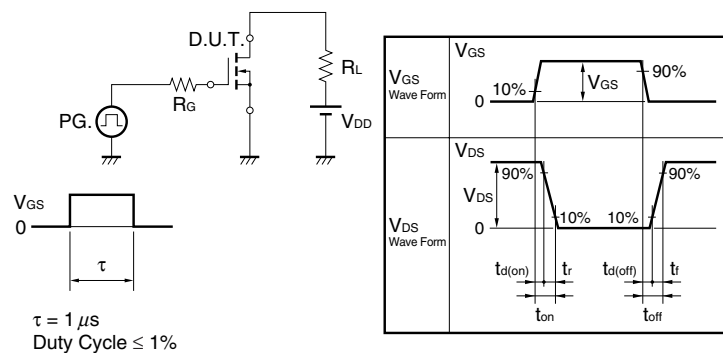
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 55 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 17 A	6	12		S
Drain to Source On-state Resistance Note	R _{DS(on)}	V _{GS} = 10 V, I _D = 17 A		15	19	mΩ
Input Capacitance	C _{iss}	V _{DS} = 25 V		1600	2400	pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		250	380	pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		120	220	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 28 V, I _D = 17 A		21	47	ns
Rise Time	t _r	V _{GS} = 10 V		15	38	ns
Turn-off Delay Time	t _{d(off)}	R _G = 1 Ω		35	70	ns
Fall Time	t _f			12	29	ns
Total Gate Charge	Q _G	V _{DD} = 44 V		30	45	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		9		nC
Gate to Drain Charge	Q _{GD}	I _D = 34 A		12		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 34 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 34 A, V _{GS} = 0 V		40		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		58		nC

Note Pulsed

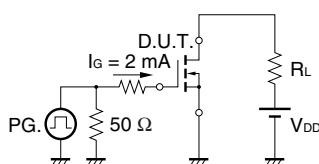
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

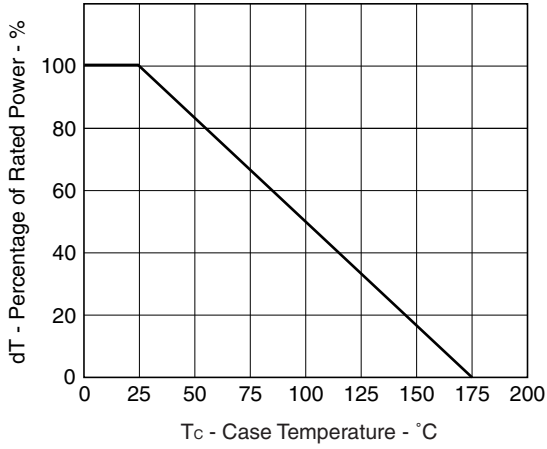


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

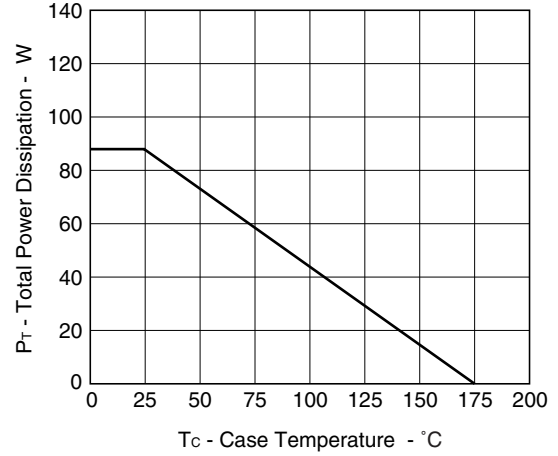


Figure3. FORWARD BIAS SAFE OPERATING AREA

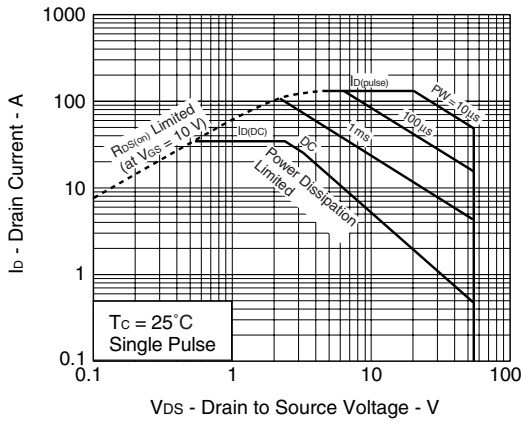


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

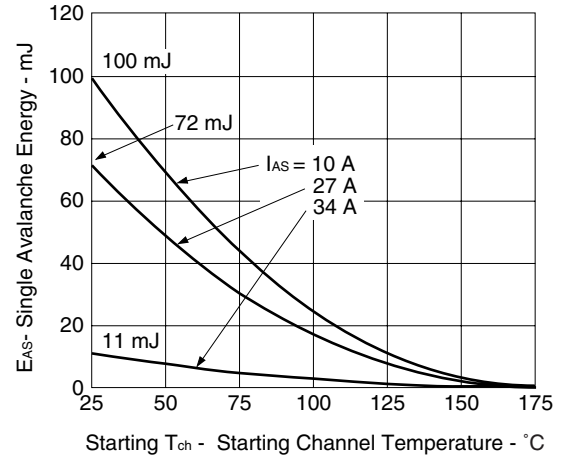


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

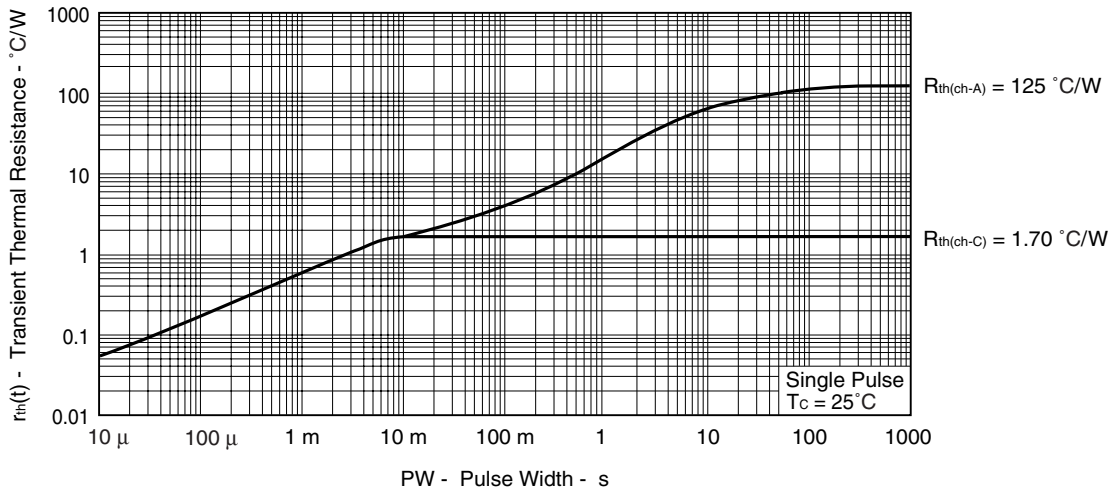


Figure6. FORWARD TRANSFER CHARACTERISTICS

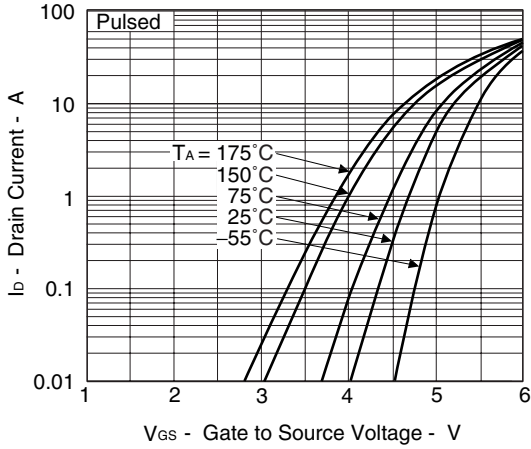


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

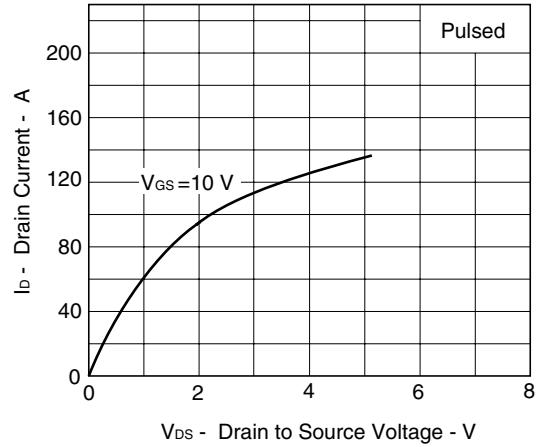


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

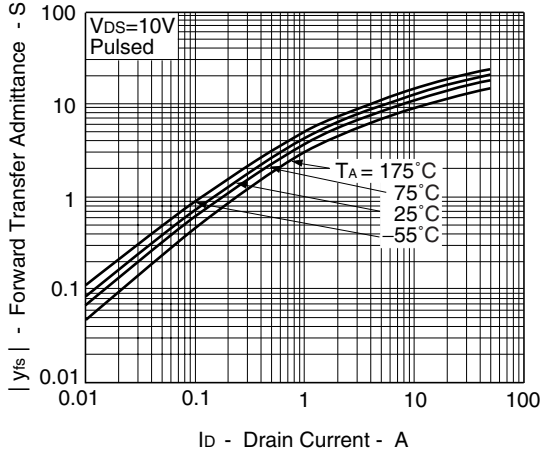


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

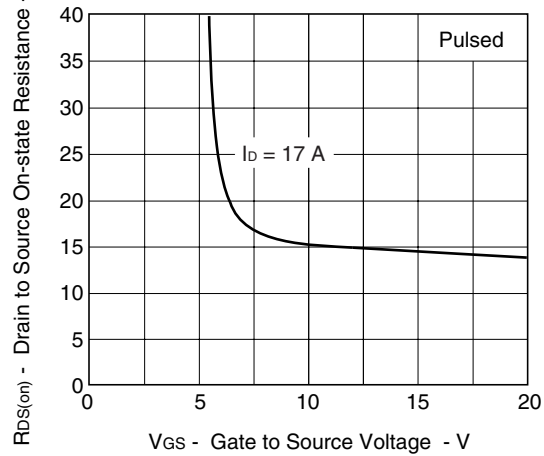


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

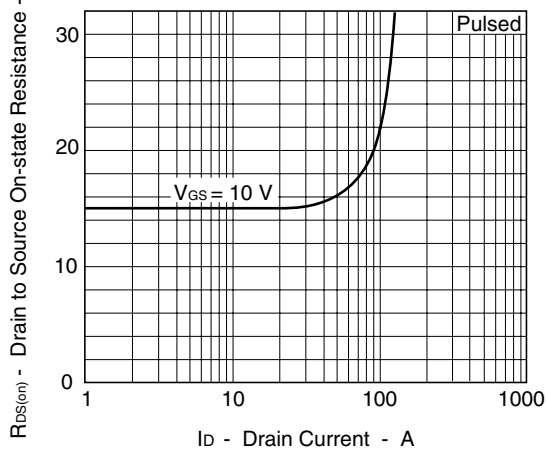


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

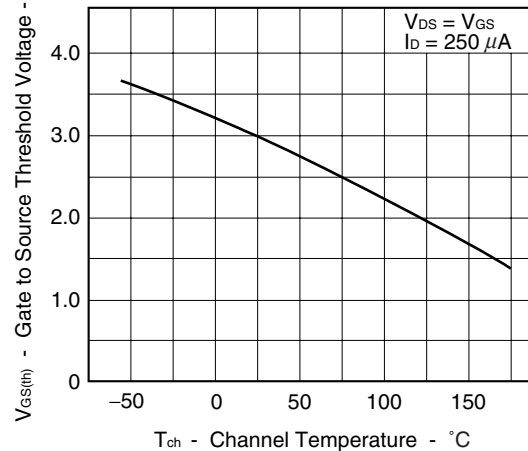


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

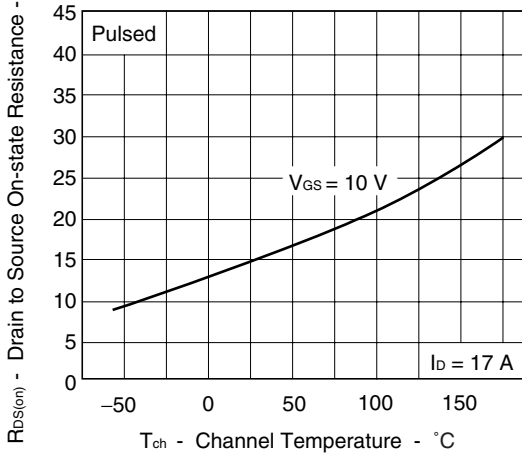


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

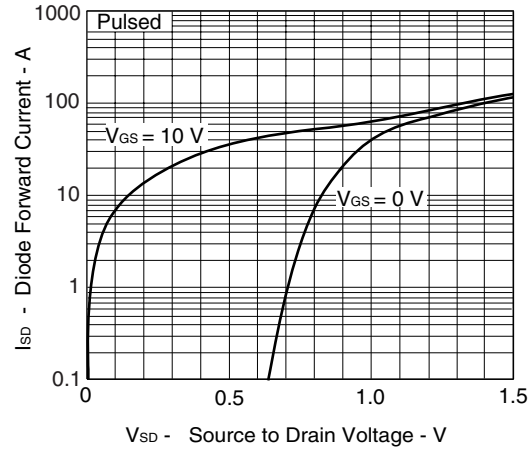


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

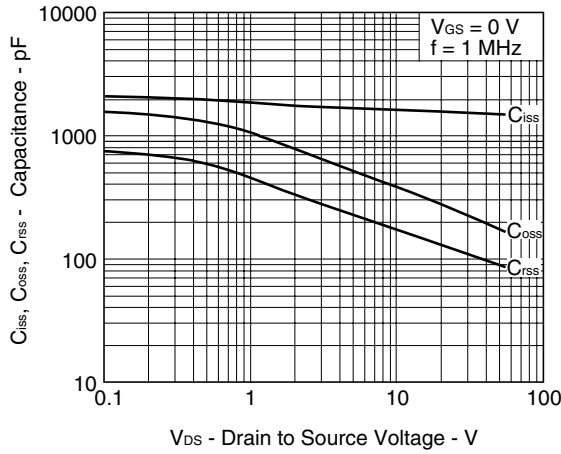


Figure15. SWITCHING CHARACTERISTICS

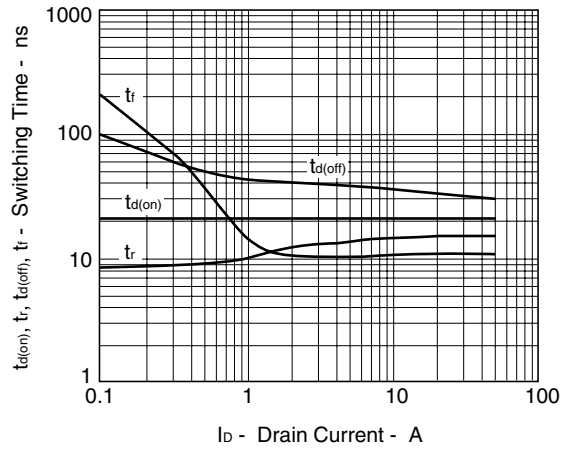


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

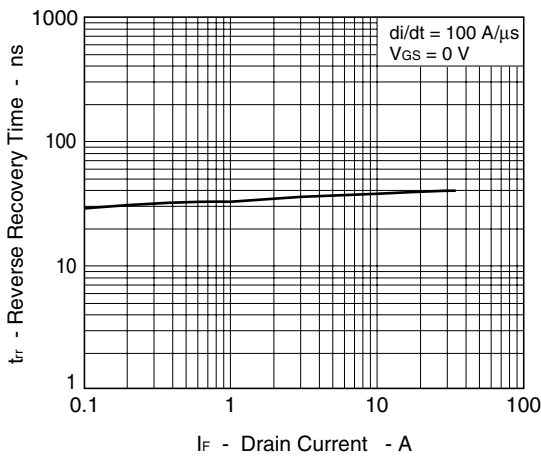
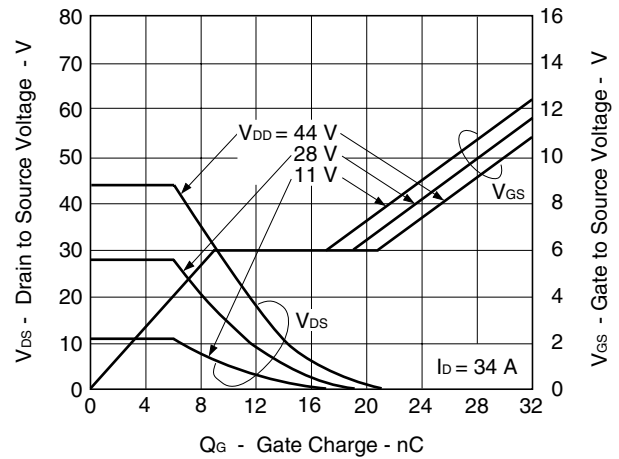
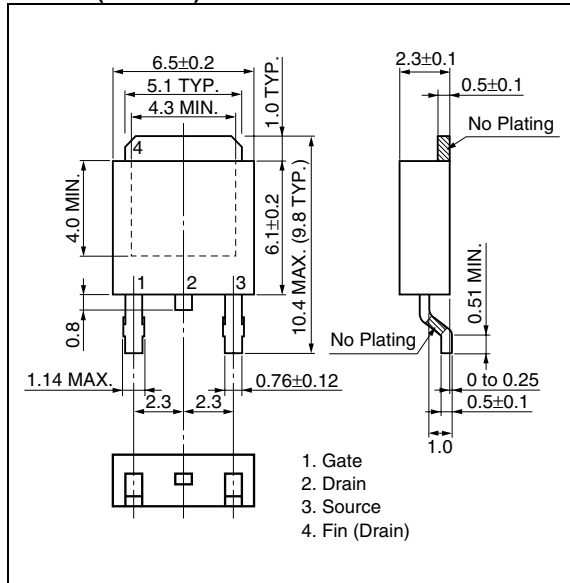


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

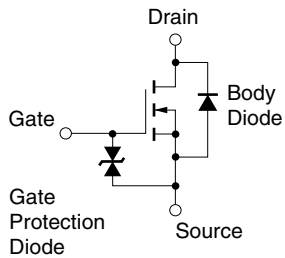


PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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