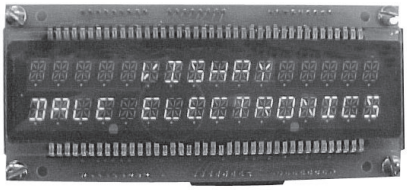
Intelligent Plasma Display



Vishay Dale's APD-32A025A is a 32 character microprocessor controlled display system. It's field of 32 quarter inch (0.65cm) characters (in 2 rows of 16) provides a compact yet highly legible display.

The APD-32A025A supplies signals to scan and decode keyboards up to 64 keys, and can also interface to 8 bit microprocessors via it's 8 bit bi-directional data bus. It's internal character generator provides 64 ASCII symbols which can be blinked, scrolled left or right and entered left to right or right to left. It also has a user enabled cursor which is either fully addressable or auto incremented and decremented.

Only two connectors are required, for data and power.

OPTICAL SPECIFICATIONS

Light Output : 60 ft./lamberts typical
Color: Neon orange
Viewing Area: 4.45" x 0.7"
Viewing Angle: 130°
Character Height: 0.25"
Character Spacing: 0.28" on centers
Row Spacing: 0.45" on centers

FEATURES

- 32 Characters, 14 segment alphanumeric (2 rows of 16 characters each)
- Plasma glow (gas discharge)
- Refresh memory
- 64 ASCII character set, internally generated
- Decodes and debounces up to 64-key keyboards
- 8 bit, three state, bi-directional data bus
- Operates from signal 5V power supply
- User enabled blinking cursor
- Cursor addressable or auto incremented/decremented
- User enabled blinking display
- Compact size, L x H x D ÷ 5.2″ x 2.3″ x 2.3″
- 60 ft./lambert light output (typical)
- Neon orange color

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature: 0°C to + 60°C

Storage Temperature: - 20°C to + 70°C

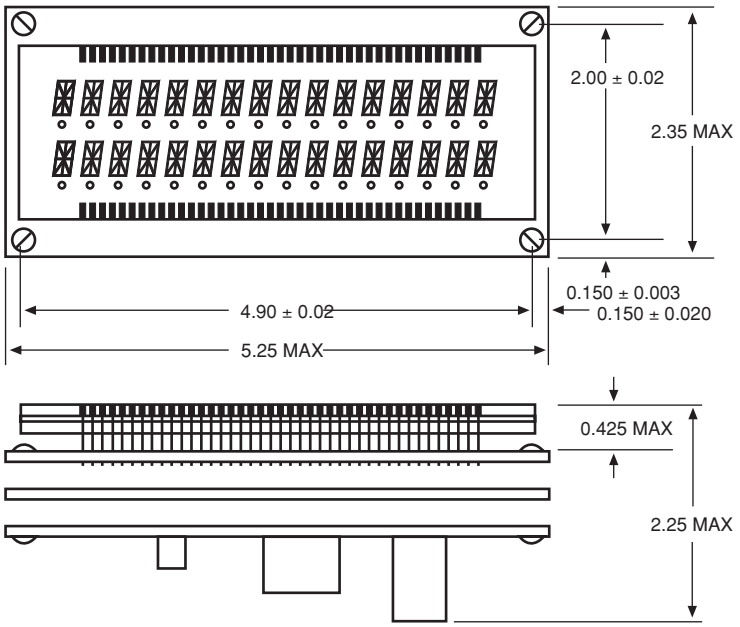
Voltage on Any Pin vs. Ground: - 0.3 to + 5.25

Input Voltage (Power Supply): 5V

Vibration: 0.018 (0.046cm) inch displacement amplitude from 10 to 50Hz, 2G acceleration from 50 to 2000Hz logarithmic sweep rate, 30 minutes duration along each of the three major axes.

Shock (Impact): 50G 1⁄2 sine wave 11.0 msec duration, 5 shocks in each of the 6 directions.

DIMENSIONS in inches [millimeters]



STANDARD ELECTRICAL SPECIFICATIONS

D.C. and Operating Characteristics

DESCRIPTION	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Low Voltage (All)	V_{il}	- 0.5	—	+ 0.8	V
Input High Voltage (All Except $\overline{RESET}$)	V_{ih}	+ 2.0	—	V_{cc}	V
Input High Voltage ($\overline{RESET}$)	V_{ih2}	+ 3.0	—	V_{cc}	V
Output Low Voltage (D_0 - D_{07})	V_{ol}	—	—	+ 0.45	V
Output Low Voltage (All Except $\overline{EOC}$)	V_{ol2}	—	—	+ 0.45	V
Output Low Voltage ($\overline{EOC}$)	V_{ol3}	—	—	+ 0.45	V
Output High Voltage (D_0 - D_{07})	V_{oh}	+ 2.4	—	—	V
Output High Voltage (All Other Outputs)	V_{oh1}	+ 2.4	—	—	V
Input Leakage Current $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A_0	I_{il}	—	—	± 10	µA
Output Leakage Current (D_0 - D_{07}), High Z State)	I_{ol}	—	—	- 10	µA
V_{dd} Supply Current (STBY)	I_{dd}	—	+ 10	+ 25	mA
Total Supply Current	$I_{cc\ STBY}$ + I_{cc}	—	+ 750	+ 1000	mA
Low Input Source Current KI0-3	V_{li1}	—	—	+ 0.4	mA
Low Input Source Current $\overline{RESET}$	V_{li2}	—	—	+ 0.2	mA

T_A = 0°C TO 55°C, Vcc = V_{ccstby} = + 5V ± 5%

STANDARD ELECTRICAL SPECIFICATIONS

A.C. Characteristics

DESCRIPTION	SYMBOL	MIN.	TYP.	MAX.	UNITS
$\overline{CS}$, A_0 Setup to $\overline{RD}\downarrow$	T_{ar}	0	+ 100	—	ns
$\overline{CS}$, A_0 Hold after $\overline{RD}\uparrow$	T_{ra}	0	- 25	—	ns
$\overline{RD}$ Pulse Width	T_{rr}	+ 250	+ 280	2 x T_{cy}	ns
$\overline{CS}$, A_0 to Data Out Delay	T_{ad}	—	+ 200	+ 225	ns
$\overline{RD}\downarrow$ to Data Out Delay	T_{rd}	—	+ 200	+ 225	ns
$\overline{RD}\uparrow$ to Data Float Delay	T_{rdf}	+ 10	—	+ 100	ns
		—	+ 120	—	ns
Recovery Time Between Reads and/or Write	T_{rv}	+ .300	+ 1	—	µS
Cycle Time	T_{cy}	+ 2.5	+ 2.5	—	µS
Write					
$\overline{CS}$, A_0 Setup to $\overline{WR}\downarrow$	T_{aw}	0	+ 50	—	ns
$\overline{CS}$, A_0 Hold after $\overline{WR}\uparrow$	T_{wa}	0	+ 40	—	ns
$\overline{WR}$ Pulse Width	T_{ww}	+ 250	+ 280	2 x T_{cy}	ns
Data Setup to $\overline{WR}\uparrow$	T_{dw}	+ 150	+ 200	—	ns
Data Hold after $\overline{WR}\uparrow$	T_{wd}	0	0	—	ns

T_A = 0°C TO 55°C, Vcc = V_{ccSTBY} = + 5V ± 5%.

PIN DESCRIPTION

PIN	SIGNAL	DESCRIPTION
J1		
A	GND	Ground (-).
B	V_{cc}	+ 5vdc ± 5%.
C	$V_{cc\ STBY}$	+ 5vdc ± 5% for standby operation (used to shutdown high voltage supply.) Connect to V_{cc} for normal operation.
J2		
1-4	KI1, KI3, KI0, KI2	Accepts timing input signals from keyboard.
5-8	KO2, KO1 KO3, KO0	Supplies timing output signals to keyboard.
9-16	D7-D0	Three state, bi-directional data bus lines - used to transfer data and commands between the master CPU and APD-32A025.
17	$\overline{WR}$	Write Strobe - used by master CPU to write data and commands into APD-32A025.
18	A0	Address Input - used by master CPU to command the APD-32A025A to put data on the bus for the CPU read (A0 = 0) or to test APD-32A025A busy flag (A0 — 1).
19	$\overline{RD}$	Read Strobe - used by master CPU to read data and status from the APD-32A025A internal registers.
20	$\overline{CS}$	Chip select - enables reading and writing to the APD-32A025.
21	GND	Ground.
22	$\overline{EOC}$	End of command (low pulse, 900 ns min width) - can be used to set a flat or to interupt the master CPU to indicate that the APD-32A025A has completed command execution.
23	GND	Ground.
24	KB IRQ	Keyboard flag from APD-32A025A to master CPU - indicates that a key has been depressed and that a key address is ready to be read by CPU.
25	GND	Ground
26	$\overline{RESET}$	Used to reset the APD-32A025A (upon low signal). All programmable APD-32A025A internal registers will be cleared. (Display refresh and keyboard scanning will stop)

A.C TEST CONDITIONS

D_7-D_0 Outputs: R_L = 2.2k to V_{ss}
4.3K to V_{cc}
C_L = 100pF

MATING CONNECTORS

J1 - Vishay Dale P/N 280108-01 or Molex P/N 08-50-0106 (terminals), 09-50-3031 (housing).
J2 - Vishay Dale P/N 280105-01 or Tyco AMP 746285-6.

RESET OPTION JUMPER W1

The APD-32A025A has a 3-pin jumper (W1) for selecting the source of the RESET signal. For most applications, the jumper should be set to INTERNAL by placing the shunt across the top 2 pins of the jumper. In some applications requiring compatibility with the earlier APD-32A025 model, the jumper should be set to EXTERNAL by placing the shunt across the bottom 2 pins of the jumper.

OPERATION PRINCIPLES

I/O Control

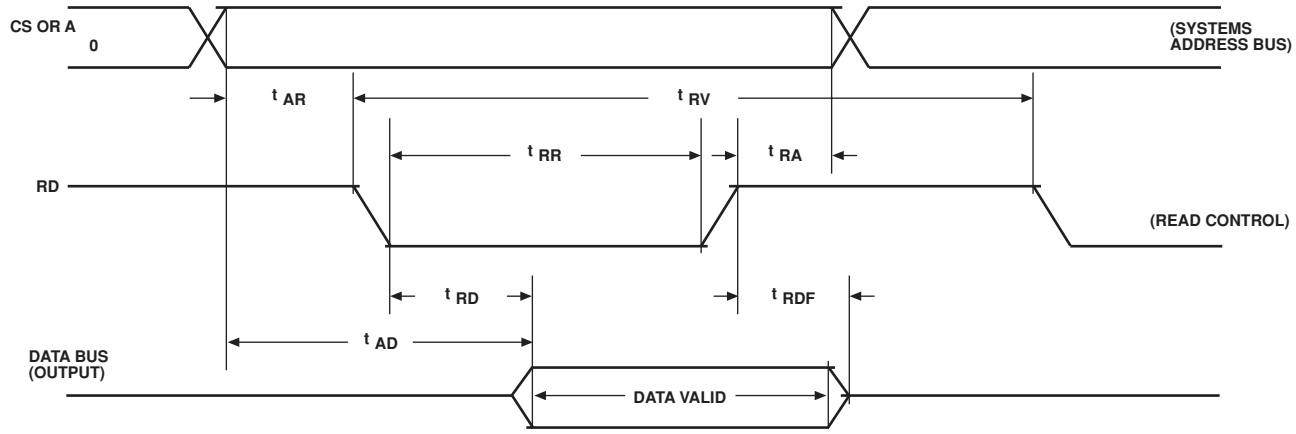
The I/O control section uses $\overline{CS}$, A0, $\overline{RD}$ and $\overline{WR}$ lines to control data to and from the internal APD-32A025A registers and buffers. The APD-32A025A has two 8-bit data registers (input and output) and an output busy flag F-F. All the data to and from the APD-32A025A is enabled by $\overline{CS}$.

The APD-32A025A input register is selected and written into by $\overline{CS}$, A0 = 0 and $\overline{WR}$. Note: 1 is not allowed for write operation.

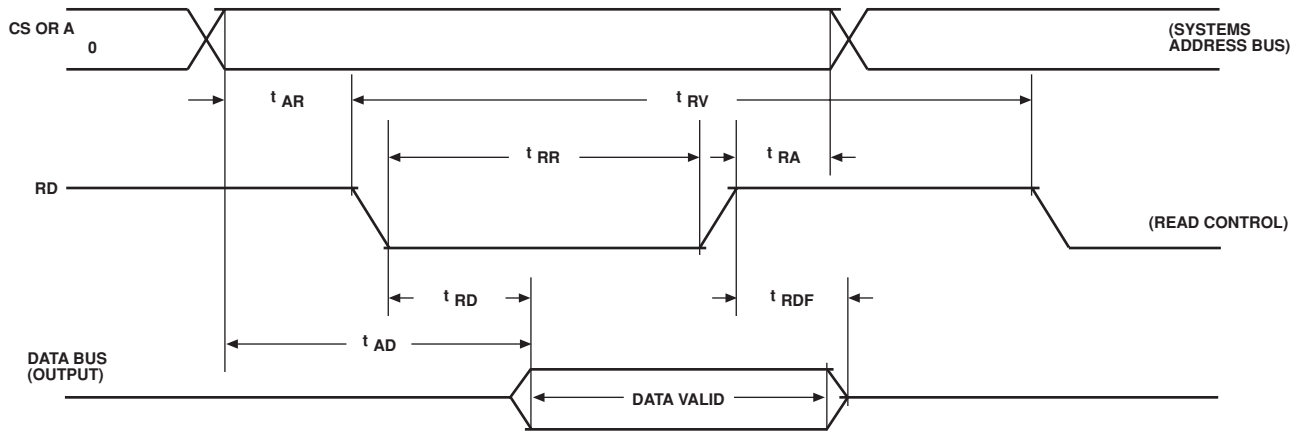
The master CPU can read either the APD-32A025A's output register or the 1 bit busy flag. The output register is selected and read by $\overline{CS}$, A0 = 0 and $\overline{RD}$. The busy flag is read (on data bus data bit 3) by $\overline{CS}$, A0 = 1 and $\overline{RD}$.

DIMENSIONS (WAVEFORMS)

READ OPERATION - OUTPUT AND FLAG REGISTER



WRITE OPERATION - INPUT REGISTER (A0 = 0)



MASTER CPU AND APD-32A025A DATA TRANSFER INTERFACE

The APD-32A025A can be easily interfaced to any 8-bit microprocessor in a number of ways. The memory mapped I/O is the simplest. The APD-32A025A is treated by the master CPU as a 2 location by 8-bit RAM. The master CPU can only write into memory location "0". It can read memory location "0" (data) or location "1" (busy flag).

The master CPU transfer commands to the APD-32A025A by writing into memory location "0". Immediately after receiving any command from the master CPU, the APD-32A025A will set the busy flag to "0" (data bus bit 3). The flag will remain "0" until the APD-32A025A has executed the given command. The master CPU can test the flag by reading memory location "1" and testing bit 3 for "1" (command execution finished). (All other bits are don't cares.)

At the end of any "GET" command the output register will be loaded with the requested data. The master CPU may read the output register at any time, however, the contents of the output will depend on the last completely executed "GET" command.

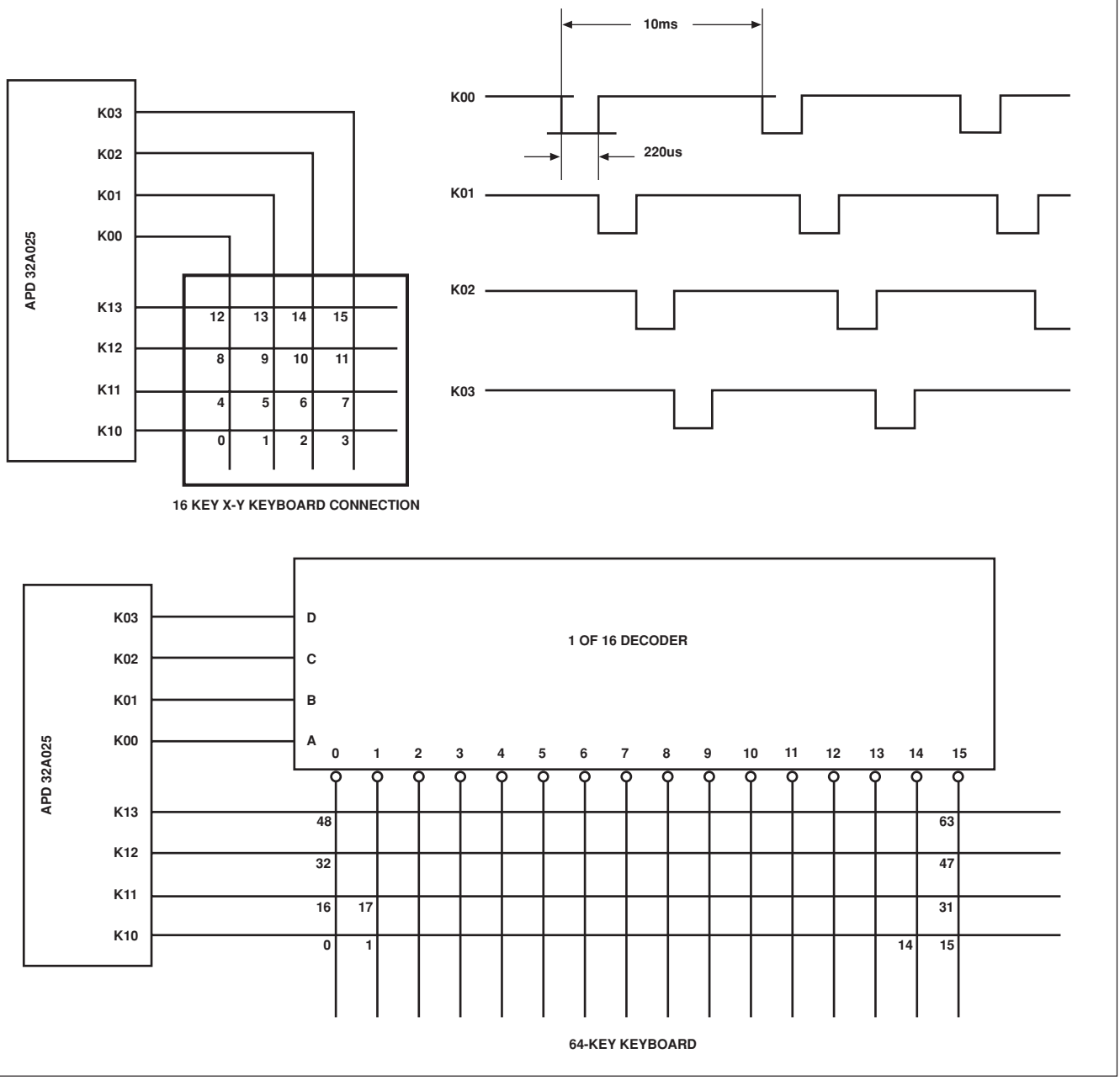
Note that the $\overline{EOC}$ line provides a low pulse (900 ns min.) indicating the end of command execution. This line can be used to set a flag or to interrupt the master CPU to indicate that the APD-32A025A has completed a command.

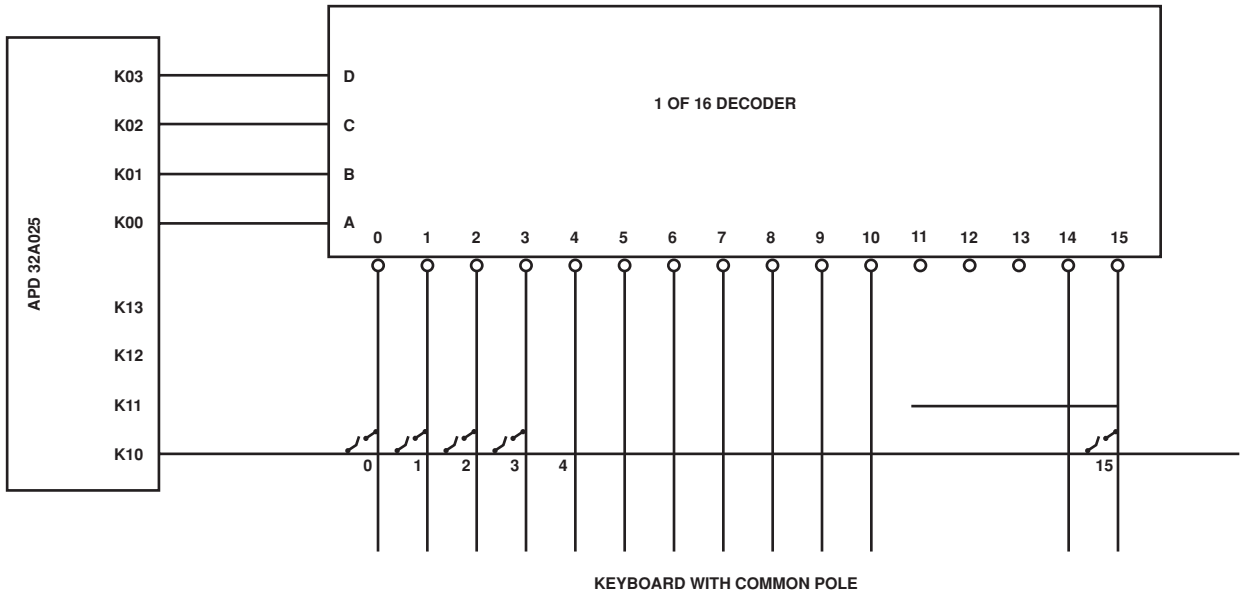
KEYBOARD INTERFACING

The APD-32A025A provides timing signals to scan keyboards of up to 64 keys, using the lockout scan method. Each key is sequentially scanned and tested for closure. After detection of the first closed key, and after the debounce time (16 msec max) the address of the key is loaded into the APD-32A025A internal keyboard register (D0-D5). The keyboard register flag bit (D7) is also set, (high) and the keyboard interrupt request flag (KB IRQ) goes low. The CPU can therefore detect a key closure by either continuously testing D7 (instruction GKA) or by the CPU interrupt (KB IRQ connected to the CPU interrupt line).

The keyboard flag (D7) will remain high and the keyboard interrupt (KB IRQ) will remain low until the master CPU reads the keyboard (command GKA). When GKA has been executed the closed keys address will be in the APD-32A025A output register, D7 will go low and KB IRQ will go high.

The APD-32A025A will scan a keyboard in one of two ways, the 16 key mode or the 64 key mode, which is programmable by command LKS (load keyboard status). Bounce time is 16 msec max and closure time is 48 msec min. Maximum rate is 10 depressions per second.





KEYBOARD WITH COMMON POLE

To scan more than 16 switches, a 4 line to 16 line decoder must be added, which will allow scanning up to 64 keys. In this mode the keyboard outputs (KO0-KO3) will work as a 4 bit binary counter.

The keyboards can be scanned by using a 4-bit code to select one of up to 16 switches. The lines are driven by a 4 to 16 decoder, which supplies a ground return to the selected switch. The switch common line is then read to sense the condition to that switch. (see keyboard with common pole).

If two or more keys are depressed simultaneously, only one key will be detected. After that key is released the second will be encoded, and etc. Note that if three keys are depressed simultaneously to form and “L” configuration, an erroneous input could occur. If this presents a potential problem, a diode (IN914) should be added to the column pole of each switch.

COMMAND SUMMARY

The APD-32A025A can execute a number of commands (instructions) for the display and keyboard manipulation. In addition certain display and keyboard parameters can be programmed.

After the master CPU issues a command to the APD-32A025A, the APD-32A025A will reset its busy flag to 0. That flag (data bit 3) can be tested by the master CPU as described earlier. When the APD-32A025A has finished execution of the command, the flag will be set to 1 and the master CPU can issue the next command. (Execution time varies for different commands.)

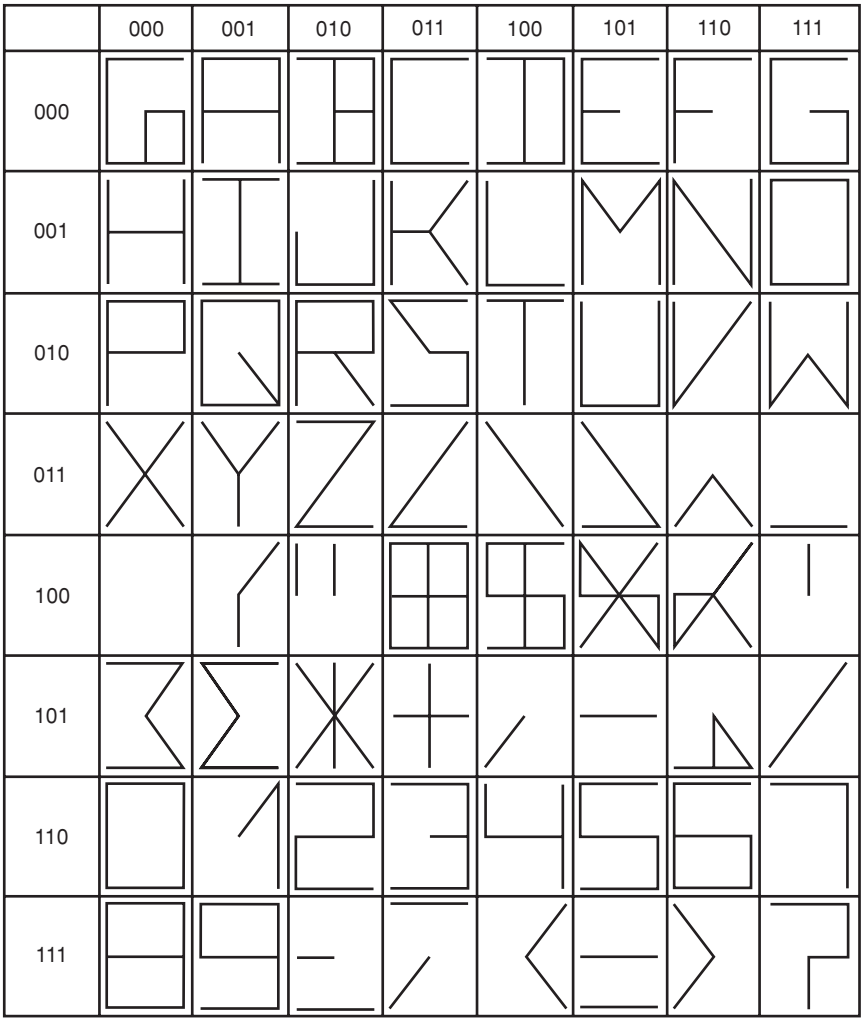
APD-32A025A COMMAND SET

MNEMONIC	CODE										DESCRIPTION
	Hex	Dec	D7	D6	D5	D4	D3	D2	D1	D0	
CLA	E0	224	1	1	1	0	0	0	0	0	Clear display memory
BLA	E1	225	1	1	1	0	0	0	0	1	Load blank to display memory
RTL	E2	226	1	1	1	0	0	0	1	0	Rotate display left
RTR	E3	227	1	1	1	0	0	0	1	1	Rotate display right
SHL	E4	228	1	1	1	0	0	1	0	0	Shift display left
SHR	E5	229	1	1	1	0	0	1	0	1	Shift display right
INC	E6	230	1	1	1	0	0	1	1	0	Increment cursor
DEC	E7	231	1	1	1	0	0	1	1	1	Decrement cursor
GKA	E9	233	1	1	1	0	1	0	0	1	Get key address
GDM	EA	234	1	1	1	0	1	0	1	0	Get display memory
GDL	EB	235	1	1	1	0	1	0	1	1	Get display length
GKS	EC	236	1	1	1	0	1	1	0	0	Get keyboard status
GDS	ED	237	1	1	1	0	1	1	0	1	Get display status
GTR	EE	238	1	1	1	0	1	1	1	0	Get timer register
GCA	EF	239	1	1	1	0	1	1	1	1	Get cursor address
LCR			1	0	0	e	d	c	b	a	Load cursor and read display
LDL			0	1	0	1	1	1	1	1	Load display length
LKS			1	0	1	1	0	0	b	a	Load keyboard/character status
LDS			1	1	0	e	d	c	b	a	Load display status
LTR			0	1	1	e	d	c	b	a	Load timer register
LDM			0	0	F	e	d	c	b	a	Load display memory

CLA	**Clear Display Memory**									
OP Code	1	1	1	0	0	0	0	0	E0	224
600µS	The display refresh memory is cleared to zero. All positions will display "@" character.									
BLA	**Load Blank to Display**									
OP Code	1	1	1	0	0	0	0	1	E1	225
600µS	The display refresh memory is loaded with the ASCII code for blank (1 0 0 0 0 0 0). All characters will be blank.									
RTL	**Rotate Display Left**									
OP Code	1	1	1	0	0	0	1	0	E2	226
800µS	The display is rotated one place to the left. The most significant character is shifted into the least significant character position. (Upper left character is shifted to lower right position.)									
RTR	**Rotate Display Right**									
OP Code	1	1	1	0	0	0	1	1	E3	227
700µS	The display is rotated one place to the right. The least significant character position is shifted into the most significant position. (Lower right character is shifted to upper left position.)									
SHL	**Shift Display Left**									
OP Code	1	1	1	0	0	1	0	0	E4	228
800µS	The display is shifted for one place to the left. The most significant character (upper left) is lost, the last character (lower right) becomes blank.									
SHR	**Shift Display Right**									
OP Code	1	1	1	0	0	1	0	1	E5	229
600µS	The display is shifted for one place to the right. The last character (lower right) is lost, the most significant character (upper left) becomes blank.									
INC	**Increment Cursor**									
OP Code	1	1	1	0	0	1	1	0	E6	230
200µS	The cursor is incremented one position (shifted to the right). The content of the display refresh memory pointed to by the cursor is placed in the output register.									
DEC	**Decrement Cursor**									
OP Code	1	1	1	0	0	1	1	1	E7	231
200µS	The cursor is decremented one position (shifted to the left). The content of the display refresh memory pointed to by the cursor is placed in the output register.									
GKA	**Get Key Address**									
OP Code	1	1	1	0	1	0	0	1	E9	233
150µS	The address of the depressed key (6 bits) is loaded into the output register. At the end of this instruction (same as for every GET instruction), the output register contains data. The CPU will read data by strobing $\overline{CS}$, $\overline{RD}$ an A0 = 0. (bit 7 up) Note that KB IRQ is cleared (set high) and Bit 7 is set low when execution is complete. g 0 f e d c b a — Output register content at the end of GKA instruction. key address Keyboard flag: 1 = key depressed; 0 = no key depressed (e and f are 0 for 16 key scan mode)									
GDM	**Get Display Memory**									
OP Code	1	1	1	0	1	0	1	0	EA	234
150µS (AUTO) 250µS (AUTO INC., DEC)	First the cursor is auto-incremented according to the display status work. Then, the content of the display refresh memory (ASCII) code) pointed to by the cursor is placed into the output register. 0 0 f e d c b a — Output register content at the end of GDM instruction. ASCII code									

GDL	**Get Display Length**									
OP Code	1	1	1	0	1	0	1	1	EB	235
100µS	The content of the display length register is loaded into the output register. 0 0 0 1 1 1 1 1 — Output register content at the end of GDL instruction. display length = 32 (0-31) Note: Display length should always equal 1 1 1 1 1									
GKS	**Get Keyboard Status**									
OP Code	1	1	1	0	1	1	0	0	EC	236
100µS	The content of the keyboard status register is loaded into the output register. 0 0 0 e d c b a — Output register content at the end of GKS instruction. 1 0 0 — 64 key scan = 1; 16 = 0 keyboard scan on = 0; off = 1 For proper operation bits “c”, “d” and “e” must be set as shown.									
GDS	**Get Display Status**									
OP Code	1	1	1	0	1	1	0	1	ED	237
100µS	The content of the display status register is loaded into the output register. 0 0 0 e d c b a — Output register at the end of GDS instruction. up/down cursor UP = 1; DOWN = 0 index/non-index cursor INDEX = 1; NON-INDEX = 0 cursor on/off ON = 0; OFF = 1 blink on/off ON = 1; OFF = 0 Display on/off ON = 0; OFF = 1									
GTR	**Get Timer Register**									
OP Code	1	1	1	0	1	1	1	0	EE	238
100µS	The content of the timer register is loaded into the output register. 0 0 0 e d c b a — Output register at the end of GTR instruction. timer code									
GCA	**Get Cursor Address**									
OP Code	1	1	1	0	1	1	1	1	EF	239
100µS	The cursor address is loaded into the output register. 0 0 0 e d c b a — Output register at the end of GTR instruction. cursor address									
LCR	**Load Cursor and Read Display**									
150µS	1 0 0 e d c b a cursor address The operand D0-D4 is loaded into the APD-32A025A’s cursor register, and the character addressed by the cursor is loaded into the output register. 0 0 f e d c b a — Output register at the end of GTR instruction. ASCII code									
LDL	**Load Display length**									
100µS	0 1 0 1 1 1 1 1 display length Executing the command has no affect on operation. This command is only maintained for compatibility with earlier model APD-32A025A									

LKS	Load Keyboard/Character Status
100µS	1 0 1 1 0 0 b a a: 64 key scan = 1; 16 = 0 b: keyboard scan on = 0; off = 1 Loads keyboard status register. Bit “b” enables the keyboard scan. Bit “a” determines the type of scanning, either 16 or 64 keys. Note: For proper operation bits “c”, “d” and “e” must be set as shown
LDS	**Get Display Status**
100µS	0 0 0 e d c b a a: up/down cursor UP = 1; DOWN = 0 b: index/non-index cursor INDEX = 1; NON-INDEX = 0 c: cursor blink on/off ON = 1; OFF = 1 d: Display on/off ON = 0; OFF = 1 The APD-32A025A’s display status register is loaded by this instruction. Bit ”e” switches display on/off. Bit “d” when logical 1 will cause the entire display to blink at approximately 1 Hz. Bit “c” allows the cursor to blink beneath the character displayed in cursor position. Bit “6” = 1 sets internal index F-F. Bit “b” = 0 resets the index F-F. If the index F-F is set , every LDM (load display memory) or GDM (get display memory) instruction will automatically increment or decrement the cursor, depending on bit “a” ()a = 0 decrement; a = 1 increment).
LTR	**Load Timer Register**
OP Code	0 1 1 e d c b a
100µS	This command is only maintained for compatibility with earlier model APD-32A025. Executing the command has no affect on operation
LDM	**Load Display Memory**
100µS (AUTO) 200µS (AUTO) INC., DEC)	0 0 f e d c b a ASCII code Loads display refresh memory at the location pointed to by the cursor.



DISPLAY CHARACTER LOCATION

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

INITIALIZATION

Initialization consists of the reset procedure followed by commands to load display and keyboard parameters as follows:

COMMAND	CODE								DESCRIPTION
LDL	0	1	0	1	1	1	1	Load Display Length	
LKS	1	0	1	1	0	0	b	A	Load Keyboard/Character Status
LCR	1	0	0	e	d	c	b	A	Load Cursor and Read Display
CLA	1	1	1	0	0	0	0	0	Clear Display memory
LDS	1	1	0	e	d	c	b	A	Load Display Status

Note: If a command is issued during the time the APD-32A025A is executing the previous command (Busy Flag = 0), the second command could cause an error condition. Therefore, it is recommended that the busy flag always be tested before issuing any command.

POWER DOWN (STANDBY) MODE

The display may be operated in a low power (STANDBY) mode by removing power to the high voltage supply, but retaining power on a STBY supply. During standby operation current drain is reduced to approximately 10 ma. The display will be dark (blank), but communications and operation can be maintained. Upon energizing the high voltage supply again, the APD-32A025A will come up with the display refresh memory and other registers unchanged.

SAMPLE PROGRAMS (for 8080 microprocessor) (It is assumed that the APD-32A025A is memory mapped and located at addresses (FFF), FFF1.)		
INITIALIZATION		
INITIAL	LXI H FFF0	Load H, L pair with PD-32A025A address
	CALL A FLAG	Jump to subroutine to test flag
	MVIM, #5F	Load PD-32A025A with micro-code for LDL (display length = 32)
	CALL A FLAG	
	MVIM #B1	Load keyboard status (keyboard scan “ON”, 64 key scan)
	CALL A FLAG	
	MVIM #79	Load timer (timer = 25)
	CALL A FLAG	
	MVIM #80	Load cursor, Read display
	CALL A FLAG	
	MVIM #E1	Load to blank display
	CALL A FLAG	
	MVIM #C7	Load display status (display “ON”, display blink “OFF”, cursor blink “ON”, auto increment “ON”)
SUBROUTINE TO TEST A BUSY FLAG		
A FLAG	LDA, FFF1	Load flag bit into accumulator
	ANI #08	Mask flag (D3)
	JZ, A FLAG	Test flag
	RET	Return from subroutine (D3 = 1)
After the last initialization command has been loaded (LDS - load display status) the display is switched on. The master CPU can write or read alphanumeric data to and from the APD-32A025A. The data (ASCII) can be loaded by a LDM (load display memory) command. A simple method is to load the master CPU accumulator with the desired ASD = CII code, with D6 and D7 set to zero, and output it to the APD-32A025A. The character will be loaded and displayed at the current cursor position. For example to write letter “M” in display:		
	LXI H, FFF0	Set APD-32A025A address
	CALL A FLAG	
	MVI A, #4D	Load accumulator with ASCII code for M (hex)
	ANI, #3F	Set D6, D7 to zero, LDM command code
	MOV M, A	Load APD-32A025A
To read display, at current cursor position: (when display status register is not set for auto increment)		
	LXI H, FFF0	Set APD-32A025A address
	CALL A FLAG	
	MVIM, #EA	Send APD-32A025A GDM command
	CALL A FLAG	
	LDA FFF0	Read APD-32A025A output register

Note: Programming can be shortened by storing the APD-32A025A commands in a table. The control program is set up as a loop that outputs one command per pass through the loop.

WARNING

THE PLASMA DISPLAY REQUIRES 200 VOLTS D.C TO OPERATE. THIS VOLTAGE IS PRESENT AT MANY LOCATIONS IN THE SYSTEM. **CAUTION SHOULD BE EXERCISED TO AVOID CONTACT.**

Notice

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