Intelligent Frequency Synthesizers

Preliminary Data Sheet PNP-1191-P22

FEATURES:

- **685-785 MHz Frequency Range**
- **Programmable Step Size**
- **Low Integrated Phase Noise**
- **Simplified Programming**

APPLICATIONS:

- **Wireless Infrastructure**
- **Test Equipment**
- **Wireless LAN**

MICROWIRE is a trademark of National Semiconductor Corp.
SPI is a trademark of Motorola, Inc.
I^2C is a trademark of Philips Corp.

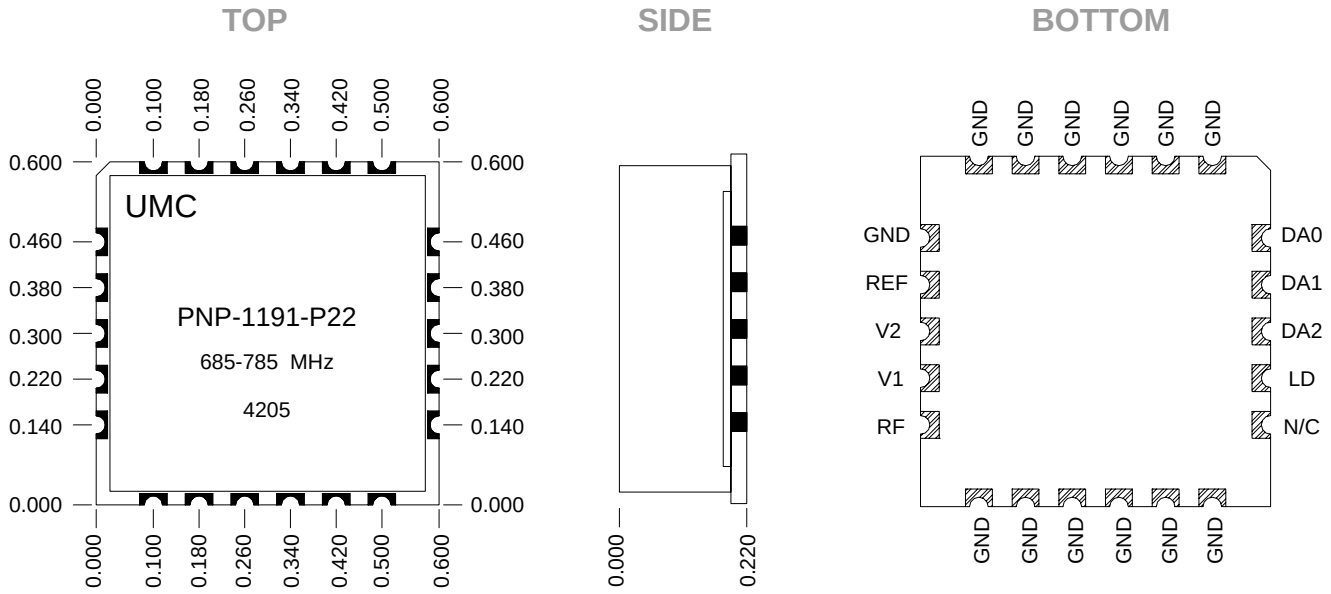
DESCRIPTION:

The PNP-1191-P22 is a complete low noise frequency synthesizer, comprised of VCO, PLL, loop filter and data interface. The PNP family of RF signal sources is the world's first truly configurable frequency synthesizer module. PNP technology offers the designer the ability to configure all of the synthesizer's vital functions 'on the fly' with simple strings of code that contain the commands of START, STOP, STEP, CHANNEL and REF. When new data is received, the PNP module optimizes its internal settings for best overall integrated phase noise, switching speed and spurious suppression, all automatically and in less than 100 μS. Therefore, if the system requires 100 kHz steps in mode #1 and 1 MHz step size in mode #2, these smart synthesizers can make quick adjustments with amazing accuracy, speed and performance.

Control of the internal registers is accomplished through a serial data interface. Many industry standard protocols are supported, including I^2C, SPI, and MICROWIRE Serial Interfaces. The PNP-1191-P22 is powered from +3V and +12.0V supplies delivering +9 dBm of RF output power.

Package Drawing

all dimensions in inches



Universal Microwave Corporation, 2339 Destiny Way, Odessa, FL 33556
UMC Worldwide Customer Support Center: 4703 S. Lakeshore Drive, Suite 2, Tempe, AZ 85282
1.877.UMC.Xtreme / Fax 480.756.6026

PNP-1191-P22 Specifications

V1 = +12.0V, V2 = +3.0V, REF =20.0 MHz, -40 to +85C

Parameter	Min	Typ	Max	Units
RF OUT Characteristics				
Frequency Range	685		785	MHz
Output Power	+7	+9	+11	dBm
Harmonics		-12	-8	dBc
Noise Characteristics				
1 kHz offset ∅ Noise		-98	-93	dBc/Hz
10 kHz offset ∅ Noise		-112	-106	dBc/Hz
100 kHz offset ∅ Noise		-132	-126	dBc/Hz
1 MHz offset ∅ Noise		-152	-146	dBc/Hz
Spurious Signals				
STEP = 100 kHz		-70	-60[1]	dBc
				dBc
				dBc
REF Feed-through		-80	-70	dBc
REF IN Characteristics				
REF Input Frequency	10	20	250	MHz
REF Input Sensitivity [2]	-5	0	+5	dBm
REF Input Current			+/-100	µA
Logic Inputs				
V_{INH}, Input High Voltage	1.35			Vdc
V_{INL}, Input Low Voltage			0.6	Vdc
I_{INH}, I_{INL}, Input Current			+/- 1	µA
C_{IN}, Input Capacitance			10	pF
Logic Outputs				
V_{OH}, Output High Voltage	V_2 - 0.4			Vdc
V_{OL}, Output Low Voltage			0.4	Vdc
I_{OH}, I_{OL}, Output Current			500	µA
Power Supplies				
Supply Voltage, V_1	11.75	12.0	12.25	Vdc
Supply Voltage, V_2	2.7	3.0	3.3	Vdc
Supply Current, I_1		48	55	mA
Supply Current, I_2		25	35	mA

NOTES: 1. Max STEP spurious are degraded by an additional 10 dB at integer multiples of the Reference Frequency within a +/-100 kHz bandwidth 2. AC coupled. For DC coupled, 0 - V_2 max.

Pin Descriptions PNP-1191-P22

Mnemonic	FUNCTION
RF	RF Output. This pin is AC coupled and should be connected to a non-reflective 50 ohm load.
V1	Supply Input. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. Use an ultra low-noise regulator followed by an RC filter for best noise.
V2	Supply Input. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. Use an ultra low-noise regulator followed by an RC filter for best noise.
REF	Reference Input. This is a CMOS input with a nominal threshold of $V_2/2$ and a dc equivalent input resistance of 100K ohms. This input can be driven from a CMOS or TTL crystal clock oscillator or it can be ac coupled.
GND	Analog and RF Ground.
DA0	Serial Interface. This input functions as **$\overline{\text{CS}}$** in MICROWIRE/SPI Bus mode. This input functions as **SDA** in I^2C BUS mode.
DA1	Serial Interface. This input functions as **DATA** in MICROWIRE/SPI BUS mode. This input functions as **SCL** in I^2C BUS mode.
DA2	Serial Interface. This input functions as **CLOCK** in MICROWIRE/SPI BUS mode. This input must be connected to the **DIGITAL GROUND** in I^2C BUS mode.
LD	Lock Detect. This output is active high and provides a continuous digital lock status.

Absolute Maximum Ratings

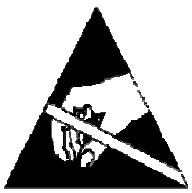
V_1 to Ground	-0.3 to +12.5 Vdc
V_2 to Ground	-0.3 to +3.6 Vdc
REF IN to Ground	-0.3 to (V_2 + 0.3) Vdc
RF OUT to Ground	+/- 25 Vdc
Digital I/O to Ground	-0.3 to (V_2 + 0.3) Vdc

Operating Temperature	-40° to +85°C
Storage Temperature	-55° to +100°C

Stress above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Operation of the device above the conditions listed in the operational sections of this specification is not implied.

Ordering Guide PNP-1191-P22

Model	I^2C Address	Type Code
PNP-1191-P22	Default	P060
PNP-1191A-P22	Default + 1	P060
PNP-1191B-P22	Default + 2	P060
PNP-1191C-P22	Default + 3	P060



CAUTION!
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the PNP family of synthesizers feature ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality

Overview

The PNP family of intelligent Frequency Synthesizers can be controlled through the use of a microprocessor interface or Bus. Several protocols are supported by PNP devices, although this specification will focus on SPI Bus, MICROWIRE-Interface and I^2C Bus implementations. For SPI and MICROWIRE applications, PNP devices require a single 32 bit string of serial data to set frequency or to change its internal settings (Figure 1). I^2C Bus utilizes some unique control bits and requires the addition of an ADDRESS byte, increasing the serial bit-stream for this protocol to 40 bits per command (Figure 2).

The PNP device is programmed at the factory with presets for the START, STOP, STEP and REFERENCE registers. It is not necessary to re-load any of these registers if the factory values are acceptable. If the application requires different values than the factory pre-sets, then the PNP device must first be initialized by loading data into each of the affected registers. It is not necessary to re-load any registers that are already set properly for the application. START defines the lowest desired frequency of operation. STOP defines the highest desired frequency of operation. STEP is used to channelize the band and REFERENCE defines the frequency of the external reference. Once the PNP device is initialized, a fixed number channels are available. Loading the CHANNEL register sets the operating frequency of the PNP device. The formula for calculating the operating frequency is:

START(Hz) + (CHANNEL * STEP(Hz)) = Frequency(Hz)

MICROWIRE Interface and SPI Bus

MICROWIRE-Interface and SPI Bus are extremely similar protocols (Figures 6 & 7). DATA bits are clocked into the PNP device on the rising edge of the CLOCK input. $\overline{CS}$, or chip select not, must be in a low state for the incoming DATA bits to be accepted. After all 32 bits have been clocked in, the $\overline{CS}$ line must transition high for the DATA string to be latched. After the string is latched, the information in the FUNCTION block (Figure 5) determines where the data will be routed internally.

I^2C Bus

The I^2C Bus is a high-speed method of communicating over a two wire interface. PNP modules are configured as “slaves” or receive-only devices and can only listen for commands from the “master” which is typically a microprocessor. The I^2C two wire Bus consists of SDA (serial data) and SCL (serial clock) lines. In order to use the I^2C Bus for control of the PNP synthesizer module, the DA2 line (see Package Drawing, Page 1) must be tied to Digital Ground. Additionally, the SDA and SCL lines must be pulled up to D_{vdd} using external resistors.
Multiple PNP devices can reside on the same two wire Bus without the danger of corrupted data or data collisions. Device selection is accomplished by sending a slave address preceding each string of data. If only one PNP device will be used on the I^2C Bus, then the factory pre-set base address will operate properly. If more than one PNP device will reside on the same I^2C Bus, then modules with unique address locations must be used. This should be specified when ordering (see Ordering Guide on page 3). For additional information refer to the I^2C Bus specification (copyright Philips Corp).

I^2C Implementation

Transferring data to PNP synthesizers using I^2C protocol varies significantly from that of SPI or MICROWIRE. PNP modules operate as slaves on the I^2C Bus and do not write to the Bus. However, due to the fact that many devices might reside on the same Bus, addressing must be used to direct the flow of data traffic. So, within the bit stream sent to the PNP device, there is a block of data that comprises the ADDRESS byte. Within this address byte there are 7 bits that are used for the address location and the eighth is used as a read/write (R/W) bit. Since PNPs are slaves and will never write to the I^2C Bus, this bit will always be set to 0 (logic low).

Each data string is sent using a series of five single byte blocks. I^2C protocol requires that each string of data begin with a master generated START (S). Each byte within the string must end with a slave generated ACKNOWLEDGE (A). Finally, after all five bytes are generated, the transfer is concluded with a master generated STOP (P). The master generated STOP must be executed following each data string for the values to be accepted by the PNP device. If this condition is not satisfied and a new master generated START occurs, the PNP device will purge the previous data without updating the desired attribute. REPEATED START (S_r) operation is not allowed when sending data to the PNP device.

The flow of data bytes to the PNP device is outlined in Figure 2. Since FUNCTION SELECT and MULTIPLIER are 4 bits each, these blocks of data are combined into one byte. Additionally, since the FREQUENCY/ CHANNEL block of data is 24 bits long, it must be fragmented into three individual bytes as shown.

FIGURE 2: **FREQUENCY/CHANNEL** (DB0 - DB23) This is a 24 bit string used to set the synthesizer's START Frequency, STOP Frequency, STEP Frequency, REF Frequency or CHANNEL number.

DB23	DBn	DB3	DB2	DB1	DB0	FREQUENCY/CHANNEL
FC23	FCn	FC3	FC2	FC1	FC0	
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
0	0	1	1	1	1	15

FIGURE 3: **MULTIPLIER** (DB24 - DB27) The data in **FREQUENCY/CHANNEL** (DB0-DB23) is multiplied by 10^n where the value of n is determined by the contents of **MULTIPLIER** (DB24-DB27) as shown below.

DB27	DB26	DB25	DB24	MULTIPLIER
M3	M2	M1	M0	
0	0	0	0	10^0 X contents of DB0-DB23
0	0	0	1	10^1 X contents of DB0-DB23
0	0	1	0	10^2 X contents of DB0-DB23
0	0	1	1	10^3 X contents of DB0-DB23
n	n	n	n	10^n X contents of DB0-DB23

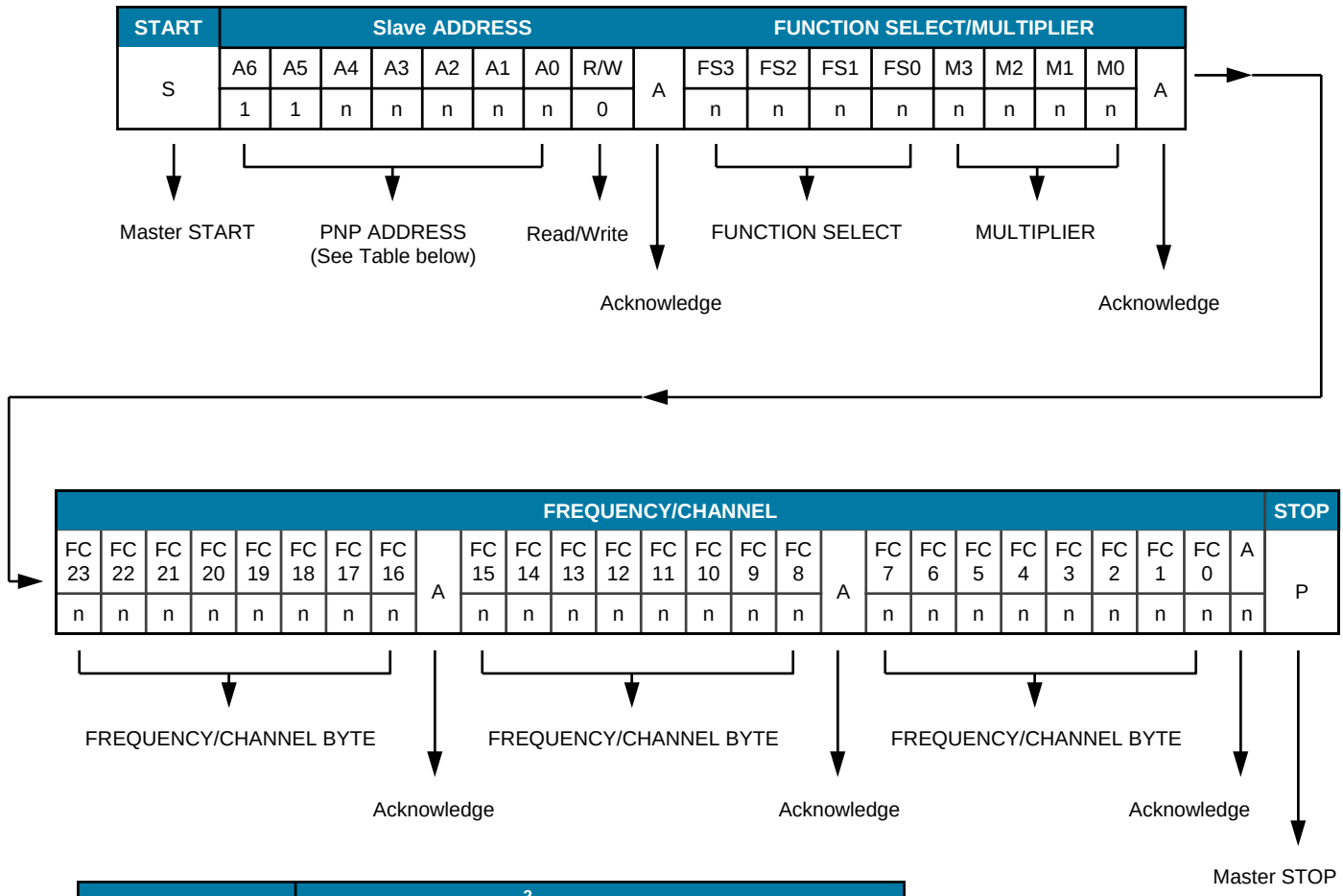
FIGURE 4: **FUNCTION SELECT** (DB28 - DB31). After the data in **FREQUENCY/CHANNEL** (DB0 - DB23) is multiplied by 10^n where the value of n is determined by the contents of **MULTIPLIER** (Figure 3), it is then routed internally to the START, STOP, STEP, REF or CHANNEL registers based on the contents of **FUNCTION SELECT** as shown below.

DB31	DB30	DB29	DB28	FUNCTION SELECT
FS3	FS2	FS1	FS0	
0	0	0	0	CHANNEL. Routes data from DB0-DB23 to the **CHANNEL REGISTER.**
0	0	0	1	START. Routes data from DB0-DB23 to the **START REGISTER.**
0	0	1	0	STOP. Routes data from DB0-DB23 to the **STOP REGISTER.**
0	0	1	1	STEP. Routes data from DB0-DB23 to the **STEP REGISTER.**
0	1	0	0	REFERENCE. Routes data from DB0-DB23 to the **REFERENCE REGISTER**
All FUNCTION SELECT values not shown above are reserved for factory use.				

Figure 1: SPI Bus/Microwire-Interface Data Structure

FUNCTION SELECT (4 BITS)				MULTIPLIER (4 BITS)				FREQUENCY/CHANNEL (24 BITS)					
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB_n	DB2	DB1	DB0
FS3	FS2	FS1	FS0	M3	M2	M1	M0	FC23	FC22	FC_n	FC2	FC1	FC0

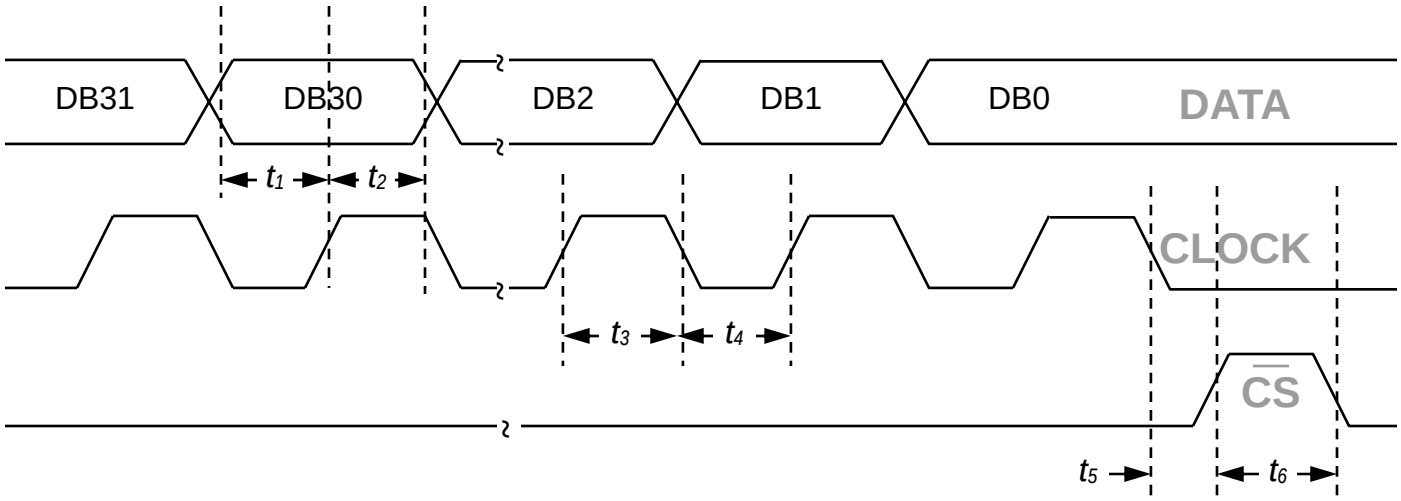
Figure 2: I^2C Bus Data Structure



MODEL NUMBER	I^2C ADDRESS						
	A6	A5	A4	A3	A2	A1	A0
PNP-745-P22	1	1	0	0	0	0	0
PNP-745A-P22	1	1	0	0	0	0	1
PNP-745B-P22	1	1	0	0	0	1	0
PNP-745C-P22	1	1	0	0	0	1	1
PNP-745x-P22	1	1	n	n	n	n	n

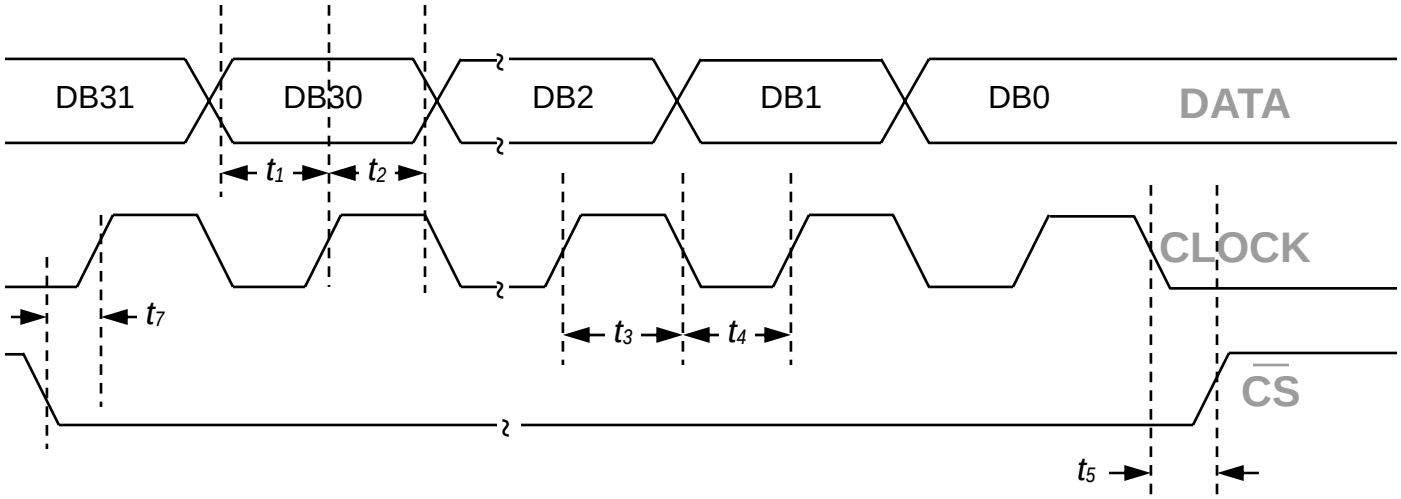
SPI Bus/MICROWIRE-Interface Timing Characteristics

Figure 6: MICROWIRE Interface Timing Diagram



Parameter	Limit at t_{min} to t_{max}	Units	Test Conditions/Comments
t_1	100	ns min	DATA to CLOCK setup time
t_2	100	ns min	DATA to CLOCK hold time
t_3	250	ns min	CLOCK high time
t_4	250	ns min	CLOCK low time
t_5	100	ns min	CLOCK to $\overline{CS}$ setup time
t_6	200	ns min	$\overline{CS}$ pulse width (applies to MICROWIRE Interface only)
t_7	200	ns min	$\overline{CS}$ to CLOCK setup time (applies to SPI BUS only)

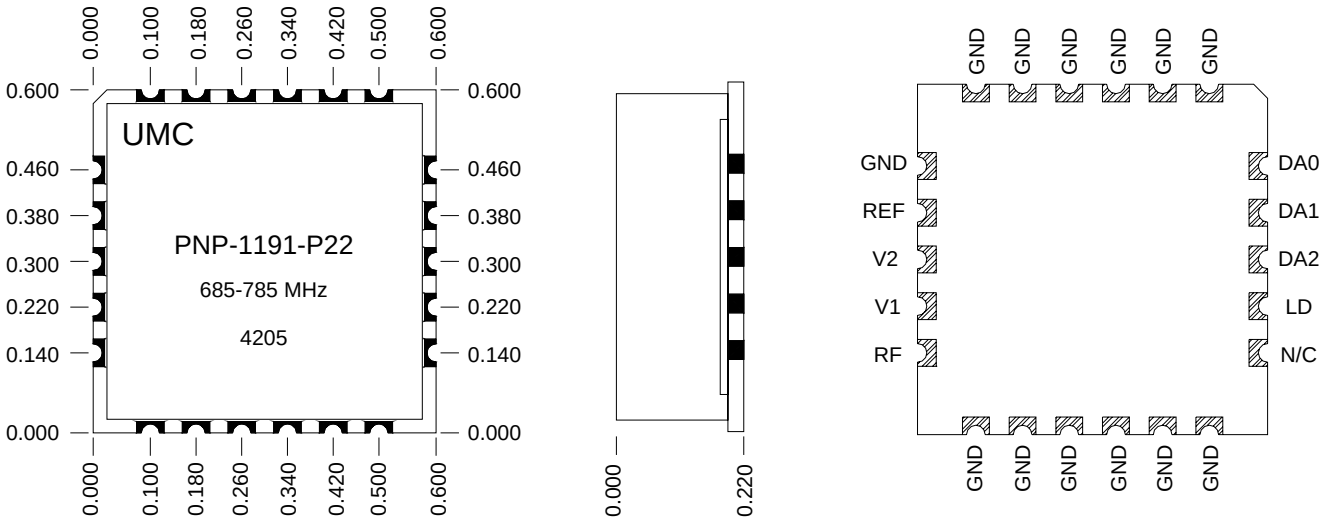
Figure 7: **SPI BUS Timing Diagram**



Package Drawing

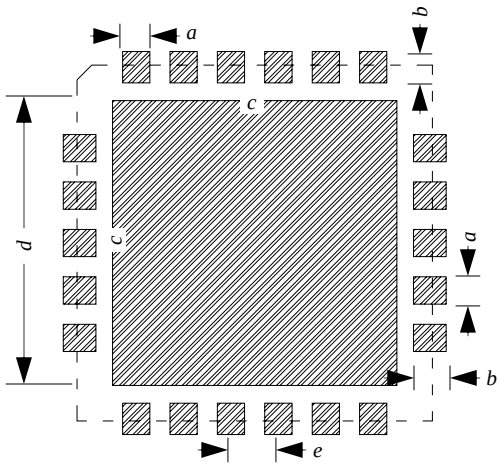
all dimensions in inches

TOP SIDE BOTTOM



Recommended Layout

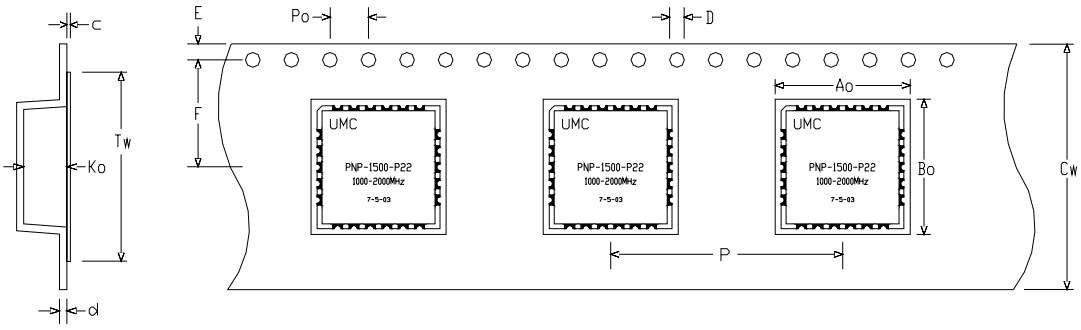
all dimensions in inches



Recommended Layout Dimensions			
	(min)	(typ)	(max)
a	0.043	0.046	0.049
b	0.052	0.055	0.058
c	0.475	0.480	0.485
d	0.535	0.540	0.545
e		0.080	

Tape and Reel Specifications

all dimensions in mm



Tape and Reel Dimensions			
Ao	15.5	***E***	1.75
Bo	15.5	***F***	10.2
P	16.0	***c***	0.06
Po	4.0	***d***	0.30
Cw	24.0	***Tw***	21.2
D	1.5	***Ko***	6.6