



**P-Channel Enhancement-Mode  
Vertical DMOS FETs**

**Ordering Information**

| BV <sub>DSS</sub> /<br>BV <sub>DGS</sub> | R <sub>DS(ON)</sub><br>(max) | I <sub>D(ON)</sub><br>(min) | Order Number / Package |          |          |
|--|------------------------------|-----------------------------|------------------------|----------|----------|
|  |                              |                             | TO-39                  | TO-92    | Die†     |
| -350V                                    | 75Ω                          | -200mA                      | VP0535N2               | VP0535N3 | VP0535ND |
| -400V                                    | 75Ω                          | -200mA                      | —                      | VP0540N3 | VP0540ND |

† MIL visual screening available

**High Reliability Devices**

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

**Features**

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

**Applications**

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

**Absolute Maximum Ratings**

|                                   |                   |
|-----------------------------------|-------------------|
| Drain-to-Source Voltage           | BV <sub>DSS</sub> |
| Drain-to-Gate Voltage             | BV <sub>DGS</sub> |
| Gate-to-Source Voltage            | ± 20V             |
| Operating and Storage Temperature | -55°C to +150°C   |
| Soldering Temperature*            | 300°C             |

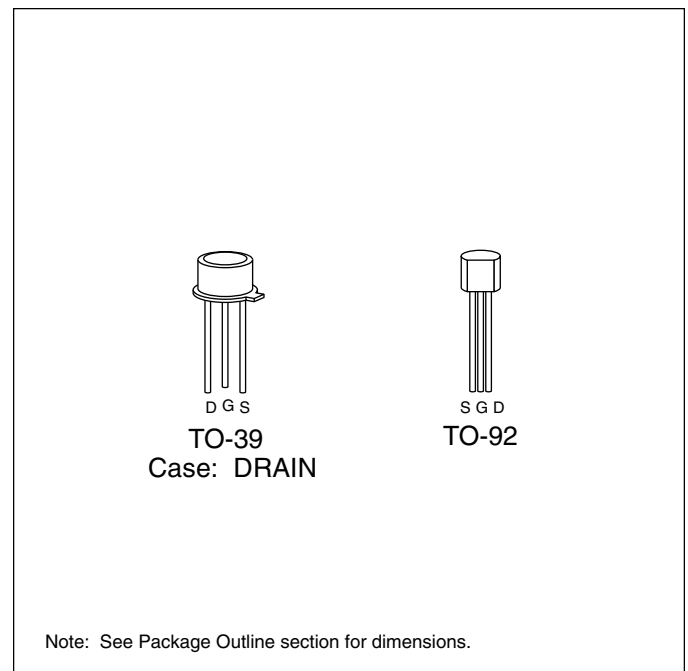
\* Distance of 1.6 mm from case for 10 seconds.

**Advanced DMOS Technology**

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

**Package Options**



## Thermal Characteristics

| Package | $I_D$ (continuous)* | $I_D$ (pulsed) | Power Dissipation<br>@ $T_C = 25^\circ\text{C}$ | $\theta_{jc}$<br>$^\circ\text{C/W}$ | $\theta_{ja}$<br>$^\circ\text{C/W}$ | $I_{DR}^*$ | $I_{DRM}$ |
|---------|---------------------|----------------|---|-------------------------------------|-------------------------------------|------------|-----------|
| TO-39   | -0.2A               | -0.5A          | 3.5W  | 35                                  | 125                                 | -0.2A      | -0.5A     |
| TO-92   | -0.1A               | -0.5A          | 1.0W  | 125                                 | 170                                 | -0.1A      | -0.5A     |

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

## Electrical Characteristics

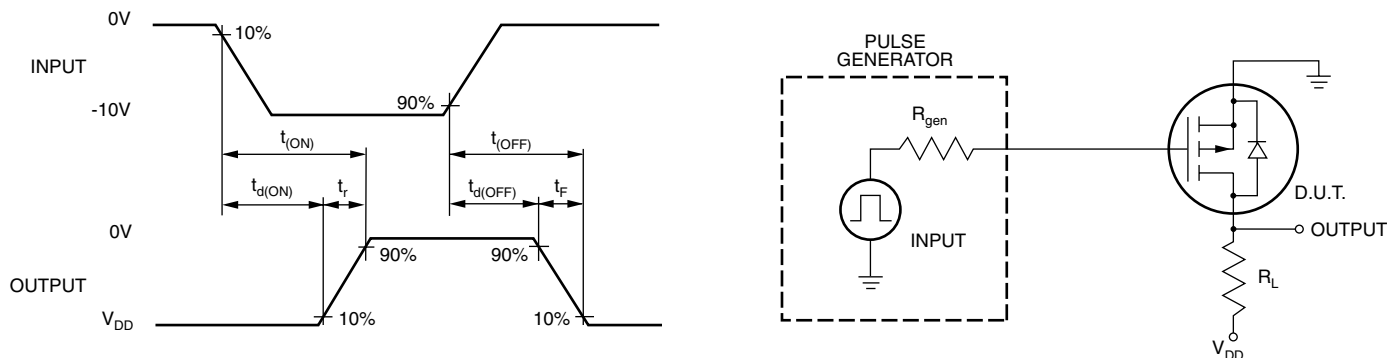
**OBSOLETE**

| Symbol              | Parameter                                  | Min    | Typ  | Max  | Unit                 | Conditions  |                           |
|---------------------|--|--------|------|------|----------------------|---|---------------------------|
| $BV_{DSS}$          | Drain-to-Source Breakdown Voltage          | VP0540 | -400 |      |                      | V   | $V_{GS} = 0V, I_D = -1mA$ |
|                     |  | VP0535 | -350 |      |                      |   |                           |
| $V_{GS(th)}$        | Gate Threshold Voltage                     | -2.5   |      | -4.5 | V                    | $V_{GS} = V_{DS}, I_D = -1mA$   |                           |
| $\Delta V_{GS(th)}$ | Change in $V_{GS(th)}$ with Temperature    |        | 3.5  | 6.0  | mV/ $^\circ\text{C}$ | $V_{GS} = V_{DS}, I_D = -1mA$   |                           |
| $I_{GSS}$           | Gate Body Leakage                          |        |      | -100 | nA                   | $V_{GS} = \pm 20V, V_{DS} = 0V$   |                           |
| $I_{DSS}$           | Zero Gate Voltage Drain Current            |        |      | -10  | $\mu\text{A}$        | $V_{GS} = 0V, V_{DS} = \text{Max Rating}$                                   |                           |
|                     |  |        |      | -500 |                      | $V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$<br>$T_A = 125^\circ\text{C}$ |                           |
| $I_{D(ON)}$         | ON-State Drain Current                     |        | -80  |      | mA                   | $V_{GS} = -5V, V_{DS} = -25V$   |                           |
|                     |  | -200   | -350 |      |                      | $V_{GS} = -10V, V_{DS} = -25V$  |                           |
| $R_{DS(ON)}$        | Static Drain-to-Source ON-State Resistance |        | 60   |      | $\Omega$             | $V_{GS} = -5V, I_D = -10mA$   |                           |
|                     |  |        | 45   | 75   |                      | $V_{GS} = -10V, I_D = -50mA$  |                           |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with Temperature    |        | 0.8  | 1.5  | %/ $^\circ\text{C}$  | $V_{GS} = -10V, I_D = -50mA$  |                           |
| $G_{FS}$            | Forward Transconductance                   | 50     | 70   |      | m $\Omega$           | $V_{DS} = -25V, I_D = -50mA$  |                           |
| $C_{ISS}$           | Input Capacitance                          |        | 40   | 60   | $\text{pF}$          | $V_{GS} = 0V, V_{DS} = -25V$<br>$f = 1 \text{ MHz}$                         |                           |
| $C_{OSS}$           | Common Source Output Capacitance           |        | 11   | 20   |                      |   |                           |
| $C_{RSS}$           | Reverse Transfer Capacitance               |        | 3    | 5    |                      |   |                           |
| $t_{d(ON)}$         | Turn-ON Delay Time                         |        |      | 10   | ns                   | $V_{DD} = -25V$<br>$I_D = -200mA$<br>$R_{GEN} = 25\Omega$                   |                           |
| $t_r$               | Rise Time                                  |        |      | 10   |                      |   |                           |
| $t_{d(OFF)}$        | Turn-OFF Delay Time                        |        |      | 15   |                      |   |                           |
| $t_f$               | Fall Time                                  |        |      | 15   |                      |   |                           |
| $V_{SD}$            | Diode Forward Voltage Drop                 |        | -0.8 | -1.5 | V                    | $V_{GS} = 0V, I_{SD} = -0.1A$   |                           |
| $t_{rr}$            | Reverse Recovery Time                      |        | 200  |      | ns                   | $V_{GS} = 0V, I_{SD} = -0.1A$   |                           |

### Notes:

- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

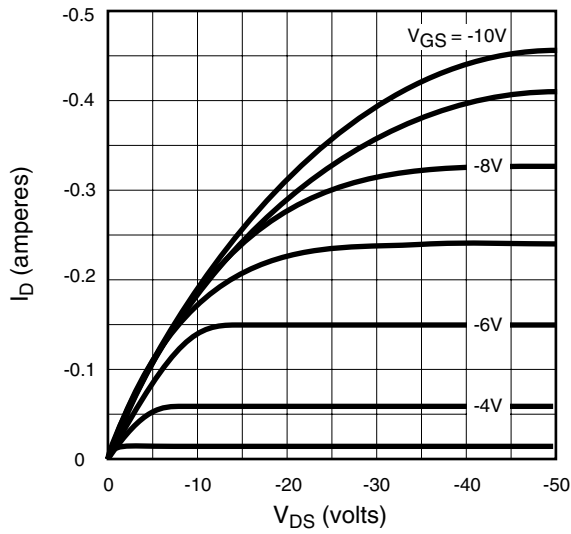
## Switching Waveforms and Test Circuit



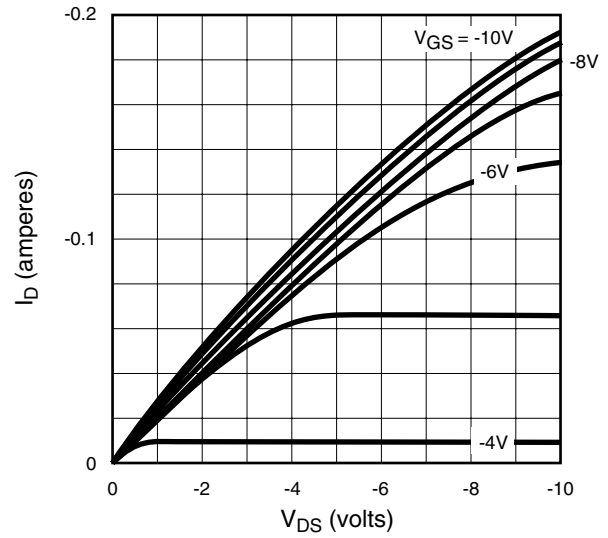
# Typical Performance Curves

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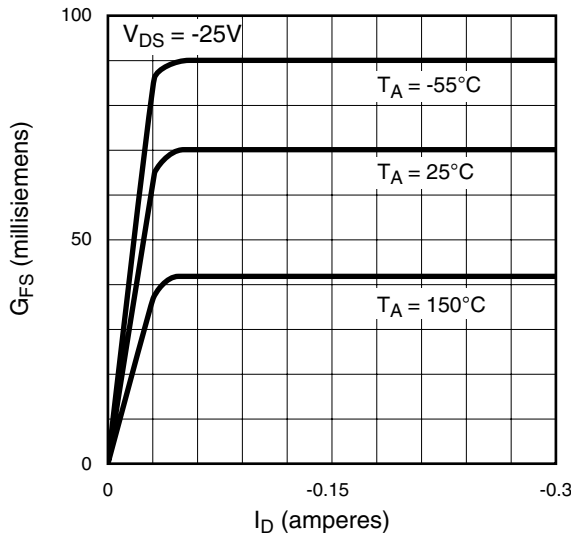
Output Characteristics



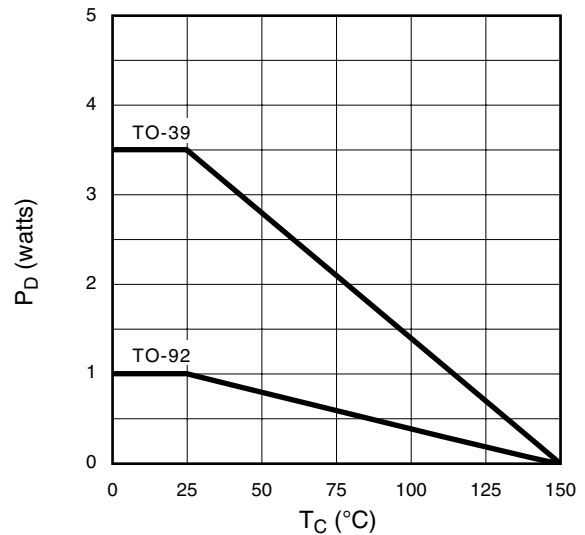
Saturation Characteristics



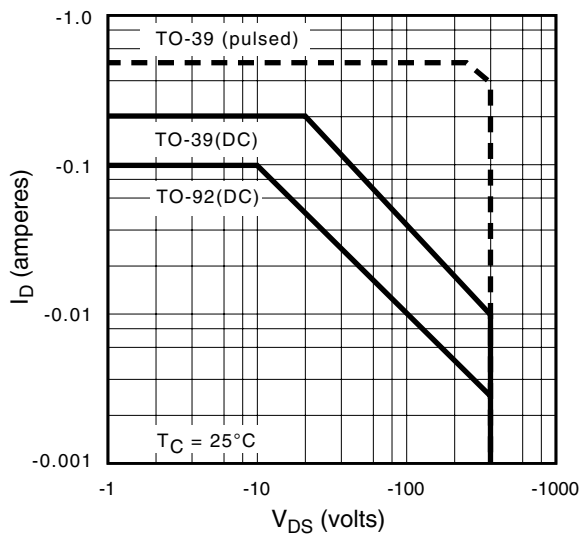
Transconductance vs. Drain Current



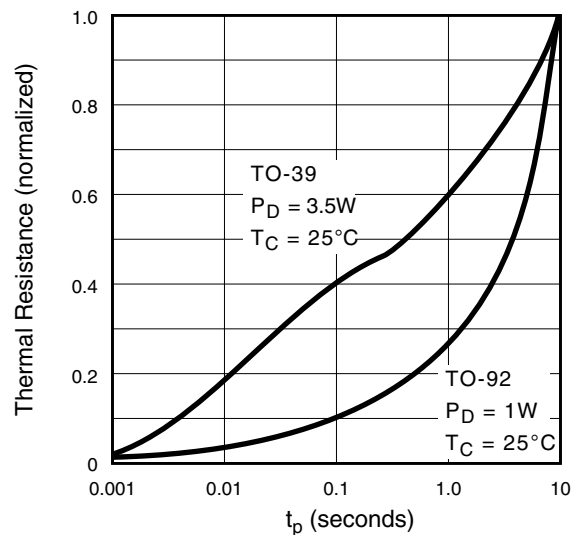
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics

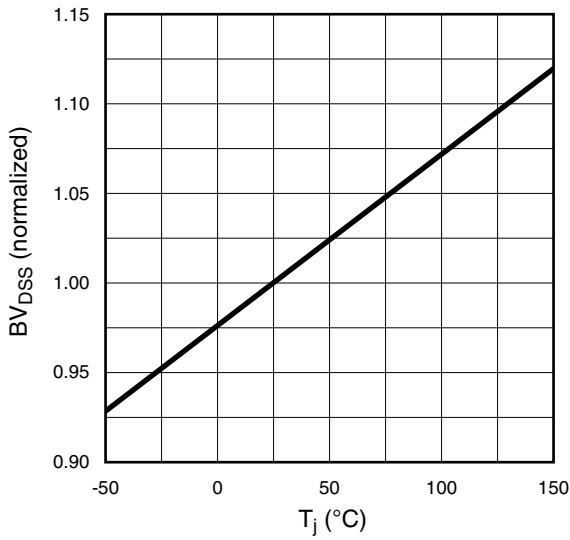


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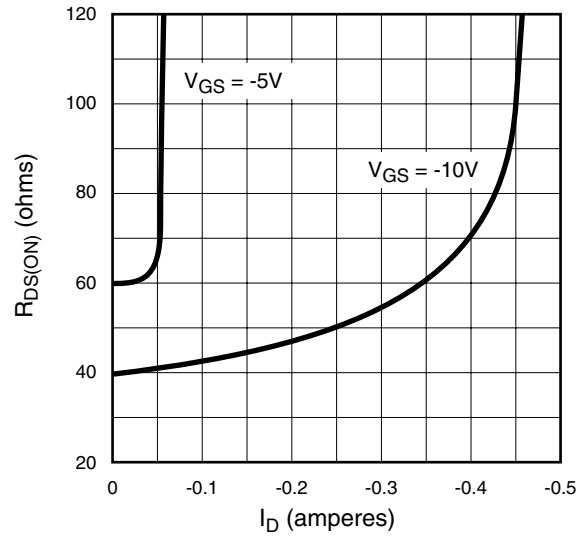
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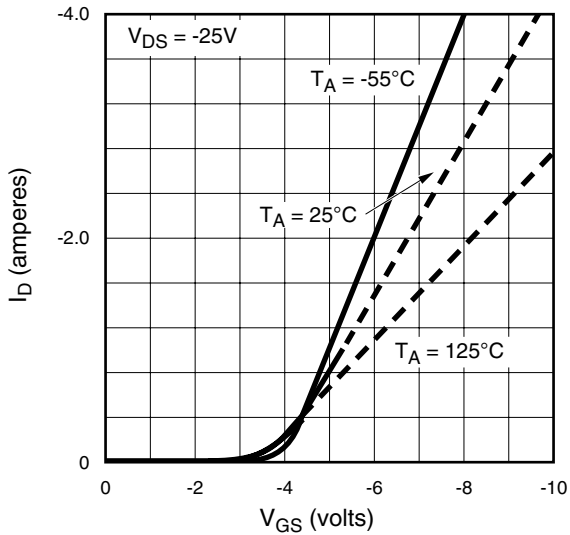
BV<sub>DSS</sub> Variation with Temperature



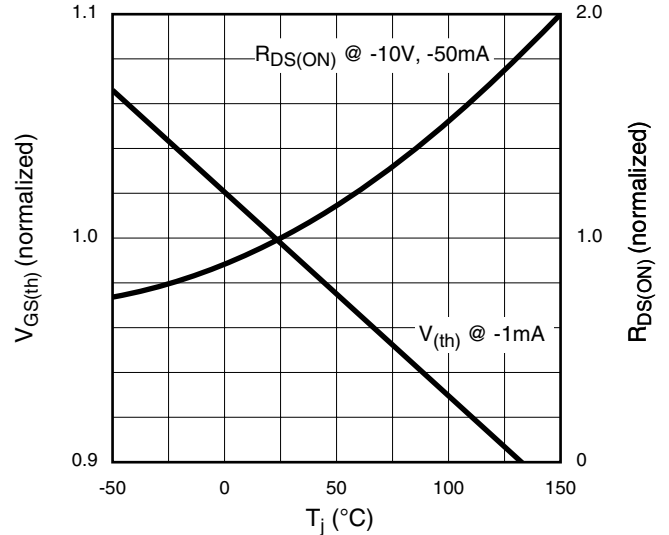
On-Resistance vs. Drain Current



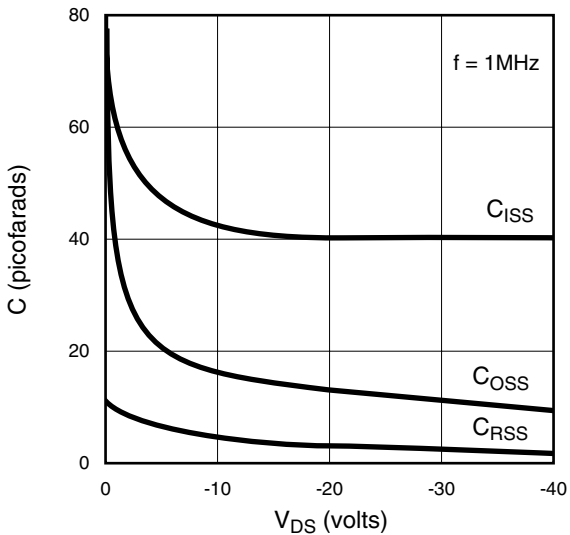
Transfer Characteristics



V<sub>(th)</sub> and R<sub>DS</sub> Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

