EPSON
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# S1F76540M0C Series
# Technical Manual

SEIKO EPSON CORPORATION

Rev.1.0

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# 1. DESCRIPTION

## 1.1 Description

S1F76540 consists of charge pump type DC/DC converter and voltage regulator with high efficiency and low power consumption using the CMOS process.

The charge pump type DC/DC converter uses four (three or two) external capacitors to negatively generate the output voltage, which is four times (triple or twice) higher than for the input voltage.

The voltage regulator uses two external resistors to set the output voltage generated by the DC/DC converter to any value and supply the regulated output voltage. If necessary, you can provide the negative temperature gradient characteristics to the regulated output voltage, and it is appropriate for LCD power.

S1F76540 turns the power off with an external signal, enabling you to reduce the wasteful current for system suspension. It is therefore appropriate for battery-driven portable devices.

## 1.2 Features

- Charge pump type DC/DC converter (negatively quadruple, triple, or double)
- Built-in voltage regulator (voltage stabilization output circuit)
- High-level conversion efficiency ····· 96% (VI= -5V, Typ.)
- Low consumption current ····· 100mA (VI= -5V, At quadruple boosting, Typ.)
- High output capability ····· 20mA (Max.)
- Input voltage range ····· -2.4 to -5.5V (At quadruple boosting)<br>-2.4 to -7.3V (At 3rd boosting)<br>-2.4 to -11V (At double boosting)
- DC/DC converter output voltage ····· Input voltage | × 4 (At quadruple boosting, Max.)
- Built-in for highly accurate regulator standard voltage ····· -1.5V±0.10V (At CT0)
- Regulator output voltage temperature gradient function ····· -0.05, -0.15, -0.35, -0.55 (%/°C)
- Standby current (At power-off) ····· 5μA (Max.)
- Adding external parts enables quintuple or more high-magnification booster and regulator.
- Power-off function by external signal
- Completely-self-contained oscillation circuit
- Compact and slim package product (SSOP2-16PIN)
- This IC is not designed for strong radiation activity proof.

# 2. BLOCK DIAGRAM

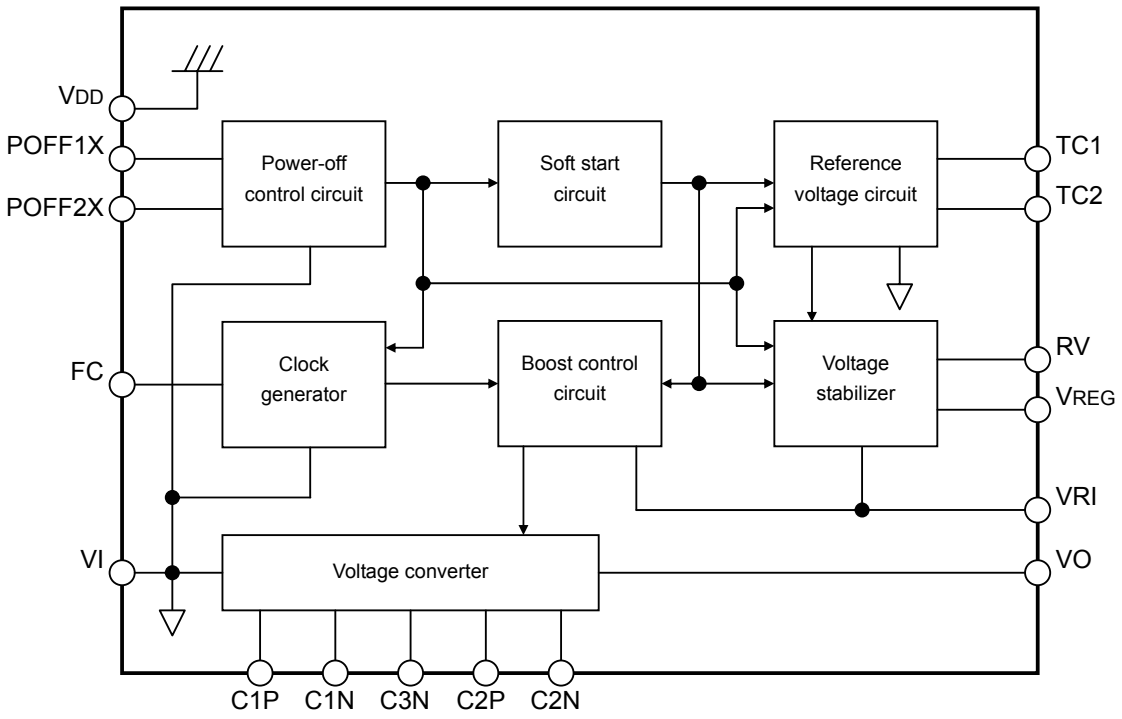



Fig.2.1 Block Diagram

# 3. PIN ASSIGNMENT

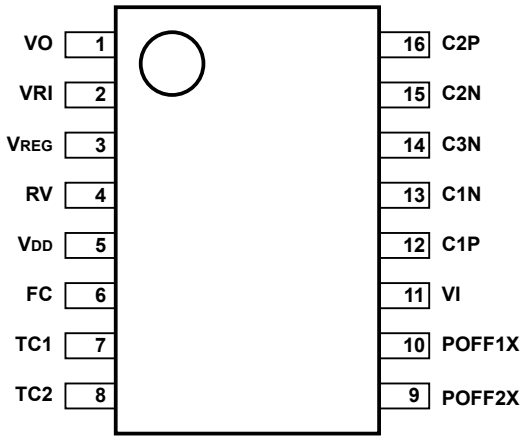



Fig.3.1 Pin assignment

# 4. PIN DESCRIPTION

Table 4.1 Pin Description

| Pin Name | Pin No. | Function |
|---|---|---|
| VO | 1 | Quadruple boosting output pin |
| VRI | 2 | Regulator input pin |
| $V_{REG}$ | 3 | Regulator output pin |
| RV | 4 | Input pin for adjusting the regulator output voltage |
| $V_{DD}$ | 5 | Power supply pin (+) |
| FC | 6 | Input pin for switching the internal clock frequency<br>Clock input pin at serial or parallel connection (Two-way pin) |
| TC1 | 7 | Input pin for specifying the regulator output temperature gradient (1) |
| TC2 | 8 | Input pin for specifying the regulator output temperature gradient (2) |
| POFF2X | 9 | Power-off control input pin (2) |
| POFF1X | 10 | Power-off control input pin (1) |
| VI | 11 | Power supply voltage (-) |
| C1P | 12 | Positive connect pin for double and quadruple boosting capacitor |
| C1N | 13 | Negative connect pin for double boosting capacitor |
| C3N | 14 | Negative connect pin for quadruple boosting capacitor |
| C2N | 15 | Negative connect pin for 3rd boosting capacitor |
| C2P | 16 | Positive connect pin for 3rd boosting capacitor |

# 5. FUNCTIONAL DESCRIPTION

## 5.1 Clock Generator

S1F76540, which contains a clock generator for boosting control, requires no external parts.

The clock frequency varies depending on the FC pin level (see Table 5.1), and you can select either the low output mode or high output mode. This results in you being able to select the clock frequency based on the load current and value of the capacitor to be used because the boosting output impedance varies depending on the clock frequency and the values of the external capacitors for boosting.

Table 5.1 FC pin settings

| FC pin | Mode name | Clock frequency | Selection judgment characteristics | | | |
|---|---|---|---|---|---|---|
| | | | Consumption current | Output ripple | Output impedance | Capacitor capacity |
| H($V_{DD}$) | Low output | 4.0kHz (Typ.) | IOP (Note 1) | VRP (Note 2) | See Fig.5.1 | See Fig.5.1 |
| L(VI) | High output | 16.0kHz (Typ.) | IOP (Note 1) | VRP (Note 2) | See Fig.5.1 | See Fig.5.1 |

(Note 1) For the consumption current value, see 7.1 DC Characteristics Table.
(Note 2) For information about how to define and roughly estimate the output ripple value, see 9.4.

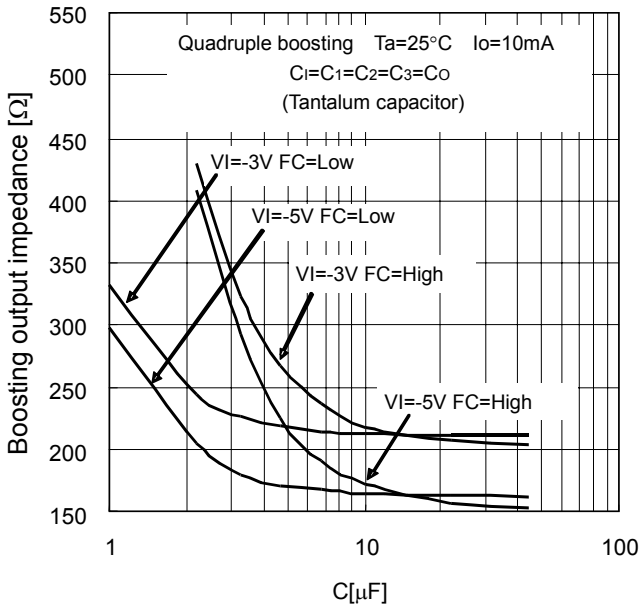



Fig.5.1 Capacitor capacity value - output impedance characteristics diagram

## 5.2 Voltage Converter

The voltage converter, which consists of boosting control circuit and voltage converter, boosts the input power supply voltage VI to four times (triple or double) using clocks from the clock generator. However, the 3rd or double boosting output cannot be obtained simultaneously with for the quadruple boosting. Fig.5.2 shows the potential relations at quadruple (3rd or double) boosting.

In the parallel connection, the C2P pin is used as a clock output pin in the master side (see Fig.9.8).

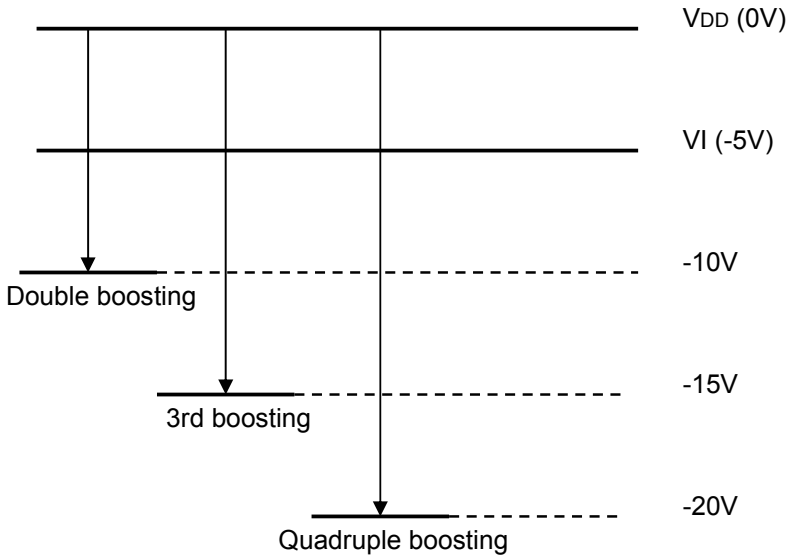



Fig.5.2 Boosting potential-relation diagram (At VI = -5V)

[Notes on connecting the capacitor for voltage conversion]

When connecting the capacitor to the C1P, C2P, C1N, C2N, C3N, and VO pins, place the capacitor near this IC so that the cable is as short as possible.

## 5.3 Reference Voltage Circuit

S1F76540 contains a reference voltage circuit for a voltage stabilization circuit (regulator).

The stabilizing potential described in Section 5.4 is defined with the split ratio between the external resistance and reference voltage values.

The reference voltage allows you to change the temperature coefficient using the TC1 and TC2 pins, and you can select one of four modes shown in Table 5.2.

Table 5.2 Reference voltage temperature coefficient settings

| Mode name | TC1 (H=$V_{DD}$) (L=VI) | TC2 (H=$V_{DD}$) (L=VI) | Reference voltage value $V_{REF}$(V) (Note 1) | | | Temperature coefficient CT (%/°C) (Note 2) | | |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. |
| CT0 | H | H | -1.60 | -1.5 | -1.40 | -0.07 | -0.05 | -0.03 |
| CT1 | H | L | -1.62 | -1.5 | -1.38 | -0.19 | -0.15 | -0.11 |
| CT2 | L | H | -1.65 | -1.5 | -1.35 | -0.42 | -0.35 | -0.28 |
| CT3 | L | L | -1.70 | -1.5 | -1.30 | -0.65 | -0.55 | -0.45 |

(Note 1) The reference voltage is based on Ta = 25°C.

(Note 2) The temperature gradient CT is defined in the following expression: In Table 5.2, the negative sign assigned to CT means that |$V_{REF}$| reduces as the temperature rises.

$$CT = \frac{|V_{REF}(50°C)| - |V_{REF}(0°C)|}{50°C - 0°C} \times \frac{100}{|V_{REF}(25°C)|}$$

(Note on switching the TC1 and TC2 pins)

When switching the TC1 and TC2 pins after power-on, be sure to turn the power off (POFF1X=POFF2X=VI).

## 5.4 Voltage Stabilizer

The voltage stabilizer stabilizes the voltage input to the VRI pin and outputs any voltage. The output voltage can be changed to any value based on the ratio between external split resistances R1 and R2 as shown in the expression (see Section 5.1). In this case, the sum of these split resistances should be as small as possible to limit influence of external noises; however, the current consumed for the split resistances will increase as shown in the expression (see Section 5.2). Therefore, the sum of split resistance values should be approximately 100Ω to 1MΩ.

The temperature coefficient of the stabilizing potential will become equal to that of the reference voltage described in Section 5.3.

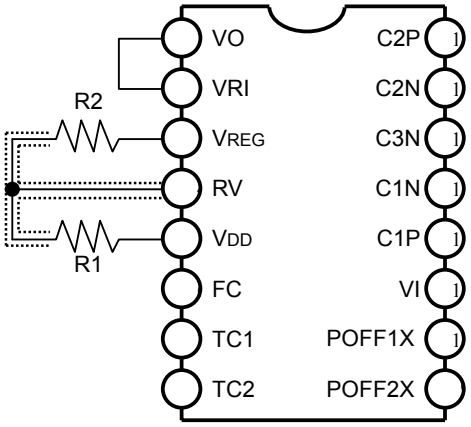



Fig.5.3 VREG setting method and assembly consideration

[Setting method]

• Relational expression between VREG and reference voltage

$$V_{REG} = \frac{R1+R2}{R1} \times \text{(Reference voltage)} \quad \cdots\cdots \text{Expression (5.1)}$$

• Consumption current for split resistances

$$I_{REG} = \frac{|V_{REG}|}{R1+R2} \quad \cdots\cdots \text{Expression (5.2)}$$

[Setting example]

The following shows a setting example for outputting VREG = -18V when VI = -5V and VO = -20V at quadruple boosting.

Determine the total resistor value of split resistances R1 and R2. If the allowable consumption current of the split resistances is 20μA, the following will be obtained from expression (5.2).

R1+R2 = 18V ÷ 20μA = 900kΩ

If the reference voltage is -1.5V, the following ratio of the split resistances will be obtained from expression (5.1).

(R1+R2) ÷ R1 = (-18V) ÷ (-1.5V) = 12

Therefore R1 and R2 will be determined as follows.

R1 = 75kΩ
R2 = 825kΩ

[Changing the temperature coefficient]

The temperature coefficient of the stabilizing potential depends on that of the reference voltage described in Section 5.3. (Case where the split ratio of resistance values for setting does not depend on the temperature) When setting the temperature coefficient other than that specifiable in S1F76540 to the stabilizing potential, change it using a thermistor resistor, etc. shown in Fig. 9.15.

The following shows how to obtain the VREG value at temperature T.

$$V_{REG}(T) = \{1+ \frac{CTR2 \times R2(T0)}{CTR1 \times R1(T0)} \times \{1+(T-T0) \times \frac{CT}{100}\} \times V_{REF}(T0) \quad \cdots\cdots \text{Expression (5.3)}$$

| | | |
|---|---|---|
| T0 | : | 25°C |
| CTR1 | : | Temperature coefficient of resistance R1 (Ratio between split resistance values at 25°C) |
| CTR2 | : | Temperature coefficient of resistance R2 (Ratio between split resistance values at 25°C) |
| CT | : | Temperature coefficient (%/°C) of internal reference voltage |
| R1(T0) | : | 25°R1 value (Ω) at 25°C |
| R2(T0) | : | 25°R2 value (Ω) at 25°C |
| VREF(T0) | : | 25°Internal reference voltage value (V) at 25°C |

If the temperature coefficient of R1 is equal to that of R2 in expression (5.3), VREG depends only on the temperature coefficient of the internal reference voltage.

[Notes on using the voltage stabilization circuit]

- To keep the S1F76540 absolute maximum rating, the setting resistor must be connected between VDD and VREG of an S1F76540 that uses the regulator. Connecting R1 to VDD of an S1F76540 that does not use the regulator when connecting the S1F76540 in series will result in deterioration or destruction in this IC.
- The stabilizing potential adjusting pin "RV" has the too high input impedance, which may result in the regulator being destabilized due to noises. When using this pin, shield the wiring section between the split resistor and RV pin, or shorten the wiring as much as possible (see Fig.5.3).
- When using the stabilizing power supply voltage pin "VRI", short-circuit the VRI and VO pins with a shorter cable (see Fig.5.3), exceeding at high-magnification boosting using an external diode shown in Section 9.8.

[Measures against oscillation]

Installing external parts enables you to take measures of oscillation.
The following shows the parts used and recommended values.

- Capacity between VREG and RV : 220pF
- Serial equivalent resistance of output capacitor CO : 10Ω or more (Note 1)

(Note 1) Specify the minimum necessary value because the ripple value of the output voltage increases. (See item 9.4.)

## 5.5 Power-off Control Circuit

S1F76540 provides the power-off function, which turns each function on and off by issuing the signals shown in Table 5.3 from the external system (microprocessor, etc.) to the POFF1X and POFF2X pins.

Using the power-off function, reactive current can be reduced in the application circuit connected in parallel.

When using the power-off function only in two states (all ON and all OFF), connect the POFF2X pin to VI; power-on and -off can be controlled using only one POFF1X pin.

Table 5.3 Combination of power-on and -off modes

| Mode name | POFF1X (H=$V_{DD}$) (L=$V_{IN}$) | POFF2X (H=$V_{DD}$) (L=$V_{IN}$) | Function state | | | |
|---|---|---|---|---|---|---|
| | | | Oscillation circuit | Booster | Regulator | Use |
| PS1 | H | L | ON | ON | ON | All circuit ON state |
| PS2 | L | L | OFF | OFF (Note 1) | OFF (Note 2) | All circuit OFF state |
| PS3 | H | H | OFF | ON | ON | Slave side in parallel connection (Booster + Regulator) |
| PS4 | L | H | ON | ON | OFF (Note 2) | Master side in parallel connection (Booster only) |

(Note 1) When the booster is off, the voltage of approximately VI+0.6V is generated in the VO pin.

(Note 2) When the regulator is off, the $V_{REG}$ pin is placed into the high impedance state.

[Notes on using the power-off function]

Before starting the power-off function with an external system signal, check that VI has been stabilized after power-on. Turning the power on or off before the power is not stabilized will result in a permanent destruction of this IC.

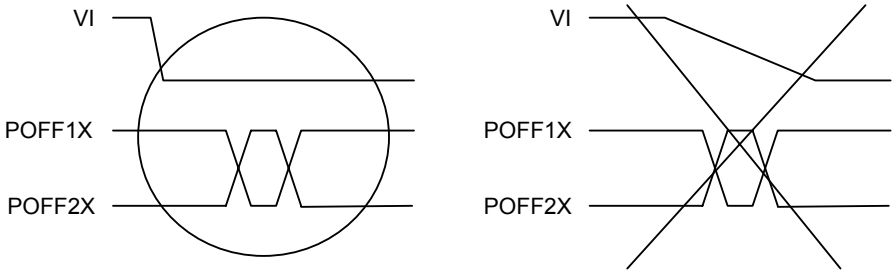



Fig.5.4 Power-off control start timing

## 5.6 Soft Start Circuit

The soft start circuit is used to minimize the peak value of the rush current at startup of the booster.

As shown in Fig.5.5, the maximum 200 ms (100mSec Typ.) after the input voltage VI has been input is set as the soft start period. During the soft start period, the VO output may not reach the electric potential that was boosted sufficiently.

In this case, the electric potential of the VO output is boosted smoothly up to the specified voltage after the soft start period has been expired.

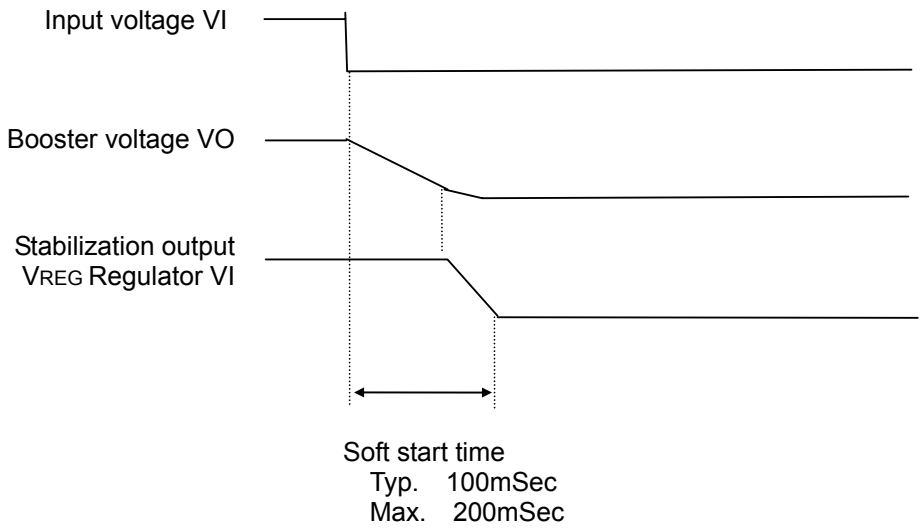



Fig.5.5 Soft start operation

**[Notes on connecting the capacitor for stabilizing the input voltage]**

**To stabilize the input voltage VI, the capacitor (CI) to be connected between the VDD and VI pins must be placed near the IC pin so that the wiring is as short as possible.**

# 6. ABSOLUTE MAXIMUM RATINGS

Table 6.1 Absolute maximum ratings

$V_{DD}$ reference

| Item | Symbol | Rated value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Input power voltage | VI | − 26.0/N | $V_{DD}$ + 0.3 | V | N = Boosting magnification<br>VI pin |
| Input pin voltage | VI | VI − 0.3 | $V_{DD}$ + 0.3 | V | POFF1X, POFF2X<br>TC1, TC2, FC pins |
| Output pin voltage 1 | VOC1 | VI − 0.3 | $V_{DD}$ + 0.3 | V | C1P, C2P pins |
| Output pin voltage 2 | VOC2 | 2 × VI − 0.3 | VI + 0.3 | V | C1N pin |
| Output pin voltage 3 | VOC3 | 3 × VI − 0.3 | 2 × VI + 0.3 | V | C2N pin |
| Output pin voltage 4 | VOC4 | 4 × VI − 0.3 | 3 × VI + 0.3 | V | C3N pin |
| Regulator input power supply voltage | VRI | N × VI − 0.3 | $V_{DD}$ + 0.3 | V | N = Boosting magnification,<br>VRI pin |
| Regulator input pin voltage | VRV | N × VI − 0.3 | $V_{DD}$ + 0.3 | V | N = Boosting magnification,<br>RV pin |
| Output voltage | VO | N × VI − 0.3 | $V_{DD}$ + 0.3 | V | N = Boosting magnification<br>$V_{OUT}$, $V_{REG}$ pins |
| Input current | IIN | — | 80 | mA | VI pin |
| Output Current | IO | — | N ≤ 4 : 20<br>N > 4 : 80/N | mA | N = Boosting magnification<br>$V_{OUT}$, $V_{REG}$ pins |
| Allowable dissipation | Pd | — | 210 | mW | Ta ≤ 25℃ |
| Operating temperature | Topr | − 40 | 85 | °C | — |
| Storage temperature | Tstg | − 55 | 150 | °C | — |
| Soldering temperature and time | Tsol | — | 260·10 | °C·S | Lead part |

(Note 1) Using with a condition exceeding the above absolute maximum rating may result in malfunction or unrecoverable damage. Moreover, normal function may be achieved temporarily but its reliability may be significantly low.

(Note 2) Potential relation with external system
The S1F76540 common power supply is set to the highest-level electric potential ($V_{DD}$). In this specifications, all the numeric values are represented based on $V_{DD}$=0V; therefore, be aware of the potential relation when connecting to an external system.

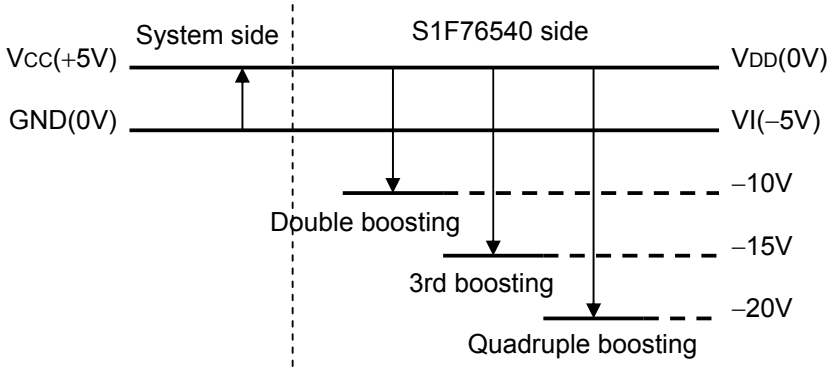



Fig.6.1 Electric potential relation diagram

# 7. ELECTRICAL CHARACTERISTICS MEASUREMENT STANDARD

## 7.1 DC Characteristics

Table 7.1 DC characteristics (1)

Ta = –40°C to +85°C, $V_{DD}$=0V, VI=-5.0V unless otherwise specified.

| Item | Symbol | Conditions | Min | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input power voltage | VI | N: Boosting magnification for CT0 | –22/N | — | –2.4 | V |
| | | N: Boosting magnification for CT1 | –22/N | — | –2.4 | V |
| | | N: Boosting magnification for CT2 | –22/N | — | –2.4 | V |
| | | N: Boosting magnification for CT3 | –22/N | — | –2.4 | V |
| Boosting start input power supply voltage | VSTA | N: Boosting magnification,<br>FC = $V_{DD}$, at no-load | –22/N | — | –2.4 | V |
| Boosting output voltage | VO | — | –22 | — | — | V |
| Regulator input voltage | VRI | — | –22 | — | –2.8 | V |
| Regulator output voltage | $V_{REG}$ | $I_{REG}$ = 0, VRI = –22V<br>RRV = 1MΩ | — | — | –2.8 | V |
| Boosting output impedance | RO | IO = 10mA (At quadruple boosting)<br>VI = –5.0V<br>C1, C2, C3, C0 = 10µF<br>(Tantalum capacitor)* | — | 180 | 270 | Ω |
| | | IO = 10mA (At quadruple boosting)<br>VI = –3.0V<br>C1, C2, C3, C0 = 10µF<br>(Tantalum capacitor)* | — | 230 | 350 | Ω |
| Boosting power conversion efficiency | Peff | IO = 2mA (At quadruple boosting)<br>VI = –5.0V<br>C1, C2, C3, C0 = 10µF<br>(Tantalum capacitor)* | — | 96 | — | % |
| | | IO = 2mA (At quadruple boosting)<br>VI = –3.0V<br>C1, C2, C3, C0 = 10µF<br>(Tantalum capacitor)* | — | 95 | — | % |
| Booster operation consumption current 1 | IOPR1 | FC = $V_{DD}$, POFF1X = VI<br>POFF2X = $V_{DD}$<br>VIN = –5.0V, at no-load<br>C1, C2, C3, C0 = 1µF<br>(Tantalum capacitor)* | — | 100 | 170 | µA |
| | | FC = $V_{DD}$, POFF1X = VI<br>POFF2X = $V_{DD}$<br>VI = –3.0V, at no-load<br>C1, C2, C3, C0 = 10µF<br>(Tantalum capacitor)* | — | 70 | 120 | µA |
| Booster operation consumption current 2 | IOPR2 | FC = $V_{DD}$, POFF1X = VI<br>POFF2X = $V_{DD}$<br>VI = –5.0V, at no-load<br>C1, C2, C3, C0 = 10µF<br>(Tantalum capacitor)* | — | 260 | 440 | µA |
| | | FC = $V_{DD}$, POFF1X = VI<br>POFF2X = $V_{DD}$<br>VIN = –3.0V, at no-load<br>C1, C2, C3, C0 = 10µF<br>(Tantalum capacitor)* | — | 160 | 270 | µA |
| Regulator operation consumption current | IOPVR | VRI = –20V, at no-load<br>RRV = 1MΩ | — | 7 | 15 | µA |
| Static current | IQ | POFF1X = VI、POFF2X = VI、FC = $V_{DD}$ | — | — | 5.0 | µA |
| Input leak current | ILKI | Applied pins: POFF1X, POFF2X, FC, TC1, and TC2 | — | — | 0.5 | µA |

Table 7.2 DC characteristics (2)

$V_{DD}$= 0V, VI= –5.0V

| Item | Symbol | Conditions | Min | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Stabilization-output saturated resistance | RSAT (Note 1) | 0 < $I_{REG}$ < 20mA<br>RV = $V_{DD}$, Ta = 25℃ | — | 6 | 10 | Ω |
| Stability of regulated output voltage | ΔVR (Note 2) | –20V < VR < –10V<br>$I_{REG}$ = 1mA, $V_{REG}$ = –9V setting | — | — | 0.2 | %/V |
| Stabilization-output load change | ΔVO (Note 3) | 0 < $I_{REG}$ < 20mA<br>VRI =–20V, $V_{REG}$ = –15V setting | — | 15 | 50 | mV |
| Reference voltage (Ta=25°C) | VREF0 | TC1 = $V_{DD}$, TC2 = $V_{DD}$ | –1.60 | –1.50 | –1.40 | V |
| | VREF1 | TC1 = $V_{DD}$, TC2 = VI | –1.62 | –1.50 | –1.38 | V |
| | VREF2 | TC1 = VI, TC2 = $V_{DD}$ | –1.65 | –1.50 | –1.35 | V |
| | VREF3 | TC1 = VI, TC2 = VI | –1.70 | –1.50 | –1.30 | V |
| Reference voltage temperature coefficient (Note 4) | CT0 | TC1 = $V_{DD}$, TC2 = $V_{DD}$<br>SSOP product | –0.06 | –0.04 | –0.02 | %/°C |
| | CT1 | TC1 = $V_{DD}$, TC2 = VI<br>SSOP product | –0.19 | –0.15 | –0.11 | %/°C |
| | CT2 | TC1 = VI, TC2 = $V_{DD}$<br>SSOP product | –0.42 | –0.35 | –0.28 | %/°C |
| | CT3 | TC1 = VI, TC2 = VI<br>SSOP product | –0.65 | –0.55 | –0.45 | %/°C |
| Input voltage level | VIH | VI = –2.4V to –5.5V<br>Applied pins: POFF1X, POFF2X, FC, TC1, TC2 | 0.2VI | — | — | V |
| | VIL | VI = –2.4V to –5.5V<br>Applied pins: POFF1X, POFF2X, FC, TC1, TC2 | — | — | 0.8VI | V |
| Capacity value of boosting capacitor | CMAX | Applied capacitor<br>C1, C2, C3 | — | — | 47 | μF |

* The characteristics vary depending on the external capacitor. Before determining constants, conduct the evaluation of the characteristics.

$$\text{(Note 1) } RSAT = \frac{V_{REG}(I_{REG}=20mA) - V_{REG}(I_{REG}=0mA)}{\Delta I_{REG}}$$

$$\text{(Note 2) } \Delta VR = \frac{V_{REG}(VRI=-20V) - V_{REG}(VRI=10V)}{\Delta VRI \times V_{REG}(VRI=-10V)}$$

$$\text{(Note 3) } \Delta VO = V_{REG}(I_{REG}=20mA) - V_{REG}(I_{REG}=0mA)$$

$$\text{(Note 4) } CT = \frac{|V_{REG}(Ta=50°C)| - |V_{REG}(Ta=0°C)}{50°C - 0°C} : \frac{|V_{REG}(Ta=25°C)|}{100}$$

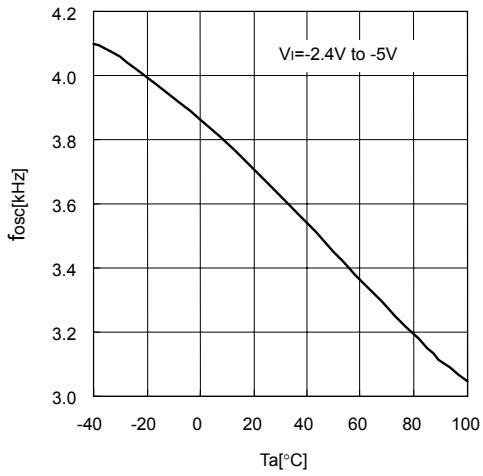
## 7.2 AC Characteristics

Table 7.2 AC Characteristics

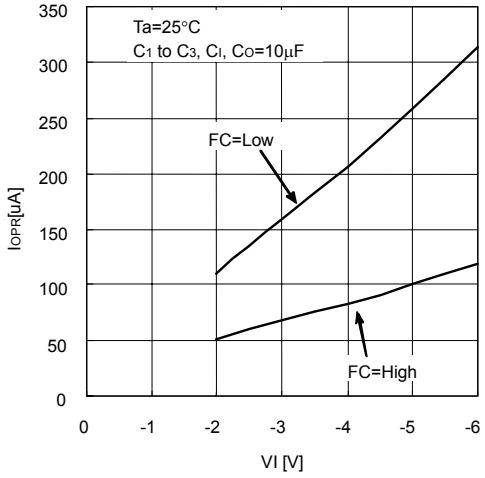
Unless otherwise noted: $V_{DD}$=0V, VI=–5.0V

| Item | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Internal clock frequency 1 | $f_{CL1}$ | FC = $V_{DD}$<br>POFF1X= VI<br>POFF2X = $V_{DD}$<br>Applied pin: C1P | Ta=25°C | 3.0 | 4.0 | 5.0 | kHz |
| | | | Ta= –40°C to +85°C | 2.0 | 4.0 | 6.0 | kHz |
| Internal clock frequency 2 | $f_{CL2}$ | FC = VI<br>POFF1X = VI<br>POFF2X= $V_{DD}$<br>Applied pin: C1P | Ta=25°C | 12.0 | 16.0 | 20.0 | kHz |
| | | | Ta= –40°C to +85°C | 8.0 | 16.0 | 24.0 | kHz |

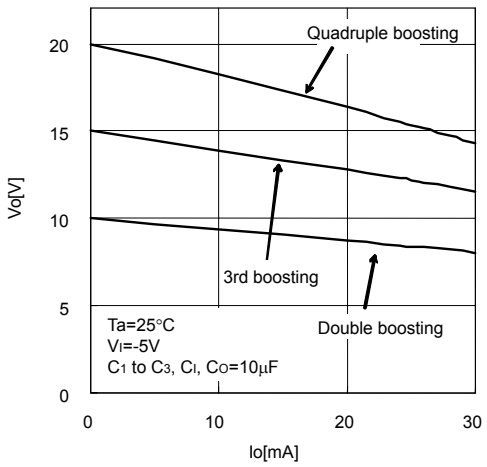
# 8. CHARACTERISTICS GRAPHS



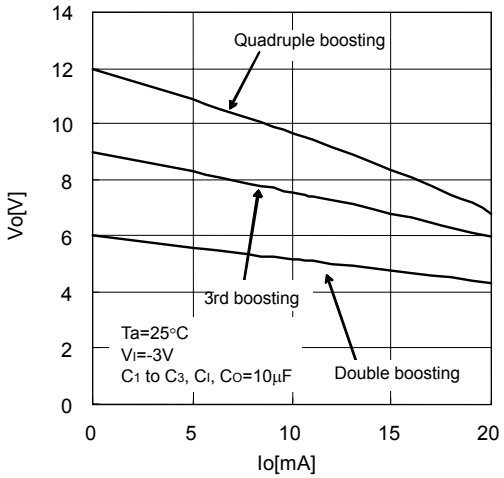

(1) Internal clock frequency 1 - Temperature




(2) Booster operation consumption current - Input Voltage

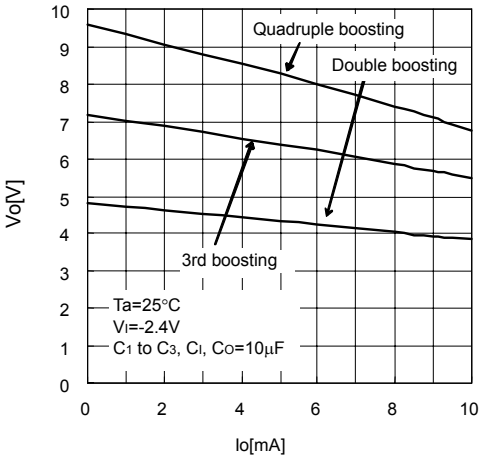



(3) Boosting output (Vo) - Output current ①

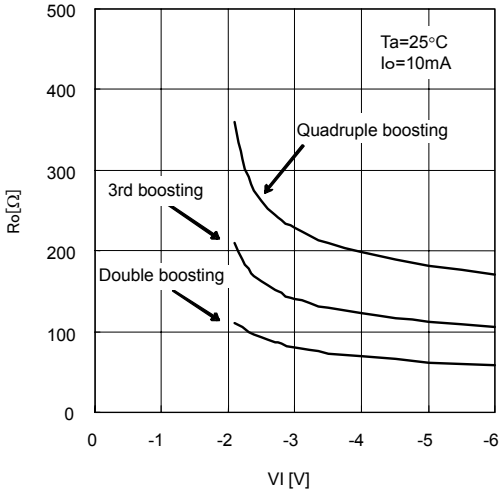



(4) Boosting voltage (Vo) - Output current ②

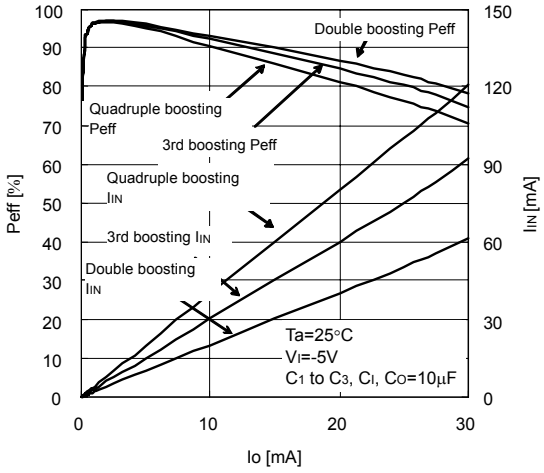
## 8. CHARACTERISTICS GRAPHS



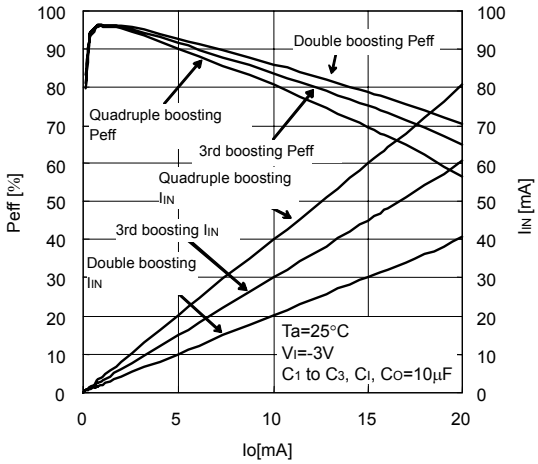

(5) Output voltage (Vo) - Output current ③



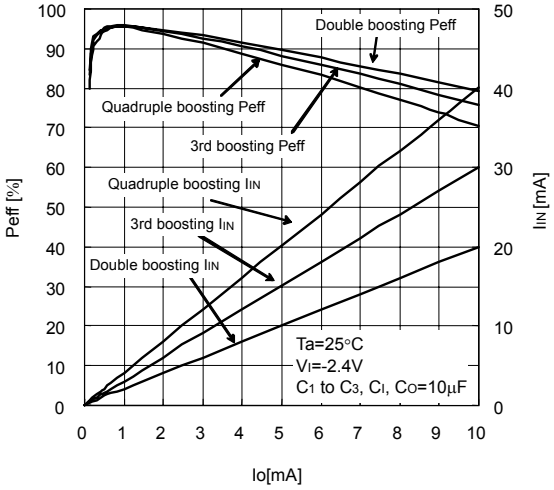

(6) Boosting output impedance - Input voltage



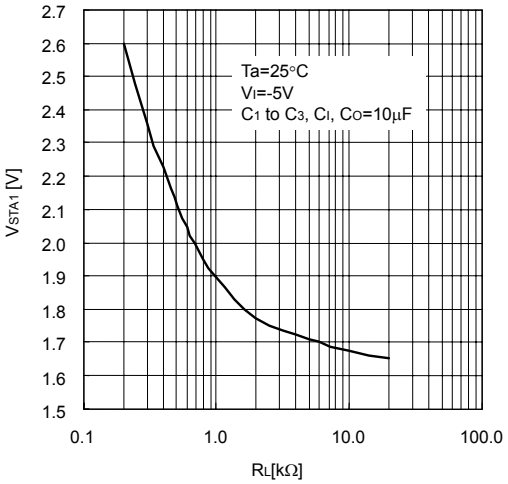

(7) Boosting power conversion efficiency - Output current ①
Input current - Output current ①



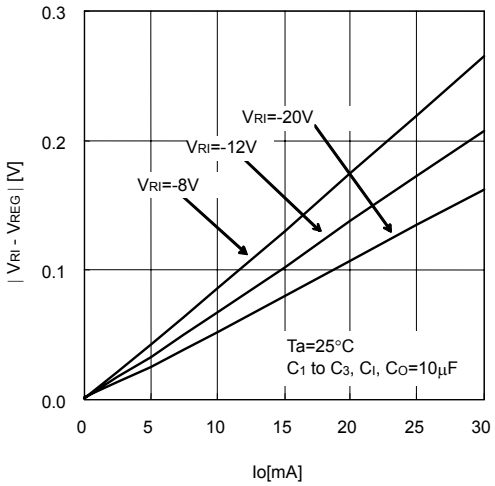

(8) Boosting power conversion efficiency - Output current ②
Input current - Output current ②



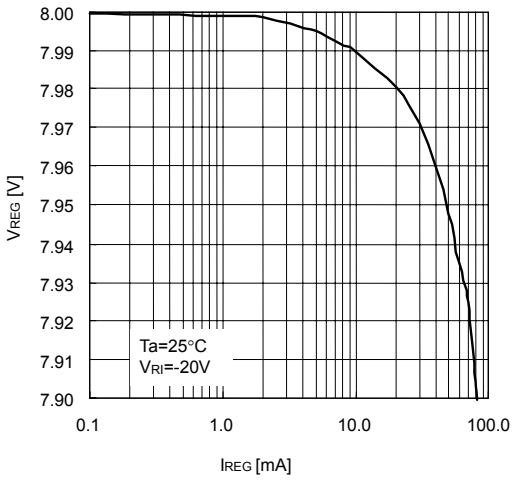

(9) Boosting power conversion efficiency - Output current ③
Input current - Output current ③



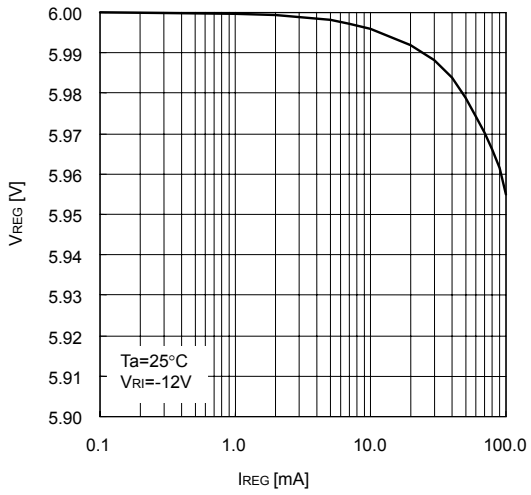

(10) Boosting start input power supply voltage - Load resistance



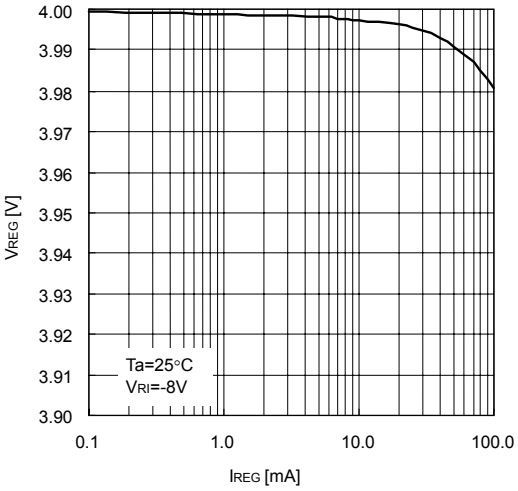

(11)Output voltage lowering - Load current



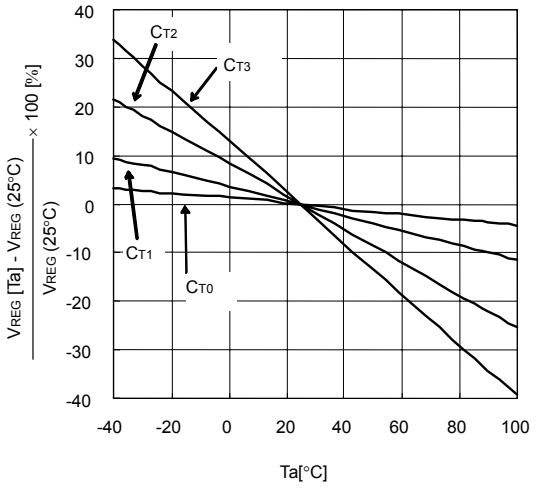

(12) Output voltage (VREG) - Output current ①



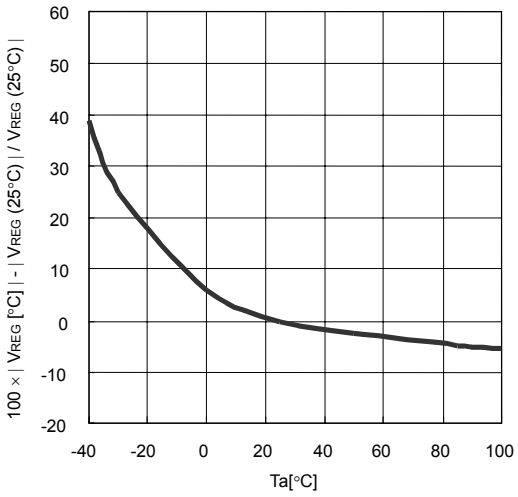

(13) Output voltage (VREG) - Output current ②




(14) Output voltage (VREG) - Output current ③




(15) Reference voltage - Temperature gradient




(16) Regulator temperature coefficient - Temperature

# 9. REFERENCE: EXTERNAL CONNECTION EXAMPLES

## 9.1 Quadruple Boosting + Regulator

Fig.9.1 shows a "quadruple boosting + regulator" connection example that is standard in S1F76540. Perform quadruple boosting in the negative direction for input voltage VI, and generate the stabilized voltage in the VREG pin.

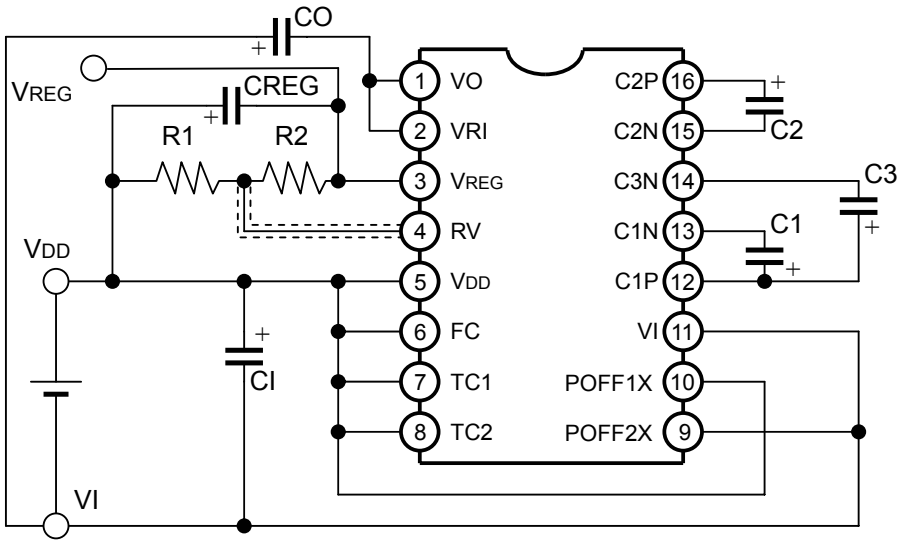



Fig.9.1 Quadruple boosting + regulator connection example

◇ Fig.9.1 Setting conditions
- Internal clock : ON (Low output mode)
- Booster : ON
- Regulator : ON (Select CT0 = -0.05%/°C.)

◇ Power-off method
Set the POFF1X pin to level LOW (VI); all circuits will be turned off.

◇ About regulator
For information about the regulator setting method and notes, see Section 5.4.

◇ Other setting conditions
① When using the high output mode
Connect the FC pin to VI.
② When changing the temperature coefficient CT
Change the TC1 and TC2 pins as shown in Table 5.3.

## 9.2 3rd Boosting + Regulator

Perform 3rd boosting in the negative direction for input voltage VI, and generate the stabilized voltage in the VREG pin.

Fig.9.2 shows a connection example.

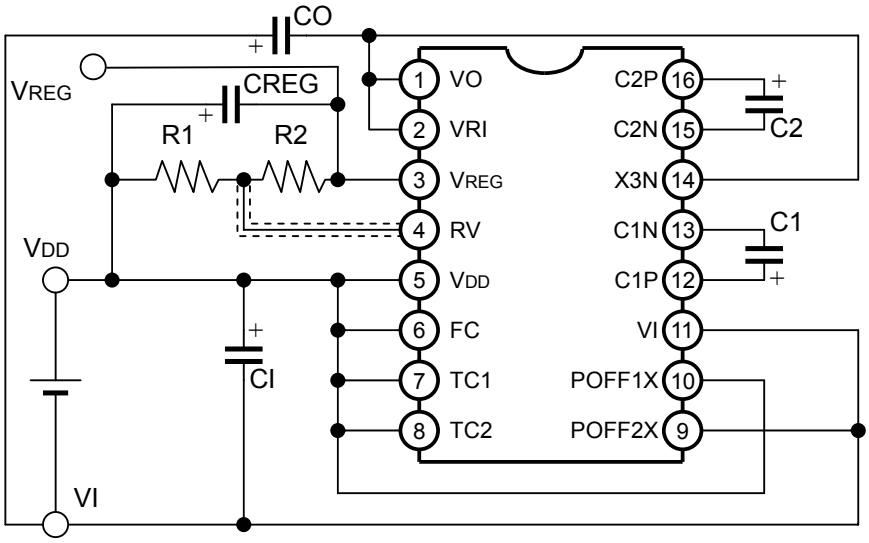



Fig.9.2 3rd boosting + regulator connection example

◇ Fig.9.2 Setting conditions
- Internal clock : ON (Low output mode)
- Booster : ON
- Regulator : ON (Select CT0 = -0.05%/°C.)

◇ Power-off method

Set the POFF1X pin to level LOW (VI); all circuits will be turned off.

◇ About regulator

For information about the regulator setting method and notes, see Section 5.4.

◇ Other setting conditions

① When using the high output mode
Connect the FC pin to VI.

② When changing the temperature coefficient CT
Change the TC1 and TC2 pins as shown in Table 5.3.

## 9.3 Double Boosting + Regulator

Perform double boosting in the negative direction for input voltage VI, and generate the stabilized voltage in the VREG pin.

Fig.9.3 shows a connection example.

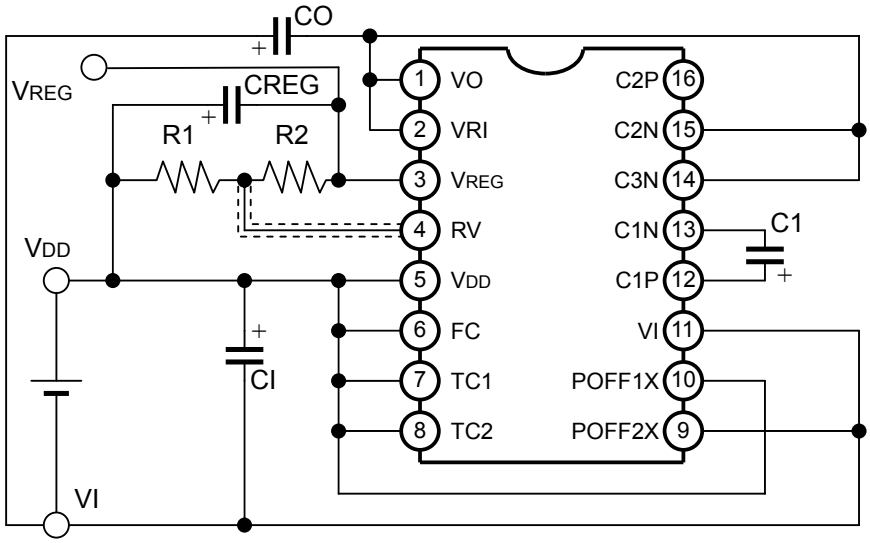



Fig.9.3 Double boosting + regulator connection example

◇ Fig.9.3 Setting conditions
- Internal clock : ON (Low output mode)
- Booster : ON
- Regulator : ON (Select CT0 = -0.05%/°C.)

◇ Power-off method
Set the POFF1X pin to level LOW (VI); all circuits will be turned off.

◇ About regulator
For information about the regulator setting method and notes, see Section 5.4.

◇ Other setting conditions
① When using the high output mode
Connect the FC pin to VI.
② When changing the temperature coefficient CT
Change the TC1 and TC2 pins as shown in Table 5.3.

## 9.4 Quadruple Boosting

Run only the booster, perform quadruple boosting in the negative direction for input voltage VI, and generate the voltage in the VO pin.

In this case, the regulator is not used, so the voltage containing ripple components is generated in the VO pin.

Fig.9.4 shows a connection example.

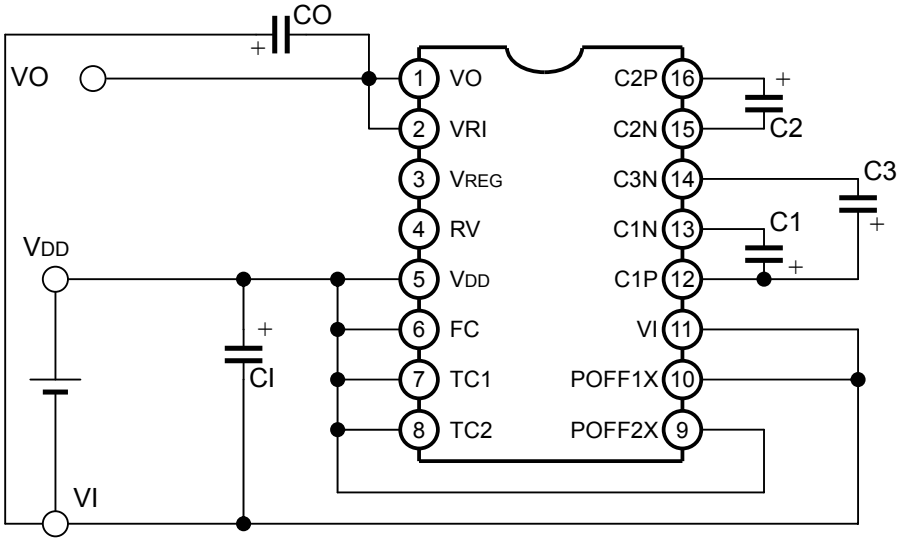



Fig.9.4 Quadruple boosting connection example

◇ Fig.9.4 Setting conditions
- Internal clock : ON (Low output mode)
- Booster : ON
- Regulator : OFF

◇ Power-off method

Set the POFF2X pin to level LOW (VI); all circuits will be turned off.

◇ About ripple voltage

The output voltage to be generated in the VO pin is not stabilized; therefore, it contains the ripple components shown in Fig.9.5. The ripple voltage VRP increases depending on the load current, and the approximate value can be obtained in expression (9.1).


Fig.9.5 Ripple waveform chart

$$VRP = \frac{IO}{2 \cdot fCL \cdot CO} + IO \times RCO \quad \cdots\cdots\cdots \text{Expression (9.1)}$$

IO : Load current (A)
fCL : Clock frequency (Hz)
RCO : Serial equivalent resistance (Ω) of output capacitor CO

◇ Other setting conditions

① When using the high output mode

Connect the FC pin to VI.

## 9.5 3rd Boosting

Run only the booster, perform 3rd boosting in the negative direction for input voltage VI, and generate the voltage in the VO pin.

In this case, the regulator is not used, so the voltage containing ripple components is generated in the VO pin.

Fig.9.6 shows a connection example.

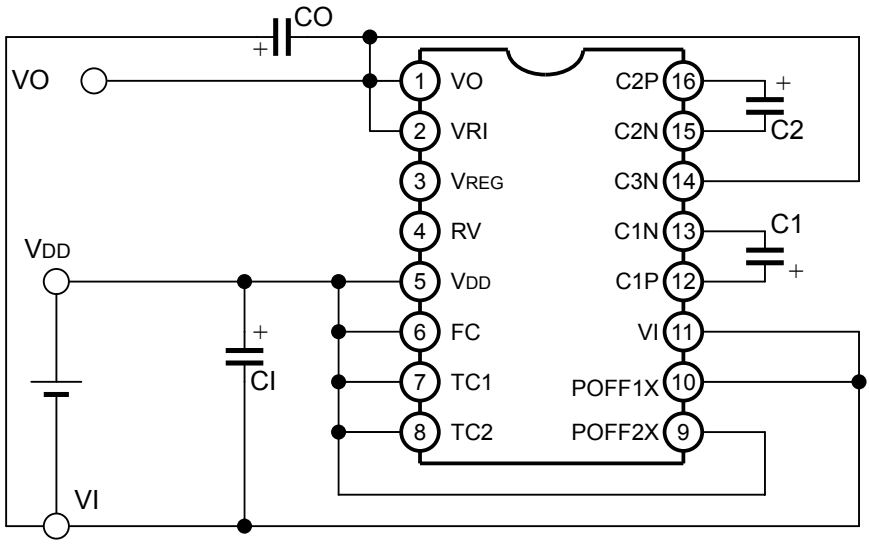



Fig.9.6 3rd boosting connection example

◇ Fig.9.6 Setting conditions
- Internal clock : ON (Low output mode)
- Booster : ON
- Regulator : OFF

◇ Power-off method

Set the POFF2X pin to level LOW (VI); all circuits will be turned off.

◇ About ripple voltage

For ripple voltage, see Section 9.4.

◇ Other setting conditions

① When using the high output mode

Connect the FC pin to VI.

## 9.6 Double Boosting

Run only the booster, perform double boosting in the negative direction for input voltage VI, and generate the voltage in the VO pin.

In this case, the regulator is not used, so the voltage containing ripple components is generated in the VO pin.

Fig.9.7 shows a connection example.

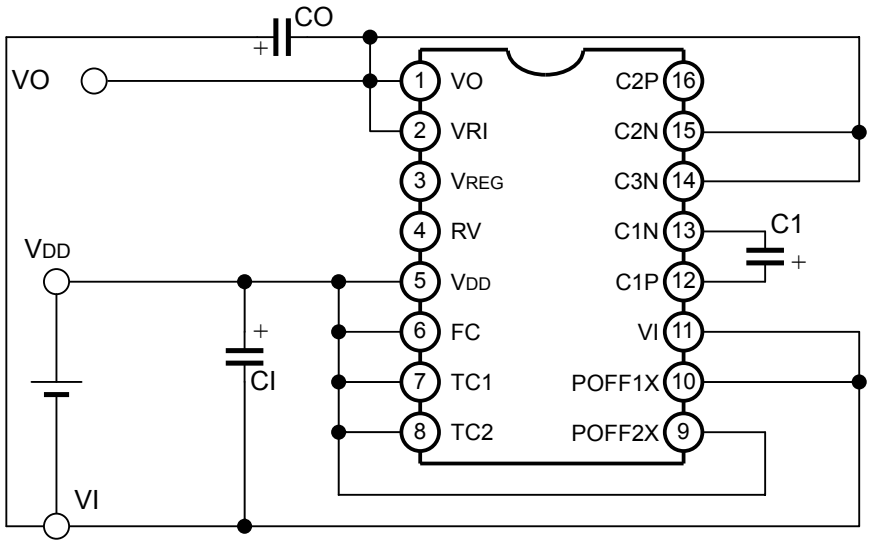



Fig.9.7 Double boosting connection example

◇ Fig.9.7 Setting conditions
- Internal clock : ON (Low output mode)
- Booster : ON
- Regulator : OFF

◇ Power-off method

Set the POFF2X pin to level LOW (VI); all circuits will be turned off.

◇ About ripple voltage

For ripple voltage, see Section 9.4.

◇ Other setting conditions

① When using the high output mode

Connect the FC pin to VI.

## 9.7 Parallel Connection (Boosting Capacity Increase)

The parallel connection is effective when lowering the boosting output impedance or reducing the ripple voltage. Connecting n S1F76540s in parallel sets the boosting output impedance to approximately 1/n. Only the smoothing capacitor CO for boosting output can be shared even in parallel connection.

Using the regulator allows you to operate only one of n S1F76540s that are connected in parallel. (Running multiple regulators in parallel will generate the reactive consumption current.)

Fig.9.8 shows a "quadruple boosting + regulator" connection example where two S1F76540s are connected in parallel.

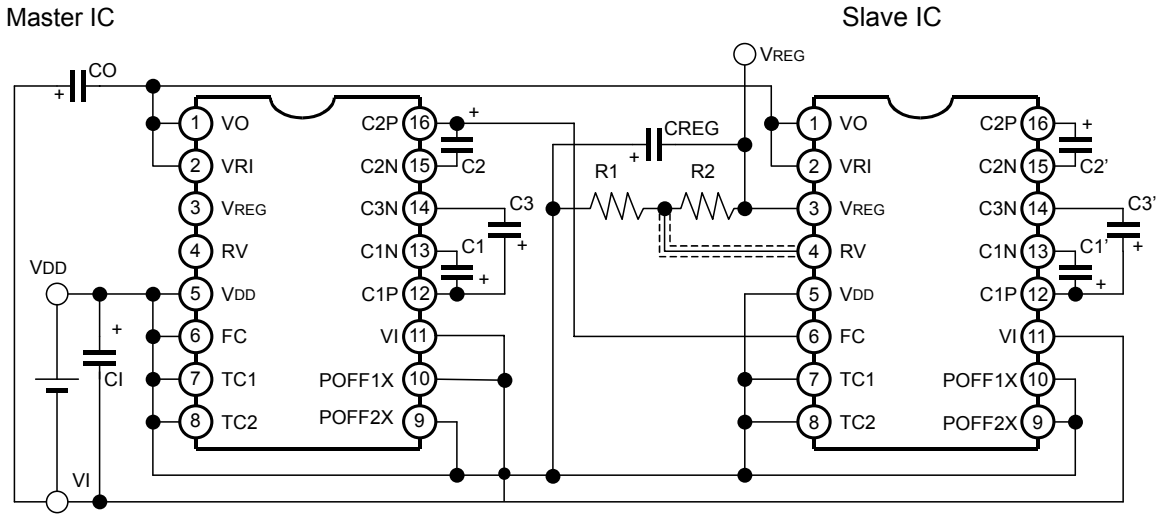



Fig.9.8 Parallel connection example

◇ Fig.9.8 Setting conditions

| Master IC | | | Slave IC | | |
|---|---|---|---|---|---|
| ・ Internal clock | : | ON (Low output mode) | ・ Internal clock | : | OFF (Clocks supplied from master IC) |
| ・ Booster | : | ON | ・ Booster | : | ON |
| ・ Regulator | : | OFF | ・ Regulator | : | ON (Select CT0 = -0.05%/°C.) |

◇ Power-off method

In the connection example shown in Fig.9.8, setting S1F76540 in the master IC to POFF2X = L (VI) enables you to stop boosting the master and slave ICs; however, the regulator in the slave IC does not stop.

When |VREG| is greater than |VI|, the voltage that is equivalent to VI is generated in the VREG pin.

When placing the VREG pin into the high impedance state, set both the master and slave ICs to POFF1X = L and POFF2X = L.

◇ Other setting conditions

① When using the high output mode
Connect the FC pin in the master IC to VI.

② When changing the temperature coefficient CT
Change the TC1 and TC2 pins in the slave IC as shown in Table 5.3.

## 9.8 High-Magnification Boosting Using a Diode

Loading an external diode in S1F76540 enables the "quintuple or more boosting + regulator" connection. Using the forward voltage lowering VF in a diode raises the boosting output impedance; therefore, you should load a diode with the lower VF value.

### 9.8.1 Quintuple Boosting + Regulator

Fig.9.9 shows a "quintuple boosting + regulator" connection example with one diode used. The cable from VO to VRI must be as short as possible. Fig.9.10 shows the electric potential relation diagram.

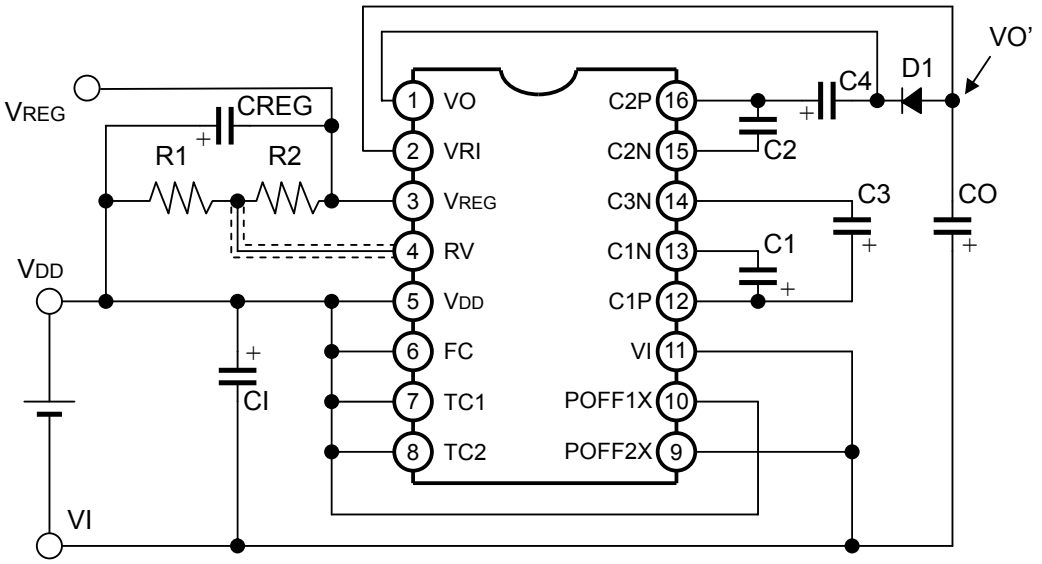



Fig.9.9 Quintuple boosting connection example using one diode

◇ Fig.9.9 Setting conditions
- Internal clock : ON (Low output mode)
- Booster : ON
- Regulator : ON (Select CT0 = -0.05%/°C.)

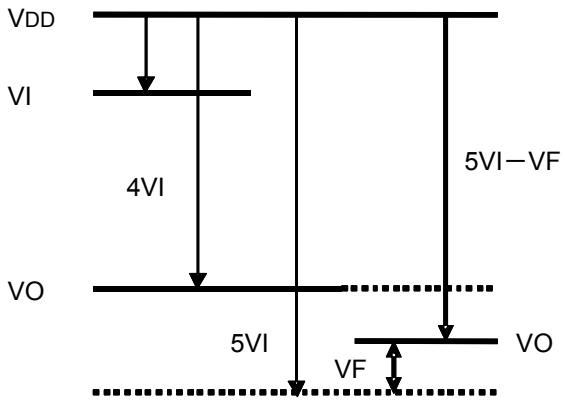



Fig.9.10 Quintuple-boosting potential relation using one diode

◇ Power-off method

Set the POFF1X pin to level LOW (VI); all circuits will be turned off.

◇ Output voltage

When loading a diode for boosting, the diode characteristics directly affect the boosting characteristics. Especially using the VF pin (forward voltage lowering) in a diode causes the boosting output voltage to be reduced. In the connection example shown in Fig.9.9, one diode is used; therefore, be sure to drop the voltage by VF as shown in Fig.9.10. The boosting output voltage is indicated in the following expression.

When increasing | VO' |, use a diode with the lower VF value.

$$| VO' | = 5\times | VI | - VF \quad \cdots\cdots\cdots \quad \text{Expression (9.2)}$$

◇ Precautions

① Input and output current conditions

To keep the input and output current ratings, multiply the entire boosting magnification by the output load current value so that it does not exceed the input current rating when performing high-magnification boosting using a diode.

In the example shown in Fig.9.9, "80mA ÷ 5 = 16mA" is used as the maximum load current.

② Input and output voltage conditions

To keep the input and output voltage ratings, be aware of the potential relation when performing high-magnification boosting using a diode.

In the circuit shown in Fig.9.9, VI must satisfy input voltage conditions (see Table 7.1) at quintuple boosting.

◇ Other setting conditions

① When using the high output mode

Connect the FC pin to VI.

② When changing the temperature coefficient CT

Change the TC1 and TC2 pins as shown in Table 5.3.

### 9.8.2 Sextuple Boosting + Regulator

Fig.9.11 shows a "sextuple boosting + regulator" connection example with two diodes used. The cable from VO to VRI must be as short as possible. Fig.9.12 shows the electric potential relation diagram.

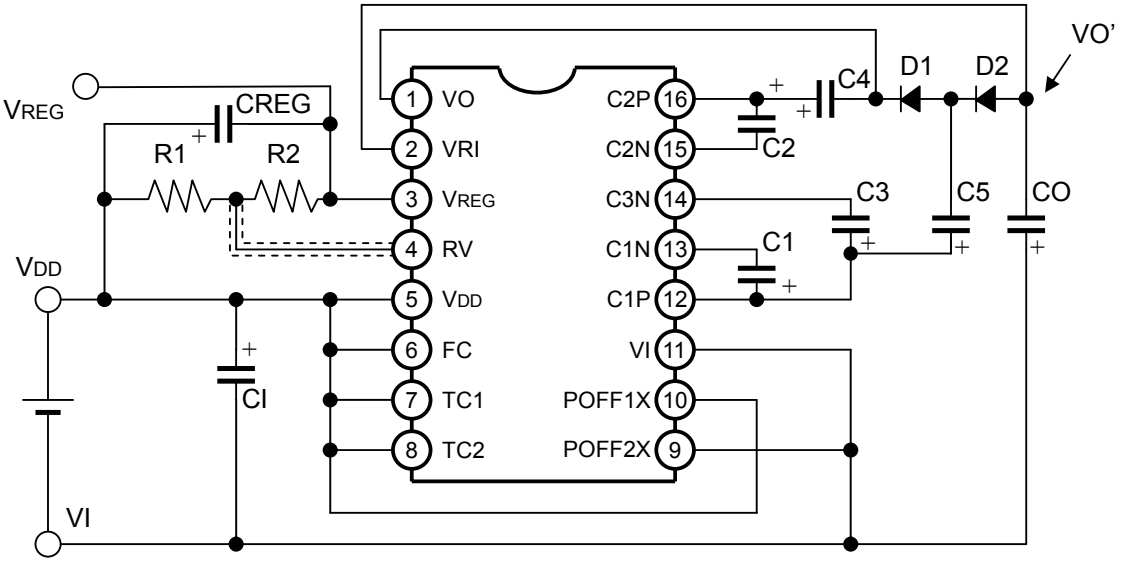



Fig.9.11 Sextuple boosting connection example using two diodes

◇ Fig. 9.11 Setting conditions
- Internal clock : ON (Low output mode)
- Booster : ON
- Regulator : ON (Select CT0 = -0.05%/°C.)

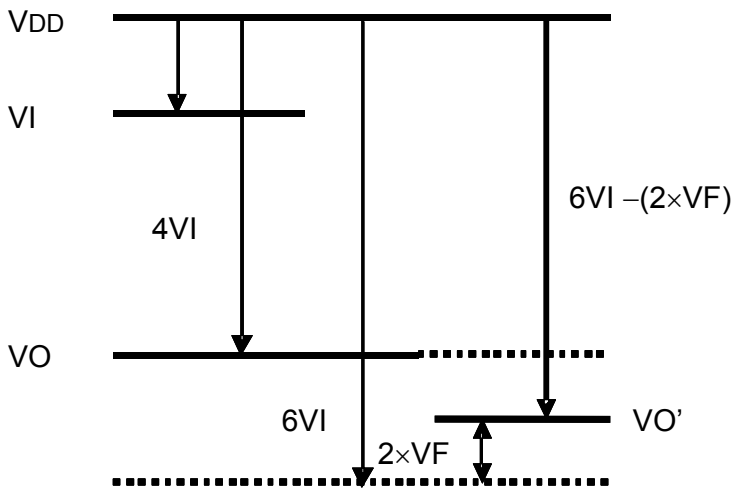



Fig.9.12 Sextuple-boosting potential relation using two diodes

◇ Power-off method

Set the POFF1X pin to level LOW (VI); all circuits will be turned off.

◇ Output voltage

When loading diodes for boosting, the diode characteristics directly affect the boosting characteristics. Especially using the VF pin (forward voltage lowering) in a diode causes the boosting output voltage to be reduced. In the example shown in Fig.9.11, two diodes are used; therefore, be sure to drop the voltage by 2 × VF as shown in Fig.9.12. The boosting power voltage is indicated in the following expression.

When increasing | VO' | , use a diode with the lower VF value.

$$| VO' | = 6\times | VI | -2\times VF \quad \cdots\cdots\cdots \quad \text{Expression (9.3)}$$

◇ Precautions

① Input and output current conditions

To keep the input and output current ratings, multiply the entire boosting magnification by the output load current value so that it does not exceed the input current rating when performing high-magnification boosting using diodes.

In the example shown in Fig.9.11, "80mA ÷ 6 = 13.3mA" is used as the maximum load current.

② Input and output voltage conditions

To keep the input and output voltage ratings, be aware of the potential relation when performing high-magnification boosting using a diode.

In the circuit shown in Fig.9.11, VI must satisfy input voltage conditions (see Table 7.1) at sextuple boosting.

◇ Other setting conditions

① When using the high output mode

Connect the FC pin to VI.

② When changing the temperature coefficient CT

Change the TC1 and TC2 pins as shown in Table 5.3.

## 9.9 Positive Voltage Converter

S1F76540 boosts to the positive electric potential side using an external diode; however, it cannot use the regulator function.

Fig.9.13 shows a "positive 3rd boosting" connection example, and Fig.9.14 shows the electric potential relation diagram.

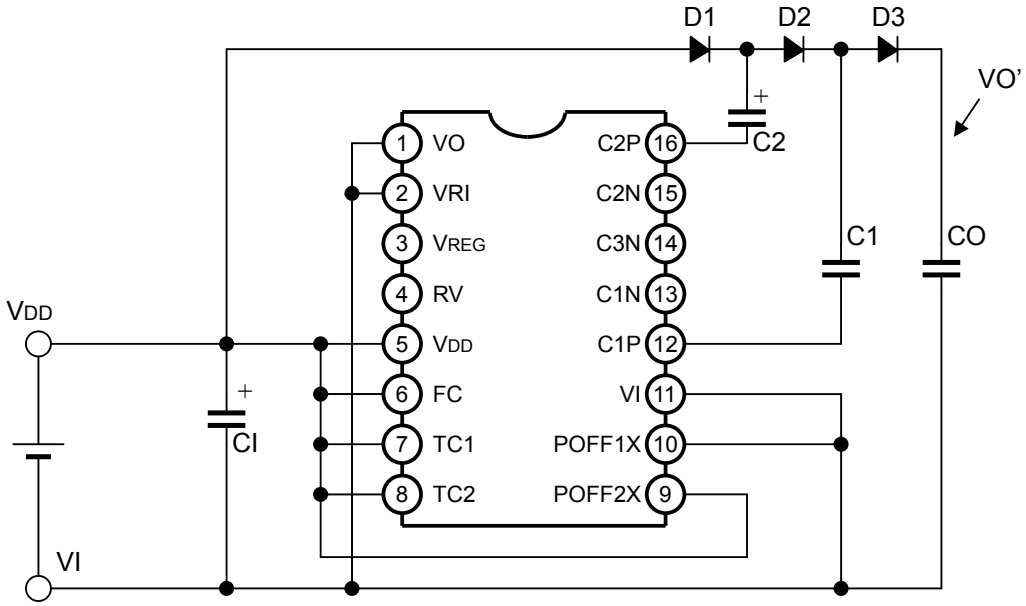



Fig.9.13 Positive voltage conversion connection example (3rd boosting)

◇ Fig.9.14 Setting conditions
- Internal clock : ON (Low output mode)
- Booster : ON
- Regulator : OFF

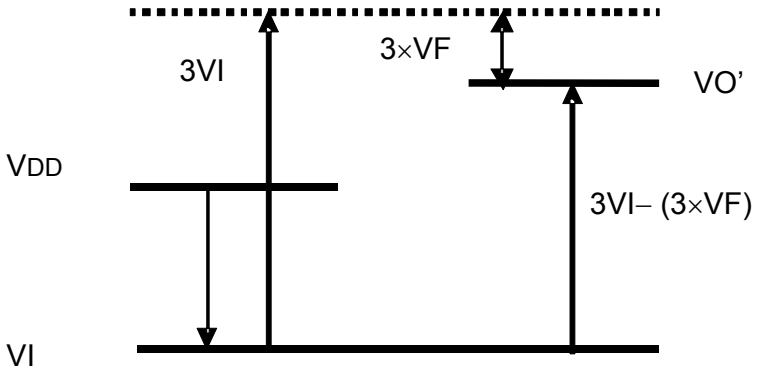



Fig.9.14 Electric potential relation diagram of positive voltage conversion connection example (3rd boosting)

◇ Power-off method

Set the POFF2X pin to level LOW (VI); all circuits will be turned off.

◇ For double boosting:

When performing double boosting, delete C2 and D1 shown in Fig.9.13, and connect the D2 anode (positive pole) side to $V_{DD}$.

◇ Output voltage

In the positive voltage conversion, the diode characteristics directly affect the boosting characteristics. Especially using the VF pin (forward voltage lowering) in a diode causes the boosting output voltage to be reduced. In the example shown in Fig.9.11, three diodes are used; therefore, be sure to drop the voltage by 3 × VF as shown in Fig.9.12. The boosting power voltage is indicated in the following expression.

| VO' | When increasing | VO' | , use a diode with the lower VF value.

$$|VO'| = 3\times|VI| - 3\times VF \quad \cdots\cdots\cdots \quad \text{Expression (9.4)}$$

◇ Precautions

① Input and output current conditions

To keep the input and output current ratings, take care so that the input current does not exceed the rating.

② Input voltage conditions

For positive voltage conversion, the input voltage rating is equal to for the negative double-boosting. (See Table 7.1.)

◇ Other setting conditions

① When using the high output mode

Connect the FC pin to VI.

## 9.10 Connection Example when Changing the Regulator Temperature Coefficient

The temperature coefficient of the regulator is determined depending on that of the internal reference voltage as described in Section 5.3.

When setting the other temperature coefficient, use a thermistor resistor, etc. as shown in Fig.9.15.

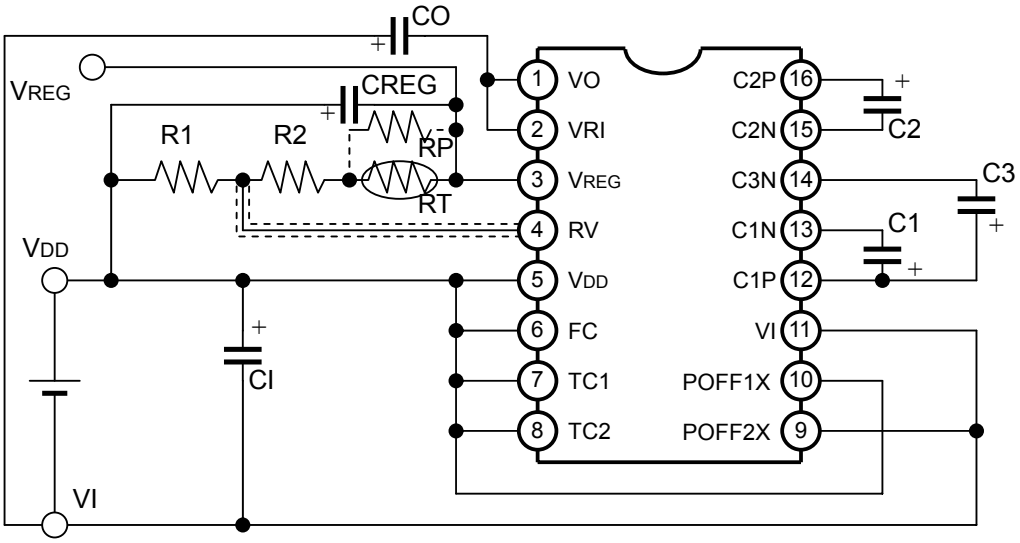



Fig.9.15 Connection Example when Changing the Regulator Temperature Coefficient

◇ Fig.9.15 Setting conditions
- Internal clock : ON (Low output mode)
- Booster : ON
- Regulator : ON
- Thermistor resistor : RT

◇ Power-off method

Set the POFF1X pin to level LOW (VI); all circuits will be turned off.

◇ Regulator temperature coefficient
- For information about the basic regulator setting method and notes, see Section 5.4.
- The temperature characteristics of the thermistor resistor RT indicate the nonlinearity. When compensating the linear characteristics, insert the RP shown in Fig.9.15.

◇ Other setting conditions

① When using the high output mode

Connect the FC pin to VI.

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