EPSON
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S1F76610M2E
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.1

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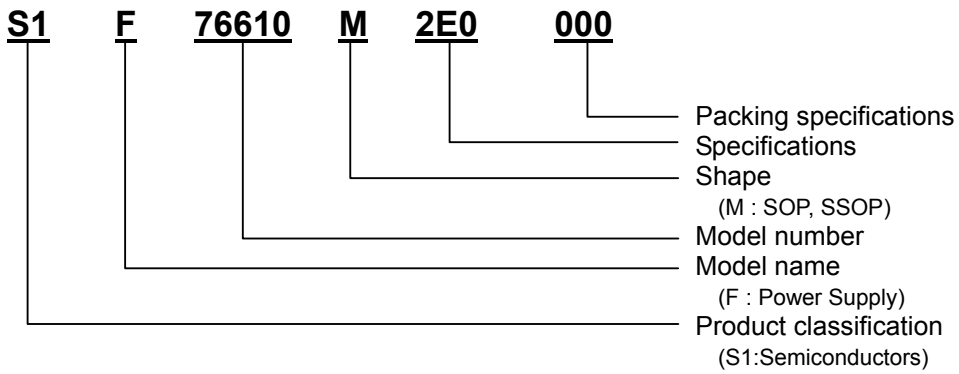
Configuration of product number

●DEVICES



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1. DESCRIPTION

The S1F76610 is a CMOS DC-DC converter with high efficiency and low power consumption.

It consists of two major components: a booster and a stabilizer. The booster assures double boosting output (-3.6 to -12V) or triple boosting output (-5.4 to -18V) for input voltage (-1.8 to -6V).

The stabilizer sets any output voltage. It also provides three types of negative temperature gradients for stabilization output, and it is appropriate for LCD power.

The S1F76610 enables you to drive an IC (liquid crystal driver, analog IC, etc.) that would usually require another power supply in addition to the logic main power, using a single power supply. Therefore, it is suitable for supplying micro-power to compact electrical devices such as hand-held computers with low power consumption.

2. FEATURES

(1) CMOS DC-DC converter with high efficiency and low power consumption
(2) Easy conversion from input voltage V_{IN} (-5V) to four types of positive/negative voltages
Output + | V_{IN} | (+5V), +2 |V_{IN} | (+10V), 2V_{IN} (-10V), and 3V_{IN} (-15V) from input V_{IN} (-5V)
(3) Output voltage stabilizer built-in
Any output voltage settable with external resistor
(4) Output current ••••••••• Max. 20 mA (V_{IN} = -5V)
(5) Power conversion efficiency ••••••••• Typ. 95%
(6) Temperature gradient selectable for LCD power
3 types: -0.05%/°C, -0.30%/°C and -0.50%/°C
(7) Power-off operation by external signal
Static current for power-off: Max. 2μA
(8) Serial connection enabled (V_{IN} = -5V, V_{OUT} = -20V using two ICs)
(9) Low voltage operation: Appropriate for battery drive
(10) CR oscillation circuit built-in
(11) SSOP2-16 pin
(12) This IC is not designed for strong radiation activity proof.

3. BLOCK DIAGRAM

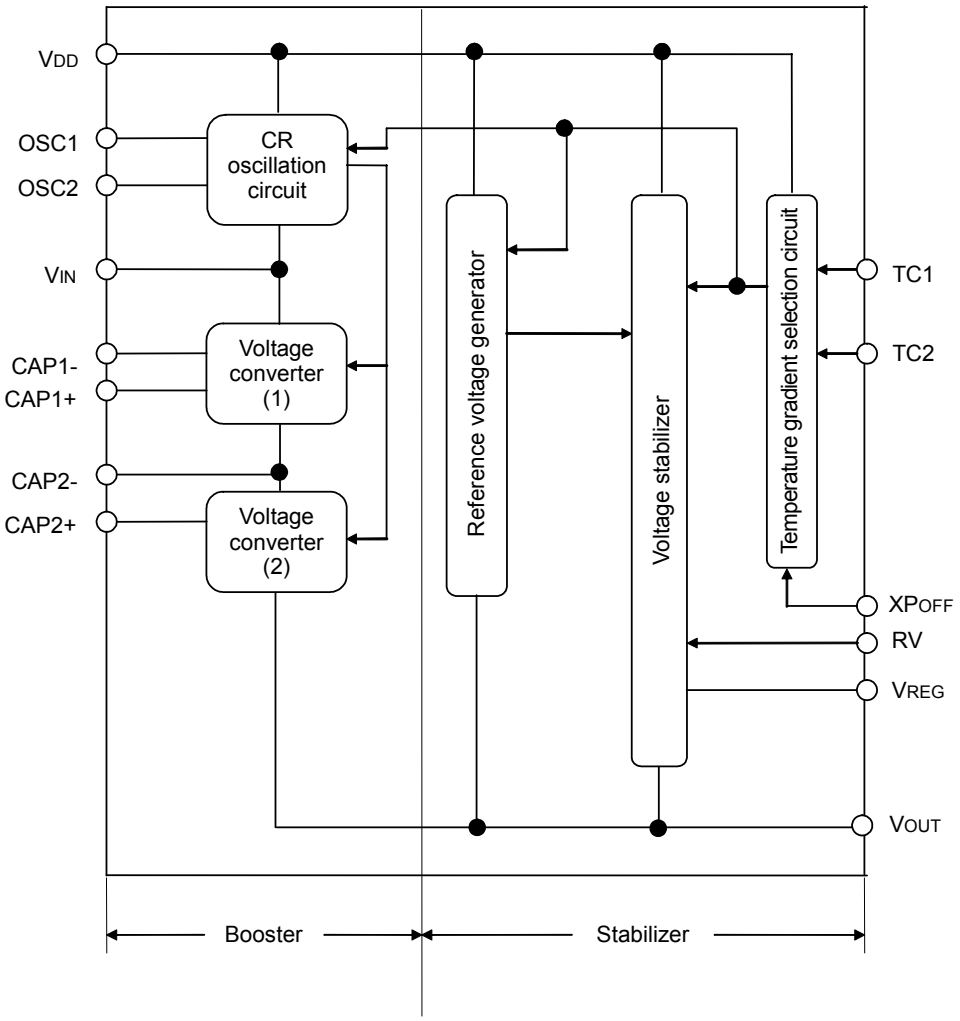


Fig.3.1 Block diagram

4. PIN DESCRIPTION

4.1 Pin assignment

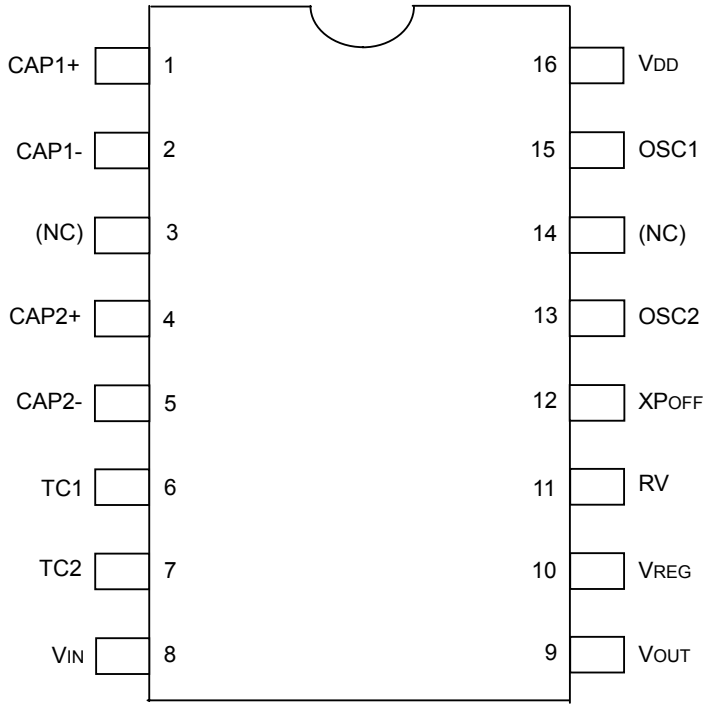


Fig.4.1 SSOP2-16 pin assignment

4.2 Pin functions

Pin No.	Pin name	Function
1	CAP1+	Positive pin connected to pump-up capacitor for double boosting
2	CAP1-	Negative pin connected to pump-up capacitor for double boosting Next-stage clock for serial connection
4	CAP2+	Positive pin connected to pump-up capacitor for triple boosting
5	CAP2-	Negative pin connected to pump-up capacitor for triple boosting Output pin for double boosting (shorted with VOUT)
6	TC1	Temperature gradient selection pin
7	TC2	
8	VIN	Power supply pin (Negative side, system GND)
9	VOUT	Output pin for triple boosting
10	VREG	Stabilizing voltage output pin
11	RV	Stabilizing voltage adjustment pin Adjusts the VREG output voltage by connecting an intermediate tap of the external volume (3-pin resistor) connected between the VDD and VREG pins to the RV pin.
12	XPOFF	VREG output ON/OFF control pin Controls S1F76610 power-off (VREG output power off) by inputting a control signal from the system to this pin.
13	OSC2	Pin connected to oscillation resistor Opened for external clock operation.
15	OSC1	Pin connected to oscillation resistor Functions as a clock input pin for external clock operation
16	VDD	Power supply pin (Positive side, system VCC)

5. FUNCTIONAL DESCRIPTION

① CR oscillation circuit

The S1F76610 is equipped with a CR oscillation circuit as an internal oscillation circuit, connecting external resistor ROSC for oscillation between the OSC1 and OSC2 pins. (Fig.5.1)

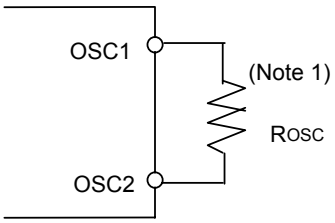


Fig.5.1 CR oscillation circuit

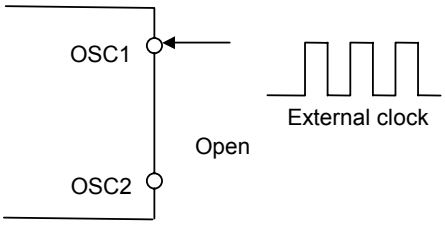


Fig.5.2 External clock operation

Note 1) The oscillation frequency varies depending on the wiring capacity, so the wire between OSC1, OSC2, and ROSC must be short as possible.

To set the external resistor ROSC, first obtain the oscillation frequency fOSC that satisfies the maximum efficiency in Fig.7.12 and 7.13, and then obtain ROSC corresponding to the fOSC in Fig.7.1. The relation between ROSC and fOSC shown in Fig.7.1 is expressed with the following formula, concerning only the straight part (500kΩ < ROSC < 2MΩ).

$$R_{OSC} = A \cdot \frac{1}{f_{OSC}}$$

A = Constant :V_{DD} = 0V, V_{IN} = -5V
→ A = 2.0×10^{10} (Ω・Hz)

Therefore, the ROSC value is obtained from the relational expression above.
(Recommended oscillation frequency: 10kHz to 30kHz (ROSC: 2MΩ to 680kΩ)

For external clock operation, as shown in Fig.5.2, open the OSC2 pin and input external clocks (duty 50%) from the OSC1 pin.

② Voltage converters (I) and (II)

Voltage converters (I) and (II) perform double boosting and triple boosting for input power voltage VIN using clocks generated in the CR oscillation circuit.

For double boosting, the double input voltage VIN is obtained from the CAP2- pin by connecting an external pump-up capacitor between CAP1+ and CAP1- and an external smoothing capacitor between VIN, CAP2, and CAP2-. For triple boosting, the triple input voltage VIN is obtained from the VOUT pin by connecting an external pump-up capacitor between CAP1+ and CAP1- and between CAP2+ and CAP2-, and connecting an external smoothing capacitor between VIN and VOUT.

Fig.4.3 and 4.4 show the relationships between input and output voltages, using VDD = 0V and VIN = -5V.

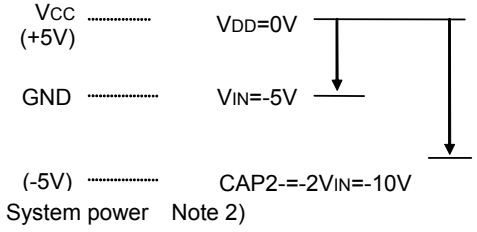


Fig.5.3 Relationships between double boosting voltages

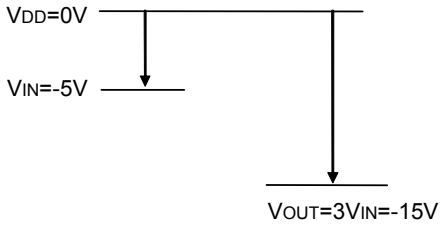


Fig.5.4 Relationships between triple boosting voltages

Note 1) In triple boosting, the double boosting output (-10V) cannot be obtained from the CAP2- pin.

Note 2) When connecting to the system power, CAP2- = -5V is obtained for double boosting output and VOUT = -10V is obtained for triple boosting by setting VIN = system power GND; VDD = system power VCC = +5V.

③ Reference voltage generator, voltage stabilizer

The reference voltage generator generates a reference voltage required to operate the voltage stabilizer, and provides a temperature gradient to the reference voltage. There are three types of temperature gradients and the appropriate one is selected by a signal sent from the temperature gradient selection circuit. The voltage stabilizer stabilizes boosting output voltage VOUT and outputs any voltage. As shown in Fig.5.5, the VREG output voltage can be set to any voltage between the reference voltage VRV and VOUT by connecting the external resistor RRV and changing the voltage of the intermediate tap.

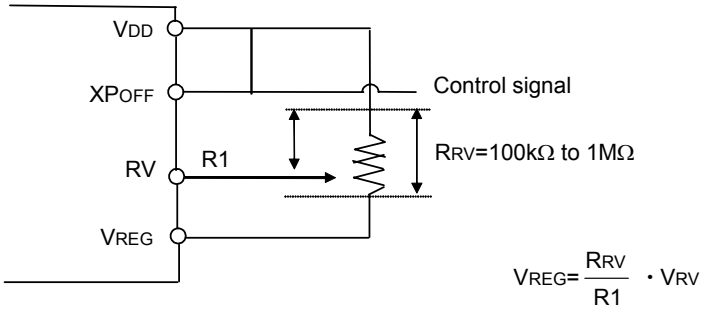


Fig.5.5 Voltage stabilizer

The voltage stabilizer, which is equipped with the power-off function, enables VREG output ON/OFF control at timings when the signal is sent from the system (microprocessor, etc.).

When XPOFF = High (VDD), the VREG output is turned ON; when XPOFF = Low (VIN), it is turned OFF.

If the VREG output ON/OFF control is not necessary, XPOFF is fixed to High (VDD).

④ Temperature gradient selection circuit

As shown in Table 5.1, the S1F76610 provides three appropriate temperature gradients for LCD driving to VREG output.

Table 5.1 Correspondence between temperature gradients and VREG output ON/OFF

XPOFF Note 1)	TC2 Note 1)	TC1 Note 1)	Temperature gradient CT Note 2)	VREG output	CR oscillation circuit	Remarks
1 (VDD)	Low (VOUT)	Low (VOUT)	-0.30%/°C	ON	ON	—
1 (VDD)	Low (VOUT)	High (VDD)	-0.05%/°C	ON	ON	—
1 (VDD)	High (VDD)	Low (VOUT)	-0.50%/°C	ON	ON	—
1 (VDD)	High (VDD)	High (VDD)	-0.50%/°C	ON	OFF	Serial connection Note 4)
0 (VIN)	Low (VOUT)	Low (VOUT)	—	OFF(Hi-Z) Note 3)	OFF	—
0 (VIN)	Low (VOUT)	High (VDD)	—	OFF(Hi-Z) Note 3)	OFF	—
0 (VIN)	High (VDD)	Low (VOUT)	—	OFF(Hi-Z) Note 3)	OFF	—
0 (VIN)	Low (VDD)	High (VDD)	—	OFF(Hi-Z)	ON	Boosting only Note 5)

Note 1) The low voltage is different between the XPOFF, TC2, and TC1 pins.

Note 2) The temperature gradient CT is defined in the following formula:

$$CT = \frac{|V_{REG}(50^{\circ}C)| - |V_{REG}(0^{\circ}C)|}{50^{\circ}C - 0^{\circ}C} \times \frac{1}{|V_{REG}(25^{\circ}C)|} \quad (\%/^{\circ}C)$$

Here, | VREG | means VDD - VREG. In Table 5.1, the negative sign assigned to each temperature gradient means that VDD - VREG = | VREG | reduces as the temperature rises.

$$\frac{\Delta |V_{REG}|(Ta)}{|V_{REG}|} = \frac{|V_{REG}(Ta)| - |V_{REG}(25^{\circ}C)|}{|V_{REG}(25^{\circ}C)|}$$

Based on this formula, Fig.7.19 shows the relationships between $\frac{\Delta|V_{REG}|}{|V_{REG}|}$ and temperature Ta.
In Fig.7.19, the inclination below indicates CT.

$$\left\{ \frac{\Delta |V_{REG}|(50^{\circ}C)}{|V_{REG}|} = \frac{\Delta |V_{REG}|(0^{\circ}C)}{|V_{REG}|} \right\} \Big/ \ (50^{\circ}C - 0^{\circ}C)$$

Example: When CT = -0.5%/°C is selected;
if VREG output at Ta = 25°C is VREG (25°C) = -8V,
Δ VREG / ΔT = CT • | VREG (25°C) | = $-0.5 \times 10^{-2} \times 8$ = -40mV/°C is obtained,
the | VREG |value reduces 40mV each time the temperature rises 1°C.
VREG (25°C) = -10V results in Δ |VREG | / ΔT = -50mV/°C.

Note 3) When the power is off (VREG output: OFF, CR oscillation circuit: OFF), the VOUT output voltage is set to VIN +0.5V.

Note 4) Selecting this mode for serial connection drives the next-stage IC with the first-stage clock, and reduces the power consumption of the next-stage IC. (See item 8 - (4).)

Note 5) This mode is recommended for boosting. It minimizes the current consumption.

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute maximum ratings

Item	Symbol	Standard value		Unit	Remarks
		Min.	Max.		
Input power voltage	V_{IN}	-20/N	V_{DD}+0.3	V	V_{IN} N = 2: Double boosting N = 3: triple boosting
Input pin voltage	V_I	V_{IN}-0.3	V_{DD}+0.3	V	OSC1, XP_{OFF}
		V_{OUT}-0.3	V_{DD}+0.3	V	TC1, TC2, RV
Output voltage	V_{OUT}	-20	V_{DD}+0.3	V	V_{OUT} Note 3)
		V_{OUT}	V_{DD}+0.3	V	V_{REG} Note 3)
Output pin voltage 1	VOC1	V_{IN}-0.3	V_{DD}+0.3	V	CAP1+, CAP2+, OSC2
Output pin voltage 2	VOC2	2×V_{IN}-0.3	V_{DD}+0.3	V	CAP1-
Output pin voltage 3	VOC3	3×V_{IN}-0.3	V_{DD}+0.3	V	CAP2-
Allowable dissipation	Pd	—	210	mW	SSOP2-16PIN
Operating temperature	T_{opr}	-40	85	°C	
Storage temperature	T_{stg}	-55	150	°C	
Soldering temperature and time	T_{sol}	—	260•10	°C•S	Lead part

Note 1) Exceeding the absolute maximum ratings above may cause a permanent destruction of the IC. A long-term operation with the absolute maximum ratings may cause a significant reduction of reliability.

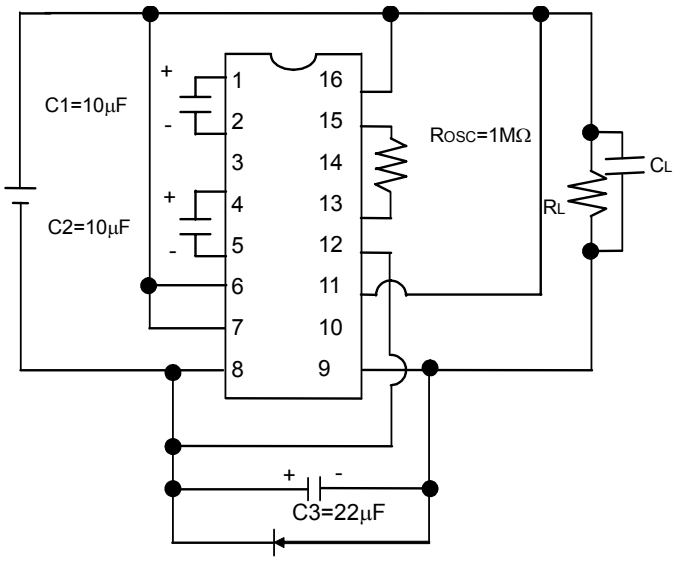
Note 2) All the voltage values above are based on V_{DD}.

Note 3) The V_{OUT} and V_{REG} output pins output the boosted voltage and stabilized boosted-voltage. No external voltage should therefore be applied to these pins. When being compelled to apply external voltage to the pins for use, it must be in the allowable range of the rated voltages above.

6.2 Recommended operating conditions

Item	Symbol	Standard value		Unit	Remarks
		Min.	Max.		
Boosting start voltage	VSAT1	—	-1.8	V	R_{OSC} = 1MΩ, C3 ≥ 10μF C_L / C3 ≤ 20 T_a = -40 to 85°C, Note 1)
	VSAT2	—	-2.2		R_{OSC} = 1MΩ
Boosting stop voltage	VSTP	-1.8	—	V	R_{OSC} = 1MΩ
Output load resistance	R_L	R_{Lim} Note 2)	—	V	—
Output load current	I_{OUT}	—	20	Ω	—
Oscillation frequency	f_{OSC}	10	30	mA	—
External resistor for oscillation	R_{OSC}	680	2000	kHz	—
Boosting capacitor	C1, C2, C3	3.3	—	μF	—
Stabilization-output adjusting resistor	R_{RV}	100	1000	kΩ	—

All the voltages are based on V_{DD} = 0V.
Note 1) For low-voltage (V_{IN} = -1.8 to -2.2V) operation, the recommended circuit is as follows:
Note 2) R_{Lmin} varies depending on the input voltage.



D1 (VF (IF = 1mA)≦0.6V recommended)

Fig.6.2.1 Recommended circuit for low-voltage operation

6.3 Electrical characteristics

T_a = -40°C to +85°C V_{DD} = 0V, V_{IN} = -5V unless especially specified.

Item	Symbol	Standard value			Unit	Conditions	Measuring circuit
		Min.	Typ.	Max.			
Input power voltage	V_{IN}	-6.0	—	-1.8	V		—
Output voltage	V_{OUT}	-18.0	—	—	V		—
Stabilizer output voltage	V_{REG}	-18.0	—	V_{RV}	V	R_L = ∞, R_{RV} = 1MΩ, V_{OUT} = -18V	②
Stabilizer operating voltage	V_{OUT}	-18.0	—	-7.0	V		—
Booster current consumption	Iopr1	—	30	60	μA	R_L = ∞, R_{OSC} = 1MΩ	①
Stabilized circuit current consumption	Iopr2	—	10	20	μA	R_L = ∞, R_{RV} = 1MΩ, V_{OUT} = -15V	②
Static current	I_Q	—	—	2	μA	R_L = ∞, OSC1 = V_{DD}, V_{OUT} = -10V	④
Oscillation frequency	f_{OSC}	16	20	24	kHz	R_{OSC} = 1MΩ	①
Output impedance	Rout	—	120	150	Ω	I_{OUT} = 10mA	①
Boosting power conversion efficiency Note 2)	Peff	90	95	—	%	I_{OUT} = 5mA	①
Stabilization output Voltage variation	$\frac{\triangle V_{REG}}{\triangle V_{OUT} \cdot V_{REG}}$	—	0.1	—	%/V	-18V < V_{OUT} < -8V, V_{REG} = -8V R_L = ∞, T_a = 25°C	②
Stabilization output Note 3) Load change	$\frac{\triangle V_{REG}}{\triangle I_{OUT}}$	—	5.0	—	Ω	V_{OUT} = -15V, V_{REG} = -8V T_a = 25°C, 0 < I_{OUT} < 10mA, TC2 = V_{DD}, TC1=V_{OUT}	②
Stabilization output Note 4) Saturated resistance	R_{SAT}	—	5.0	—	Ω	R_{SAT} = Δ (V_{REG} - V_{OUT}) / Δ I_{OUT} 0 < I_{OUT} < 10mA, RV = V_{DD}, T_a = 25°C	②
Reference voltage	VRV0	-4.0	-3.0	-2.0	V	TC2 = V_{OUT}, TC1 = V_{DD}, T_a = 25°C	②
	VRV1	-2.5	-2.0	-1.5	V	TC2 = TC1 = V_{OUT}, T_a = 25°C	
	VRV2	-1.3	-1.1	-1.0	V	TC2 = V_{DD}, TC1 = V_{OUT}, T_a = 25°C	
Temperature gradient	CT0	-0.15	-0.05	+0.10	%/°C	CT1,CT2,CT3= ((|V_{REG}(50°C)|-|V_{REG} (0°C |) / (50°C - 0°C)) × (1/|V_{REG} (25°C)|) × 100	②
	CT1	-0.40	-0.30	-0.15	%/°C		
	CT2	-0.60	-0.50	-0.40	%/°C		
Input leak current	I_{LKI}	—	—	2	μA	XP_{OFF}, TC1, TC2, OSC1, RV pin	③
Input voltage	V_{IH}	0.3V_{IN}	—	—	V	V_{IN} = -1.8 to -6.0V, XP_{OFF} pin	—
	V_{IL}	—	—	0.7V_{IN}	V	V_{IN} = -1.8 to -6.0V, XP_{OFF} pin	—

Note 1) All the voltages are based on V_{DD} = 0V.

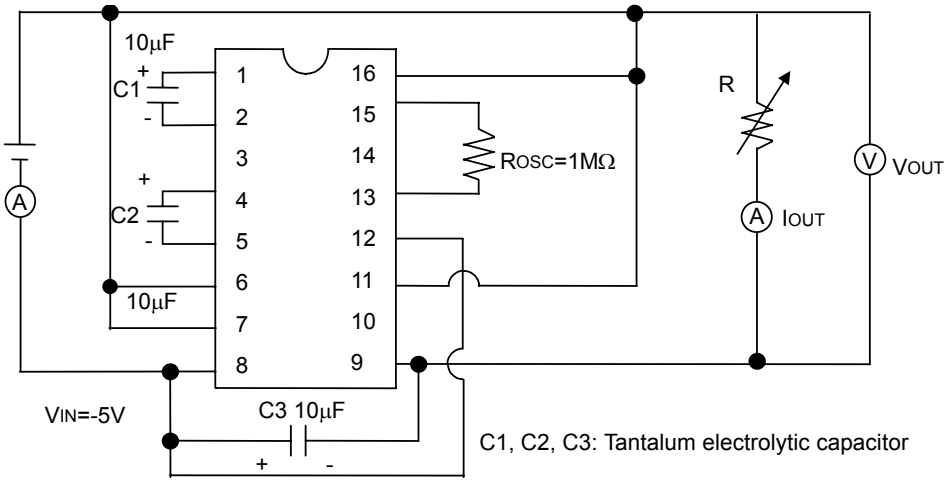
Note 2) The values above indicate the conversion efficiency of the booster. When the stabilizer is active, the loss is (V_{REG} - V_{OUT}) × I_{OUT}.
We therefore recommend a method of reducing (V_{REG} - V_{OUT}) as much as possible.
If (V_{REG} - V_{OUT}) × I_{OUT} is high, the stabilizer characteristics vary as the IC temperature rises.

Note 3) See Fig.7.15, 7.16, and 7.17.

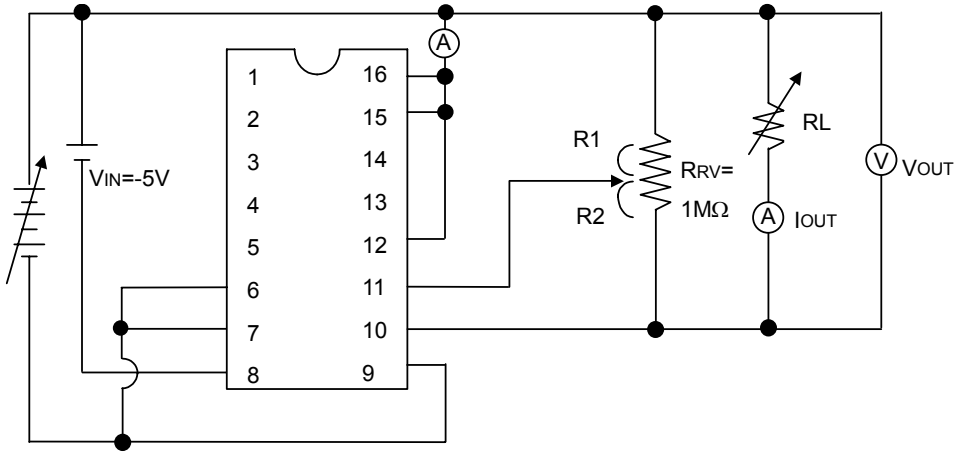
Note 4) R_{SAT} indicates the inclination shown in Fig.7.18; V_{OUT} + Δ (V_{REG} - V_{OUT}) indicates the lower limit voltage of the V_{REG} output.

6.4 Measuring circuits

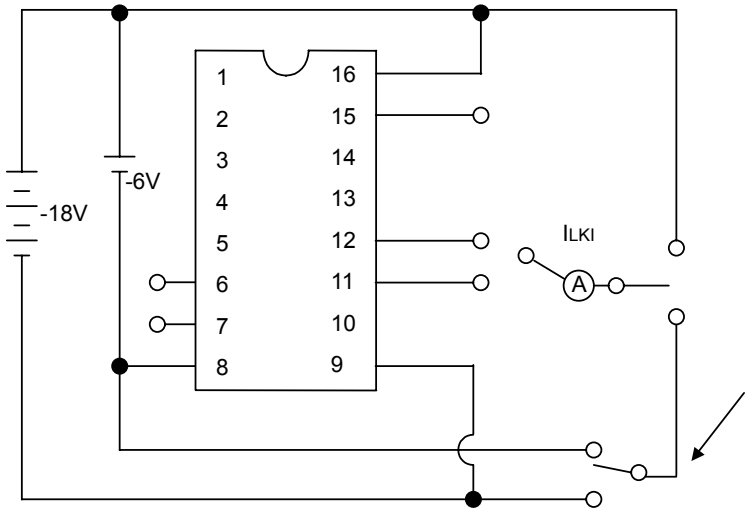
① Booster characteristic measuring circuit



② Stabilizer characteristic measuring circuit

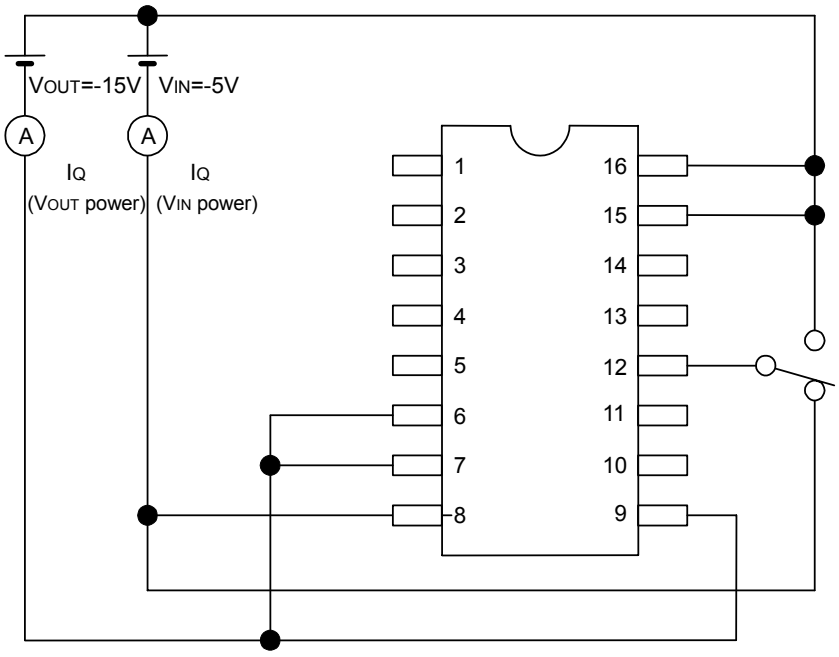


③ Input leak current characteristic measuring circuit



- Connect to -18V for measurement of pins 6, 7, and 11.
- Connect to -6V for measurement of pins 12 and 15.

④ Static-current characteristic measuring circuit



7. CHARACTERISTIC DATA SHEETS

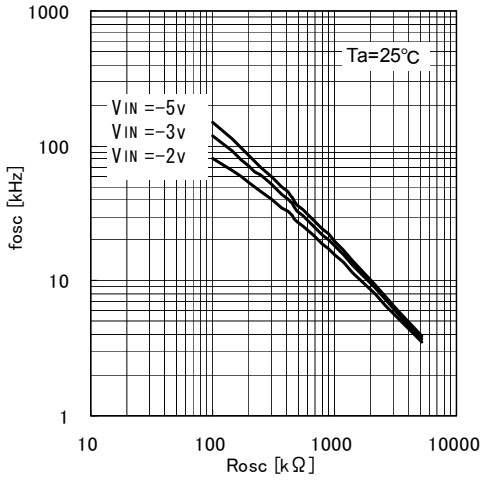


Fig.7.1 Oscillation frequency - External resistor for oscillation

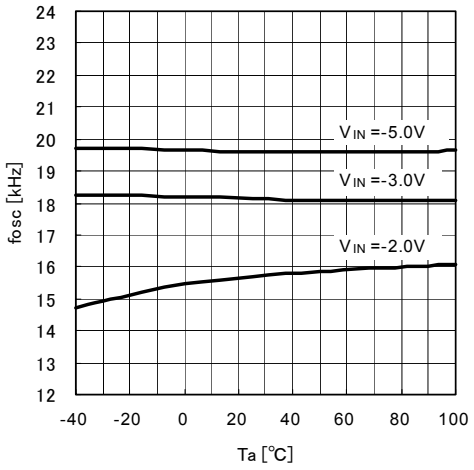


Fig.7.2 Oscillation frequency - Temperature

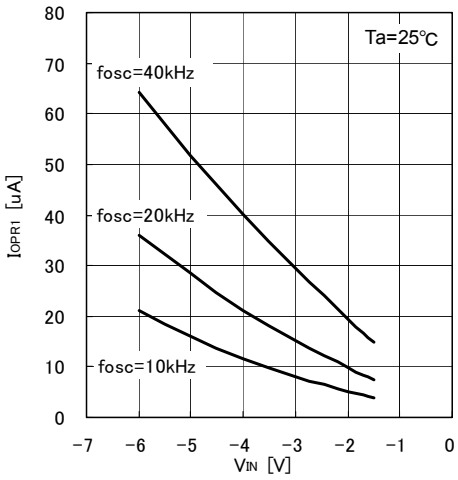


Fig.7.3 Booster current consumption - Input voltage

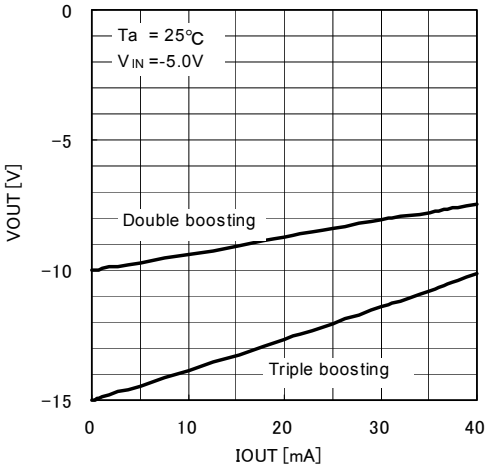


Fig.7.4 Output voltage - Output current

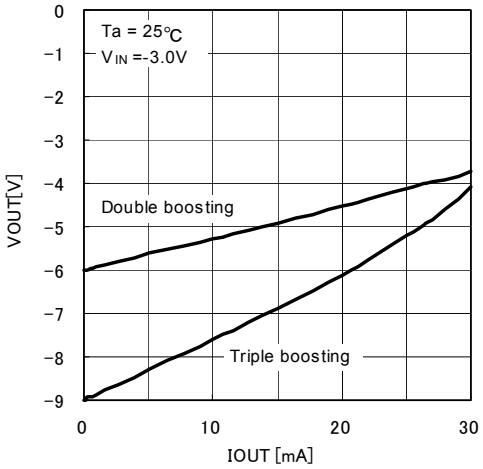


Fig.7.5 Output voltage - Output current

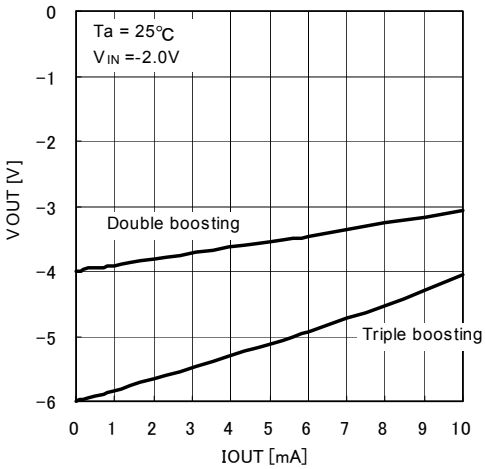


Fig.7.6 Output voltage - Output current

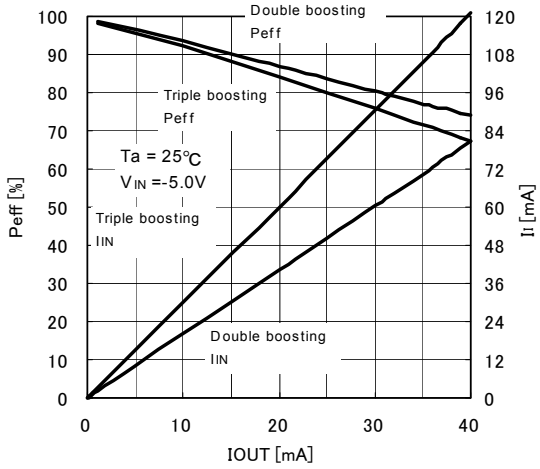


Fig.7.7 Power conversion efficiency -
Output current
Input current - Output current

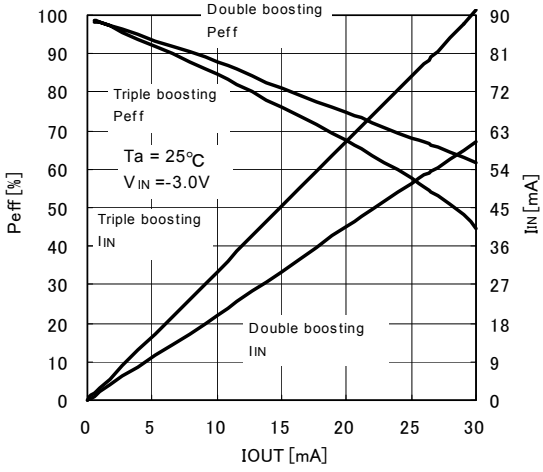


Fig.7.8 Power conversion efficiency -
Output current
Input current - Output current

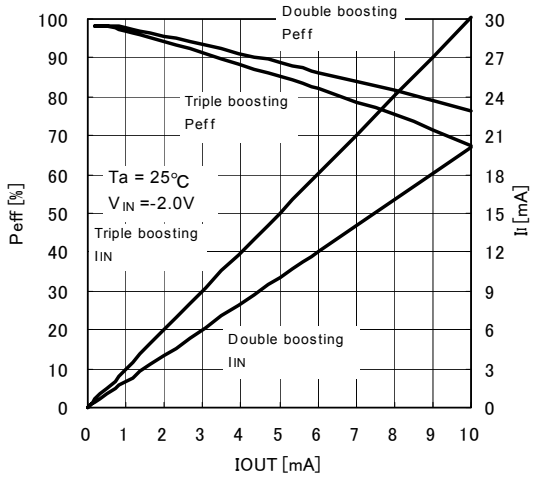


Fig.7.9 Power conversion efficiency - Output current
Input current - Output current

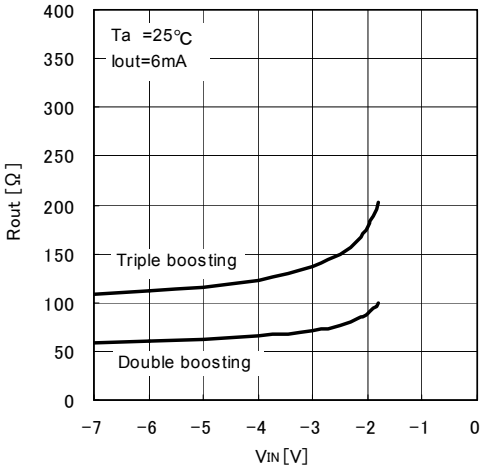


Fig.7.10 Output impedance - Input voltage

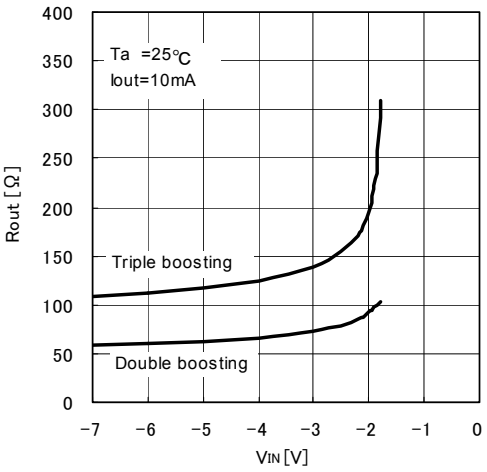


Fig.7.11 Output impedance - Input voltage

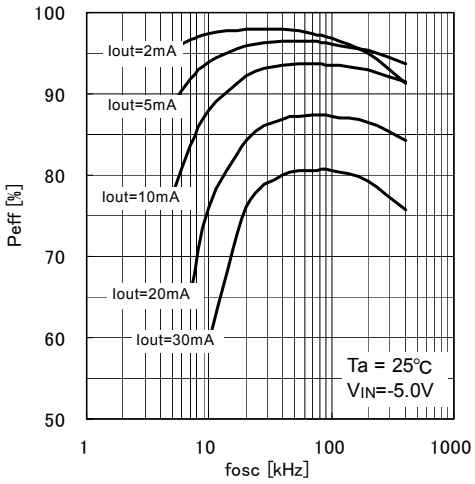


Fig.7.12 Power conversion efficiency - Oscillation frequency

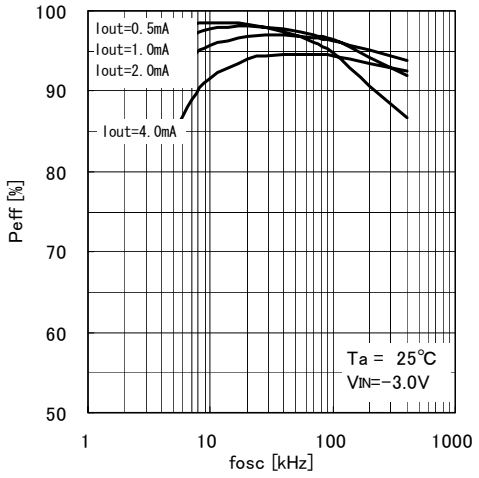


Fig.7.13 Power conversion efficiency - Oscillation frequency

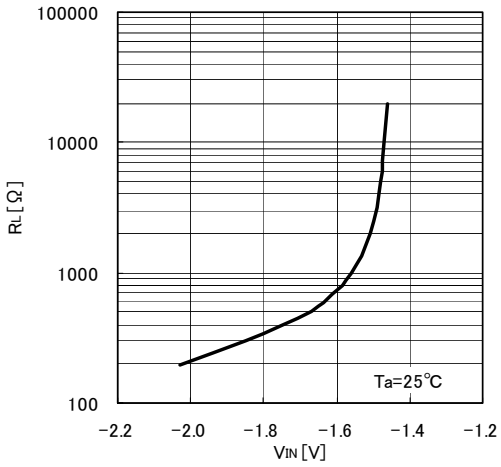


Fig.7.14 Minimum load resistance - Input voltage

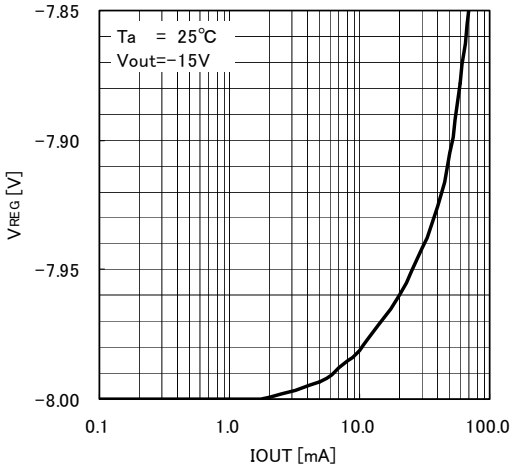


Fig.7.15 Output voltage - Output voltage

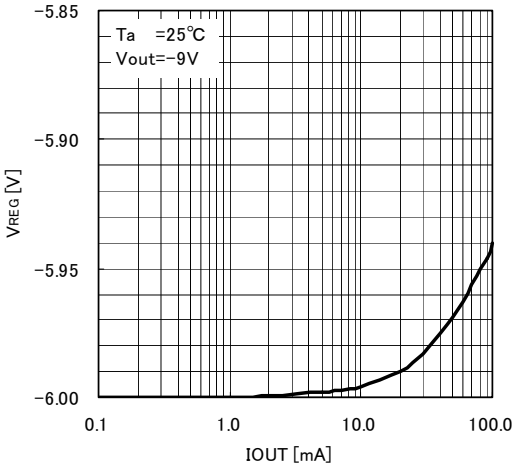


Fig.7.16 Output voltage - Output voltage

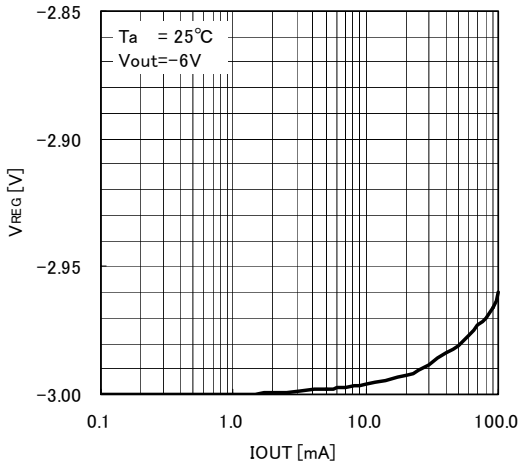


Fig.7.17 Output voltage - Output voltage

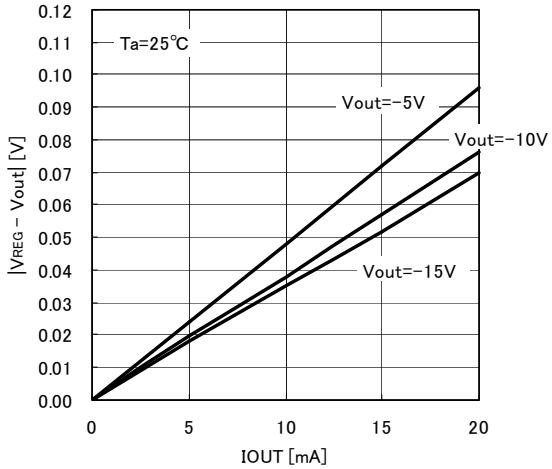


Fig.7.18 Stabilization output saturated resistance - Output current

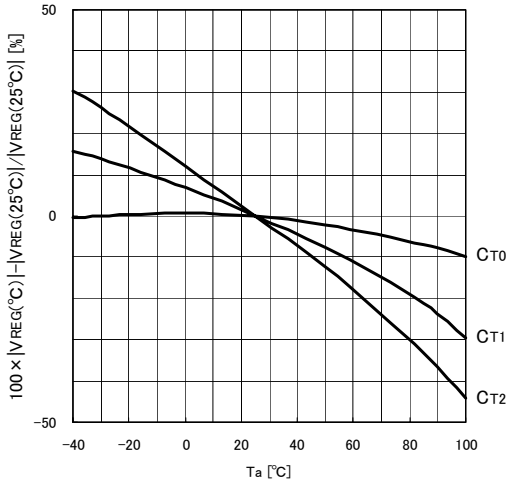


Fig.7.19 Output voltage - Temperature

8. APPLIED-CIRCUIT EXAMPLES

(1) Double boosting and Triple boosting

Fig.8.1 shows a connection example for obtaining the triple boosting output for input voltage by running only the booster. For double boosting, remove capacitor C2 and short between the CAP2- (No.5) and VO (No.9) pins; double boosting (-10V) is obtained from VO (CAP2-).

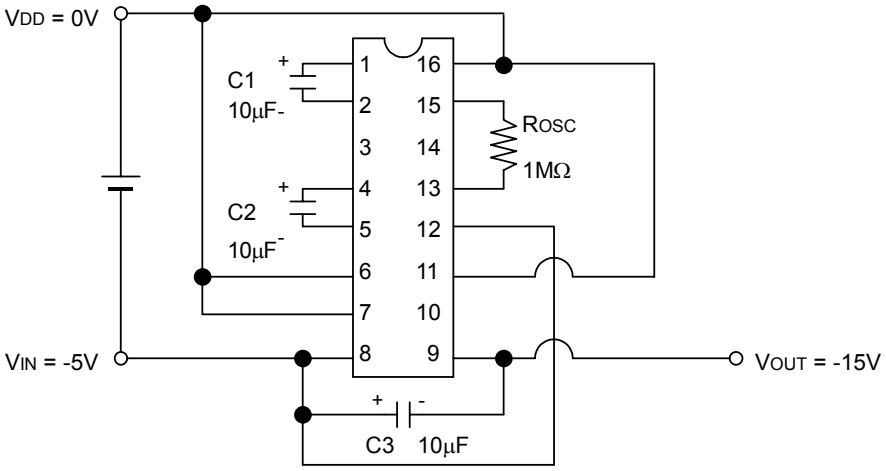


Fig.8.1 Triple boosting

(2) Triple boosting + Stabilizer

1) Fig.8.1 shows an applied-circuit example for stabilizing the boosting output obtained by double boosting and triple boosting through the stabilizer and providing the temperature gradient to the VREG output through the temperature gradient selection circuit. This applied-circuit example can indicate two outputs from VO and VREG at the same time. Using the double boosting described in item (1) "Double Boosting and triple Boosting" enables double boosting + stabilizer.

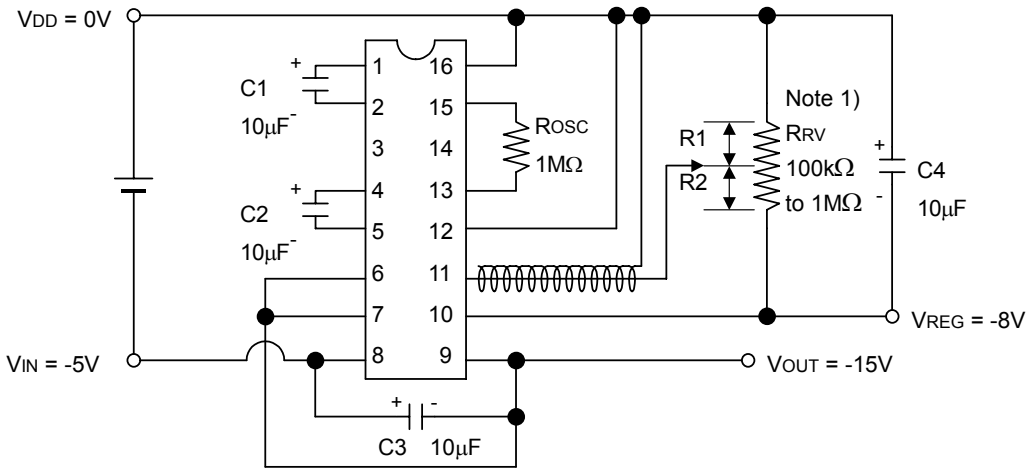


Fig.8.2 Triple boosting + Stabilizer operation (Temperature gradient = -0.3%/°C)

Note 1) The RV pin (No.11) has high input impedance. If the wire is long, use a shield wire to prevent a noise.
To reduce the influence by a noise, lower the RRV value. (However, the RRV current consumption will increase.)

Note 2) The VREG output voltage must be within | VO | - | VREG | ≤ 10V.
The set voltage is obtained from the following formula:

$$VREG = \frac{RRV}{R1} \times VRV$$

(3) Parallel connection

As shown in Fig.8.3, multi-connection reduces output impedance RO. Therefore, a configuration of n parallel connections lowers RO to 1/n. Smoothing capacitor C3, which is a single device, is shared by those connections.

To obtain stabilization output after parallel connections, apply the connection shown in Fig.8.2 to only one of the n parallel connections shown in Fig.8.3.

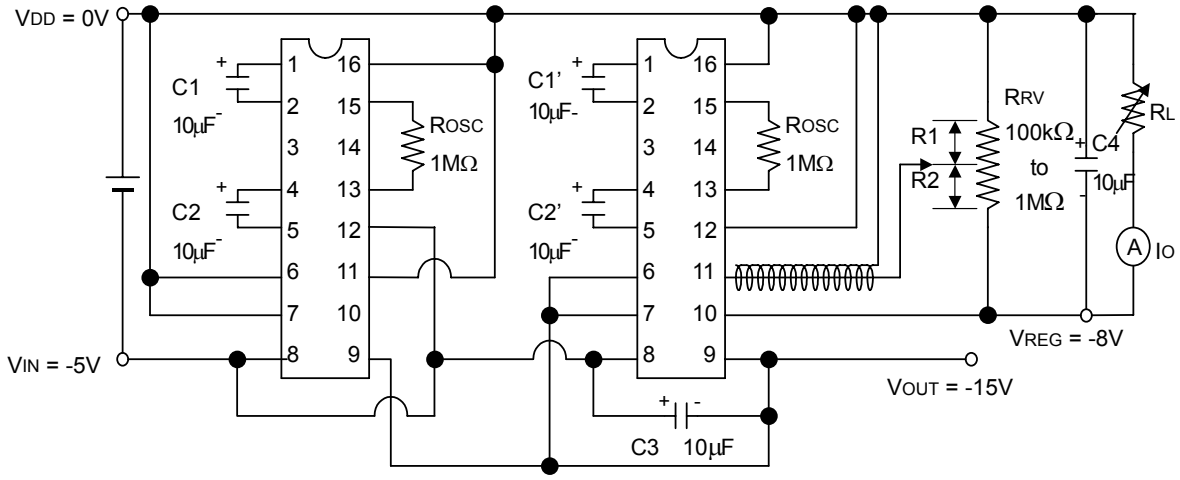


Fig.8.3 Parallel connection

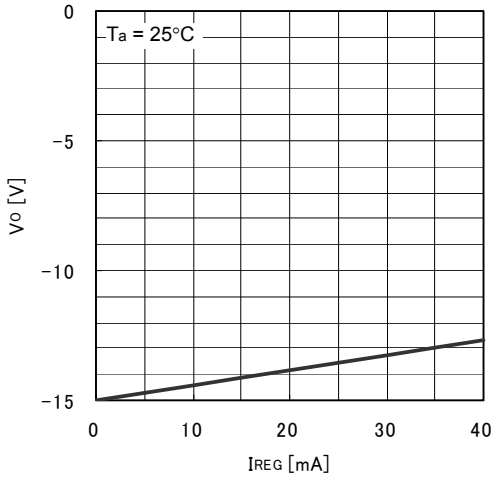


Fig.8.4 Output voltage - Output current

(4) Serial connection

The serial connection in the S1F76610 (connecting VIN and VOUT in the pre-stage to VDD and VIN in the next stage respectively) further increases output voltage. However, the serial connection raises output impedance. Fig.8.5 shows a serial connection example for obtaining VOUT = -20V from VIN = -5V to stabilize output voltage.

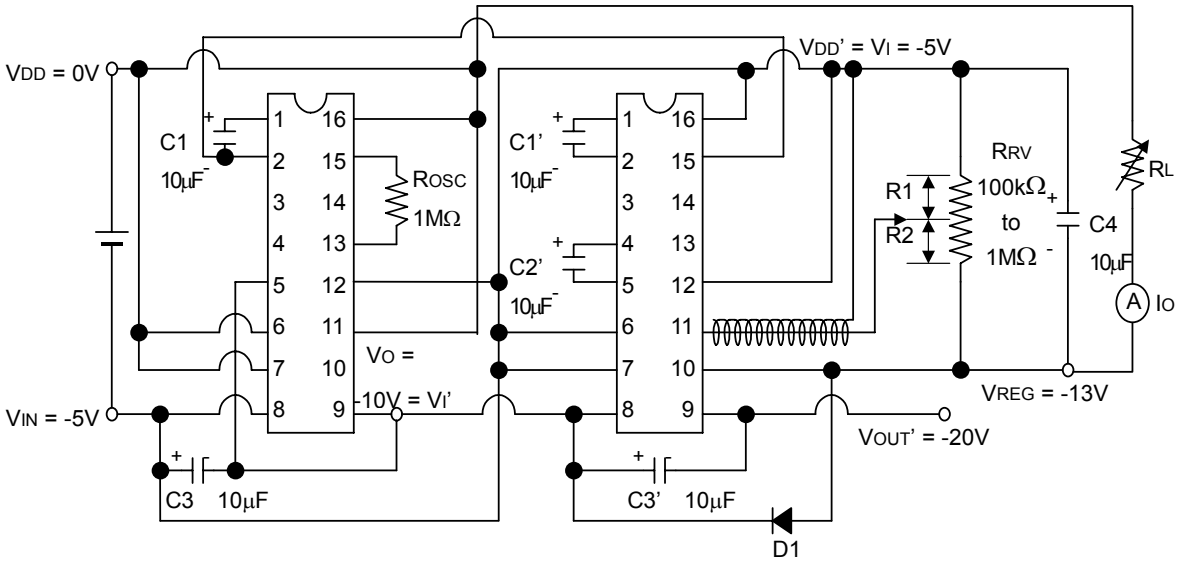


Fig.8.5 Serial connection

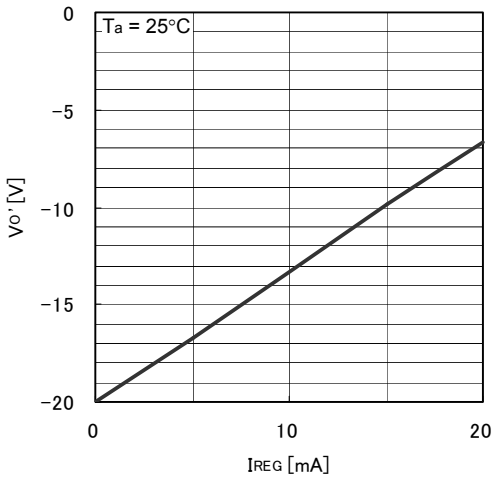


Fig.8.6 Output voltage - Output current

Note 1) <Notes on load connection>
As shown in Fig.8.5, when connecting load between VDD (or other voltage above VDD') and VREG in serial connection, take care of the following points:
When the IC is activated or no normal output is generated at the VREG pin like VREG by the XPOFF signal, current is supplied from VDD (or other voltage above VDD') to the VREG pin through the load. If the voltage exceeds the absolute maximum rating above VDD' at the VREG pin, the IC may fail normal operation. For serial connection, as shown in Fig.8.5, connect diode D1 between VI' and VREG so that the voltage above VDD' is not applied to the VREG pin.

Note 2) In Fig.8.5, the first stage is assigned to double boosting and the next-stage to triple boosting; however, triple boosting is available for both the first and next stages unless the input voltage VDD' - VI' in the next stage exceeds the standard value (6V). For serial connection, each IC must be designed in conformity with the standard (VDD - VI ≤ 6V, VDD - VO ≤ 18V). (See Fig.8.7.)

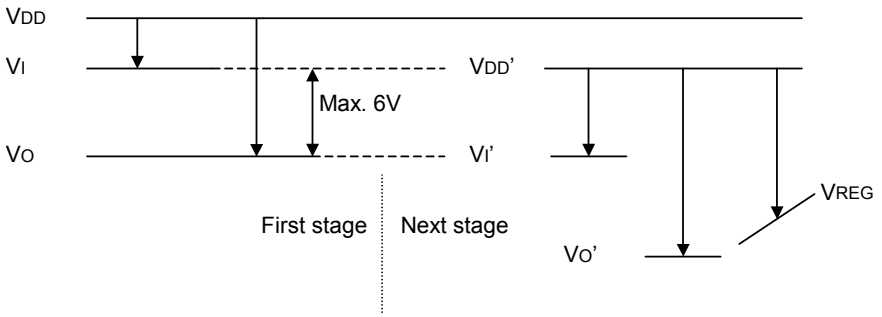


Fig.8.7 Power system in serial connection

Note 3) When double boosting is provided in the first stage, the first-stage CAP1- output can be used as a next-stage clock; however, when triple boosting is provided, it cannot be used as a next-stage clock. Therefore, to obtain a next-stage clock, mount ROSC in the external side and use an internal oscillator. As shown in Table 5.1, the next-stage external clock operation by the pre-stage CAP1- output is available only for temperature gradient CT = -0.5%/°C. If another temperature gradient is required, use an internal oscillator like the above.

Note 4) In serial connection, the temperature gradient is provided to the VDD - VREG voltage (VDD' - VREG in Fig.8.7) of the IC in which the stabilizer is active. The VREG value changes depending on the temperature as follows:

$$V_{REG} = \frac{\Delta |V_{REG}|}{\Delta T} = C_T(V_{DD'} - V_{REG})(25℃))$$

(5) Positive-voltage exchange

The S1F76610 converts input voltage to positive voltage for double boosting or triple boosting through the circuit shown in Fig.8.8. (For double boosting, remove capacitor C2 and short both ends of D3.)

However, output voltage VO lowers by forward voltage VF of the diode. For example, as shown in Fig.8.8, VDD = 0V; VI = -5V; and VF = 0.6V results in VO = 10V -3 × 0.6V = 8.2V (5V -2 × 0.6V = 3.8V for double boosting).

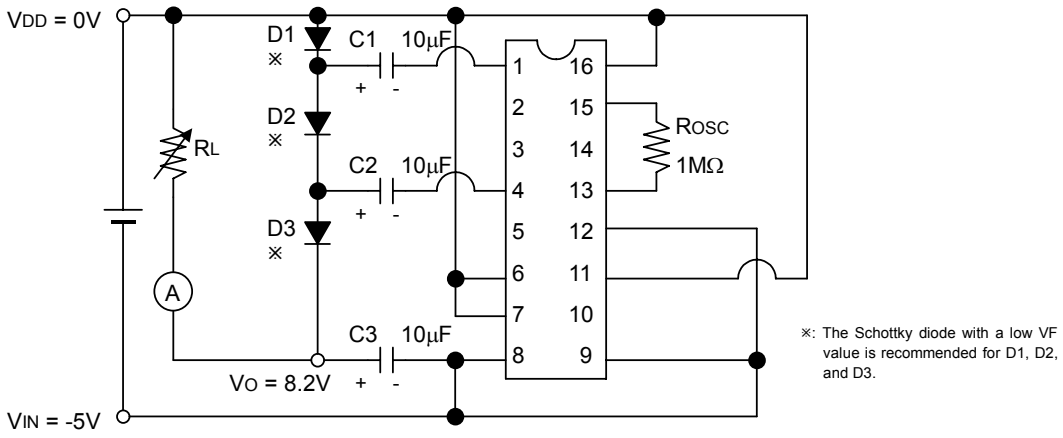


Fig.8.8 Positive-voltage conversion

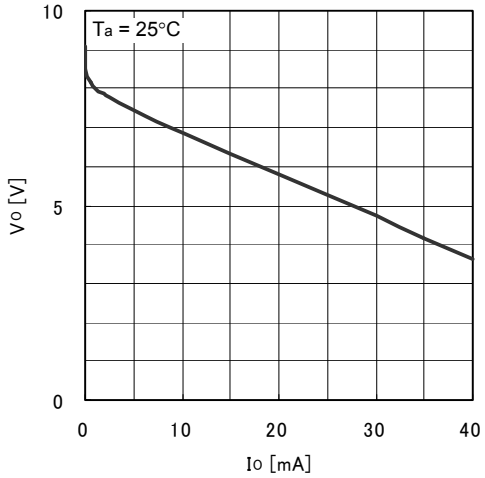


Fig.8.9 Output voltage - Output current

(6) Negative-voltage conversion + Positive-voltage conversion

Combining the triple boosting (Fig.8.1) with the positive voltage conversion (Fig.8.8) generates the circuit shown in Fig.8.9, and outputs -15V and +8.2V from -5V input.

In this case, the output impedance is higher than that for negative voltage conversion only or positive voltage conversion only.

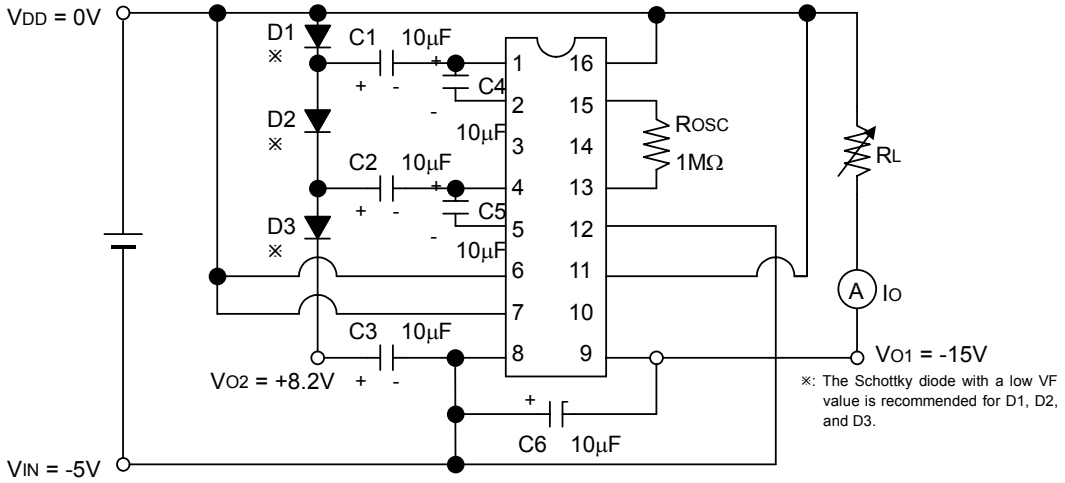


Fig.8.9 Negative-voltage conversion + Positive-voltage conversion

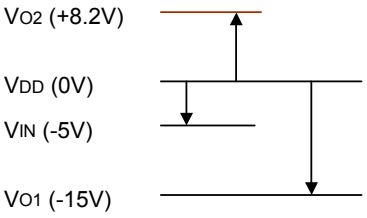


Fig.8.10 Voltage relations at VDD = 0V and VIN = -5V

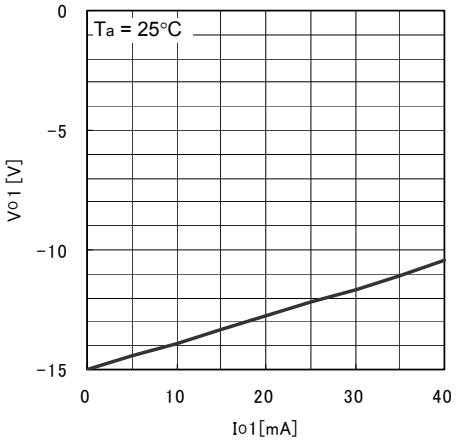


Fig.8.11 Output voltage - Output current

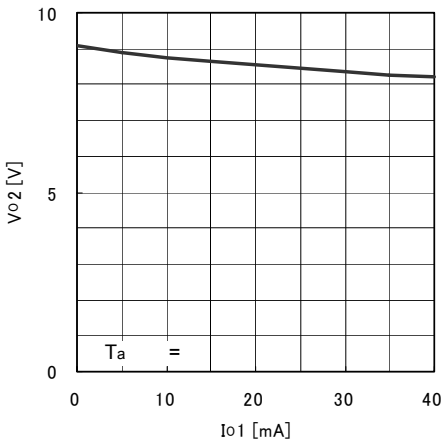


Fig.8.12 Output voltage - Output current

(7) Example of changing the temperature gradient with an external temperature sensor (thermistor)

The S1F76610, which is equipped with the temperature gradient selection circuit in the stabilizer, enables you to select three types of temperature gradients (-0.05%/°C, -0.3%/°C, and -0.5%/°C as VREG output. If the other temperature gradient is required, as shown in Fig.8.13, connect a thermistor to resistor RRV (for output voltage adjustment) in series; you can change the temperature gradient to any value.

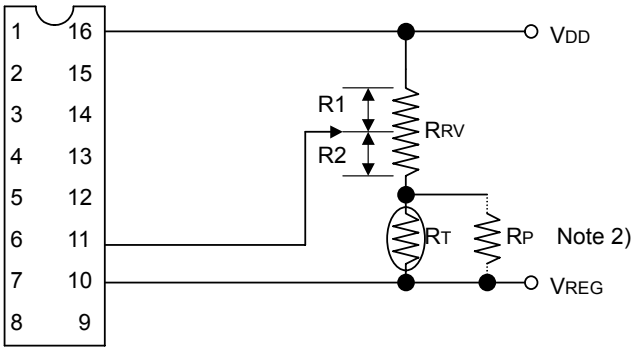


Fig.8.13 Temperature gradient change example

For a connection other than pins 10, 11, and 16, follow Fig.8.2. For pins 6 and 7, select a lower temperature gradient than the one to be changed from Table 5.1.

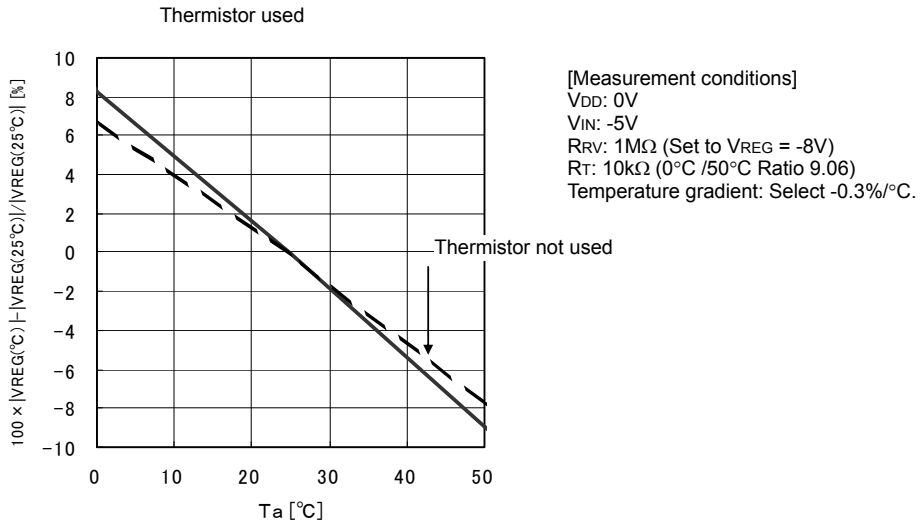


Fig.8.14 Output voltage - Temperature

Note 1) The relation between RT and VREG is indicated as follows:

$$V_{DD} - V_{REG} = \frac{R_{RV} + R_T}{R1} \times (V_{DD} - V_{RV})$$

Using a thermistor as RT increases the temperature gradient for VDD - VREG.

Note 2) The temperature characteristics of the thermistor indicate the nonlinearity; however, connecting resistor RP to the thermistor in parallel changes nonlinear characteristics to linear characteristics.

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