EPSON
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Power Supply IC

S1F76980

Technical Manual

SEIKO EPSON CORPORATION

Rev.1.0

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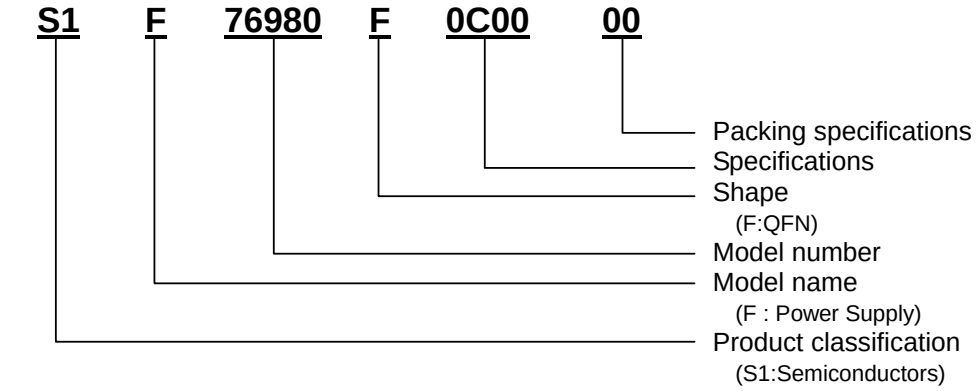
Configuration of product number

●DEVICES



CONTENTS

1. DESCRIPTION

The S1F76980 series is a low consumption current power supply input control IC, which monitors the voltage of 3-system input power supply and is capable of continuously switching power supply of the system selected in the priority sequence in the IC. For operations below the operating voltage, the product also guarantees operations in reduced power mode by setting the output level of the control signal to Hi-Z.
The use of this IC decreases voltage drop, if the Pch power MOS transistor is used as a switch for a conventional diode circuit, and contributes to the battery life extension. If the result of monitoring the output voltages shows the voltage higher than that set externally, the voltage limiter circuit operates and provides measures against overvoltage after output stage.
The package is QFN4-24.
This IC is most suitable for power input control circuit of portable device that is used by switching 3-system input power.

2. FEATURES

- Consumption current : Typ. 20µA (V_{CC}=0V, V_{BUS}=0V, V_{BAT}=2.5V, 25°C)
  Max. 40µA (V_{CC}=0V, V_{BUS}=0V, V_{BAT}=2.5V, -30°C to +85°C)
  Typ. 0.1µA (V_{CC}=0V, V_{BUS}=0V, V_{BAT}=2.5V, POWER switch OFF, 25°C)
- Operating voltage : 0 to 6.5V (Absolute maximum rating - 0.3 to 9.0V)
  (The output level of control signal is forced to be Hi-Z under the output guarantee voltage.)
- Temperature characteristics : Typ. ±100ppm/°C
- Built-in power monitoring circuit (V_{CC}, V_{BUS}) :
  Detecting voltage 2.0 to 6.3V (Aluminum option: 0.1V steps)
  Hysteresis width: 0.05 to 1.00V (Aluminum option: 0.05V steps)
  Accuracy: Set voltage ±3.0%

- Built-in power monitoring circuit (V_{BAT}):
  Detecting voltage 1.6 to 4.3V (Aluminum option: 0.1V steps)
  Hysteresis width: 0.1 to 2.1V (Aluminum option: 0.1V steps)
  Accuracy: Set voltage ±3.0%

- Built-in power-on detecting circuit, voltage limiter circuit for preventing output overvoltage, and power input control logic circuit.
- Operating temperature : -30°C to +85°C
- Package : QFN4-24P(4×4×0.85mm)
- This IC is neither designed for strong radiation activity proof nor light resistance.

3. SERIES PRODUCT NAME LIST

Table 3.1 Series product name list

Product name	Power voltage monitoring [V] Typ.						Output guarantee Voltage [V]Typ.	Shipment mode	Remarks
	V_{CC}		V_{BUS}		V_{BAT}				
	-CDET	+CDET	-UDET	+UDET	-BDET	+BDET	VHIZ		
S1F76980F0A000*	5.000	5.250	3.800	4.000	2.800	3.600	2.250	QFN4-24	—
S1F76980F0B000*	2.300	2.400	3.800	4.000	1.600	2.000	1.150	QFN4-24	—
S1F76980F0C000*	2.300	2.400	3.800	4.000	1.600	1.900	1.150	QFN4-24	—

(Note 1) For detecting voltage (-*DET) and release voltage (+*DET), those other than the above table are also available.

4. BLOCK DIAGRAM

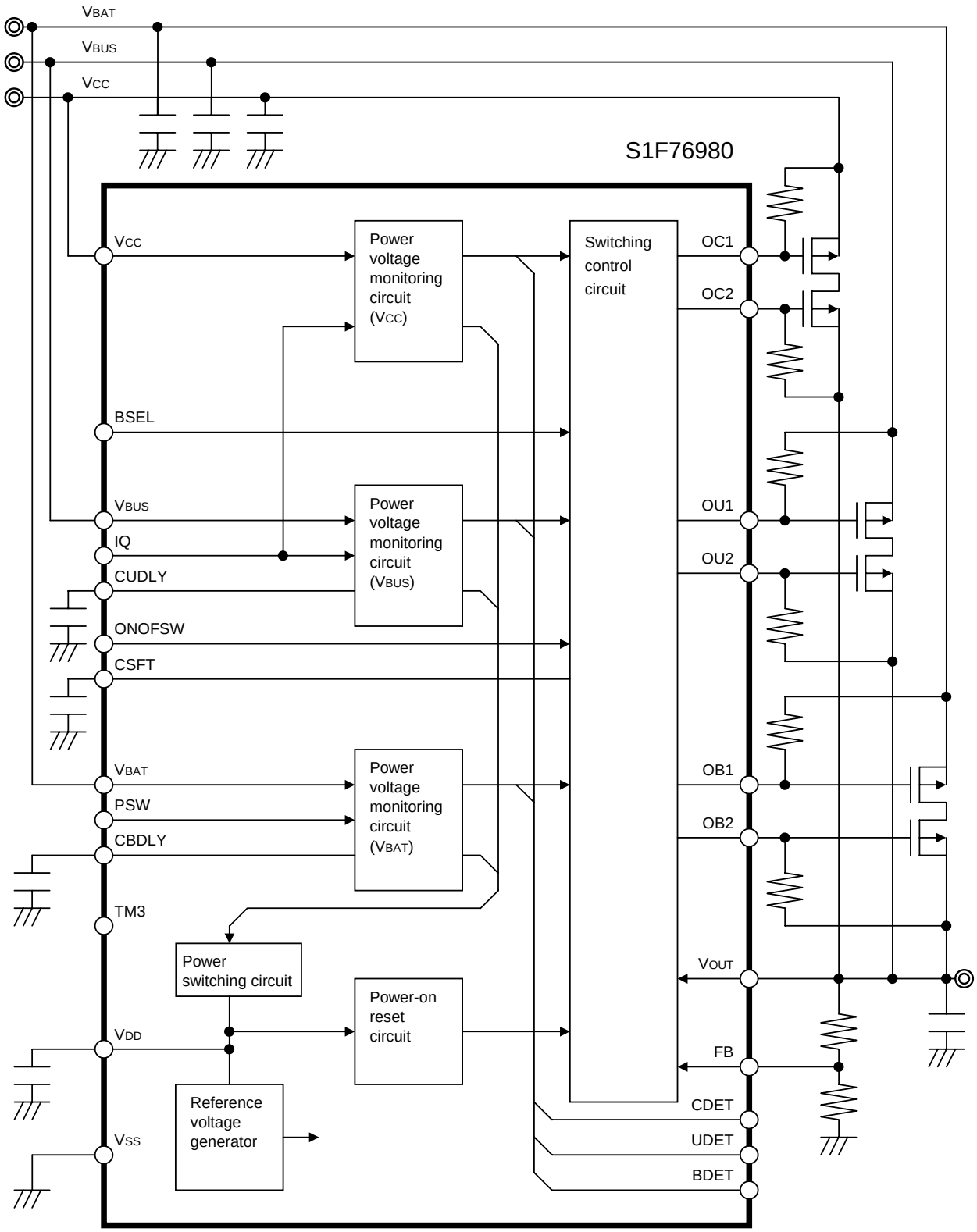


Fig.4.1 Block diagram

5. DESCRIPTION OF BLOCK DIAGRAM

(1) Power voltage monitoring circuit (V_{CC}, V_{BUS}, V_{BAT})
This circuit monitors input voltage of each power supply pin and detects low voltage. Leaving hysteresis width prevents output from becoming unstable (oscillating) when low voltage is detected.
Moreover, the IC contains a circuit to guarantee the voltage monitoring result below the operating voltage.

(2) Power switching circuit
This circuit selects a power supply (V_{DD}) used in the IC from three power supplies (V_{CC}, V_{BUS} and V_{BAT}).

(3) Reference voltage generator
This circuit generates reference voltage and reference current necessary in this IC.

(4) Power-on reset circuit
This circuit generates IC initialization signal until the internal power supply of the IC (V_{DD}) is recharged.

(5) Switching control circuit
This circuit controls output of a signal that selects optimum input power supply according to input conditions of three power supplies (V_{CC}, V_{BUS}, and V_{BAT}) and in the priority sequence set in the IC. The priority sequence of V_{BUS} and V_{BAT} can also be switched during operation, using the external pin BSEL.

6. PIN ASSIGNMENT

QFN4-24pin S1F76980F0*****

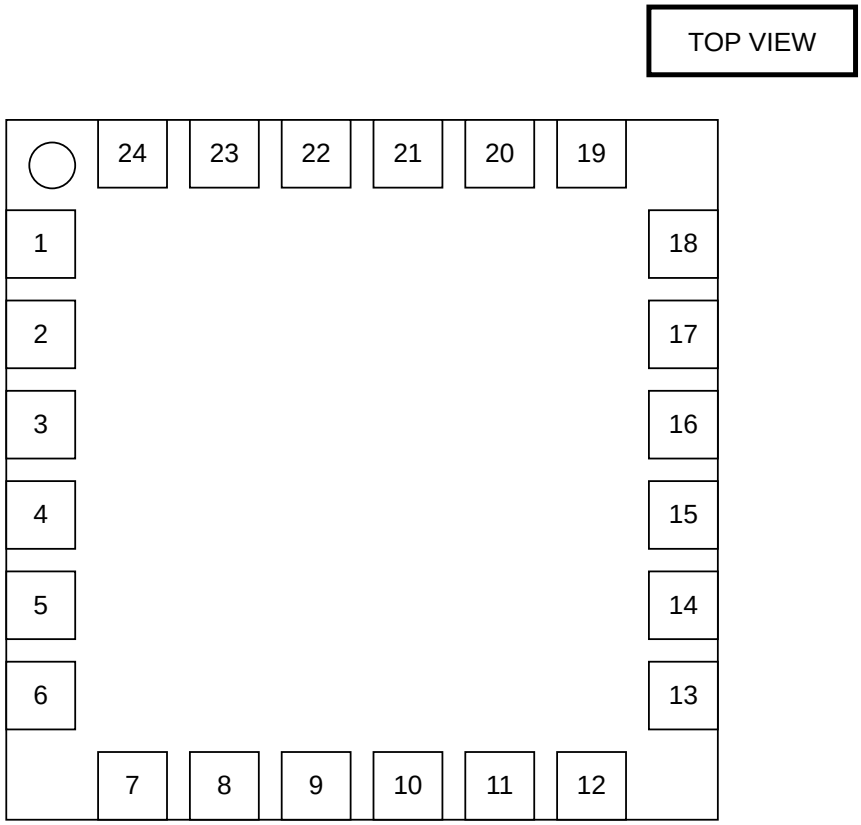


Fig.6.1 Pin assignment

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	13	FB
2	ONOFSW	14	V_{BAT}
3	V_{DD}	15	PSW
4	BSEL	16	CBDLY
5	V_{OUT}	17	IQ
6	OC1	18	BDET
7	OC2	19	TM3
8	V_{SS}	20	CUDLY
9	OU1	21	UDET
10	OU2	22	V_{BUS}
11	OB2	23	CSFT
12	OB1	24	CDET

7. PIN DESCRIPTION

7.1 Pin Functions

- Functional pins

Pin Name	I/O	Pin No.	Function
ONOFSW	I	2	Power switching operation select pin. H: ON-ON switching, L: OFF-OFF switching
PSW	I	15	V_{BAT} power supply switch pin H: OFF, L: ON (normally fixed at LOW)
BSEL	I	4	Used to set the priority sequence of V_{BUS} and V_{BAT}. H:V_{BUS}, L:V_{BAT}
FB	I	13	Feedback input pin. If measures against overvoltage are taken after output stage, feed back voltage at an appropriate voltage dividing ratio. If it is not necessary to take measures against overvoltage, pull down.
CBDLY	O	16	Pin used to connect the V_{BAT}-system low voltage detection dead time setting capacitor
CUDLY	O	20	Pin used to connect the V_{BUS}-system low voltage release delay time setting capacitor
CSFT	O	23	Pin used to connect the soft start time setting capacitor
CDET	O	24	Output pin used to monitor the V_{CC} (adapter) power supply input voltage. On Nch open drain output L: Input enabled, Hi-Z: Input disabled
UDET	O	21	Output pin used to monitor the V_{BUS} (USB) power supply input voltage. On Nch open drain output L: Input enabled, Hi-Z: Input disabled
BDET	O	18	Output pin used to monitor the V_{BAT} (battery) power supply input voltage. On Nch open drain output L: Input enabled, Hi-Z: Input disabled
OC1	O	6	V_{CC} (adapter) power supply input-side control pin. L: Switch ON, H: Switch OFF To take measures against overvoltage, operate an external MOS transistor as a regulator.
OC2	O	7	V_{CC} (adapter) power supply output-side control pin. L: Switch ON, H: Switch OFF
OU1	O	9	V_{BUS} (USB) power supply input-side control pin. L: Switch ON, H: Switch OFF To take measures against overvoltage, operate an external MOS transistor as a regulator.
OU2	O	10	V_{BUS} (USB) power supply output-side control pin. L: Switch ON, H: Switch OFF
OB1	O	12	V_{BAT} (battery) power supply input-side control pin. L: Switch ON, H: Switch OFF To take measures against overvoltage, operate an external MOS transistor as a regulator.
OB2	O	11	V_{BAT} (battery) power supply output-side control pin. L: Switch ON, H: Switch OFF

- Power Supply Pin

Pin Name	I/O	Pin No.	Function
V_{CC}	I	1	V_{CC} (adapter) power supply input-side pin.
V_{BUS}	I	22	V_{BUS} (USB) power supply input-side pin.
V_{BAT}	I	14	V_{BAT} (battery) power supply input-side pin.
V_{OUT}	I	5	3-system select power supply output-side pin.
V_{SS}	I	8	GND pin.
V_{DD}	O	3	Pin used to connect the smoothing capacitor in the IC.

- Test pin

Pin Name	I/O	Pin No.	Function
TM3	I	19	Normally fixed to LOW.
IQ	I	17	Normally fixed to LOW.

8. FUNCTIONAL DESCRIPTION

8.1 Operation Description

The S1F76980 series is a low consumption current power supply input control IC, which monitors the voltage of 3-system input power supply and is capable of continuously switching power supply of the system selected in the priority sequence in the IC. The voltage limiter function of output voltage is included in the switching control circuit to control the output voltage VOUT not to exceed the set voltage, using the voltage dividing ratio of an external resistor. For operations below the operating voltage, the function also guarantees operations in reduced power mode by setting the output level of the control signal to Hi-Z.

8.2 Power Voltage Monitoring Circuit (VCC, VBUS, VBAT)

This circuit monitors input voltage of each power supply pin and detects low voltage. It inputs the dividing voltage (VREG) of the resistors R1, R2, and R3 connected between power supplies and the reference voltage (VREF) generated in the IC to the comparator for detecting voltage. The comparator detects a potential difference between VREG and VREF even if it is inappreciable; therefore, a hysteresis circuit is added to avoid a possible defective condition due to power noise or the like.
In the example below, the detecting voltage (-VDET) with input voltage lowered and the release voltage (+VDET) with input voltage raised are set using the following formulas:
Detecting voltage: $-V_{DET} = (R2 + R3) / R3) \cdot V_{REF}$ (Formula 8.2.1)
Release voltage: $+V_{DET} = (R1 + R2 + R3 / R3) \cdot V_{REF}$ (Formula 8.2.2)

The power line is equipped with an output guarantee circuit that turns the power off when the voltage drops to below the output guarantee voltage and forces to set the *DET (*=C/U/B) pin to Hi-Z by fixing the XOFF signal to LOW
Fig.8.2.1 shows the VCC power voltage monitoring circuit.
Fig.8.2.2 shows the VBUS power voltage monitoring circuit.
Fig.8.2.3 shows the VBAT power voltage monitoring circuit.

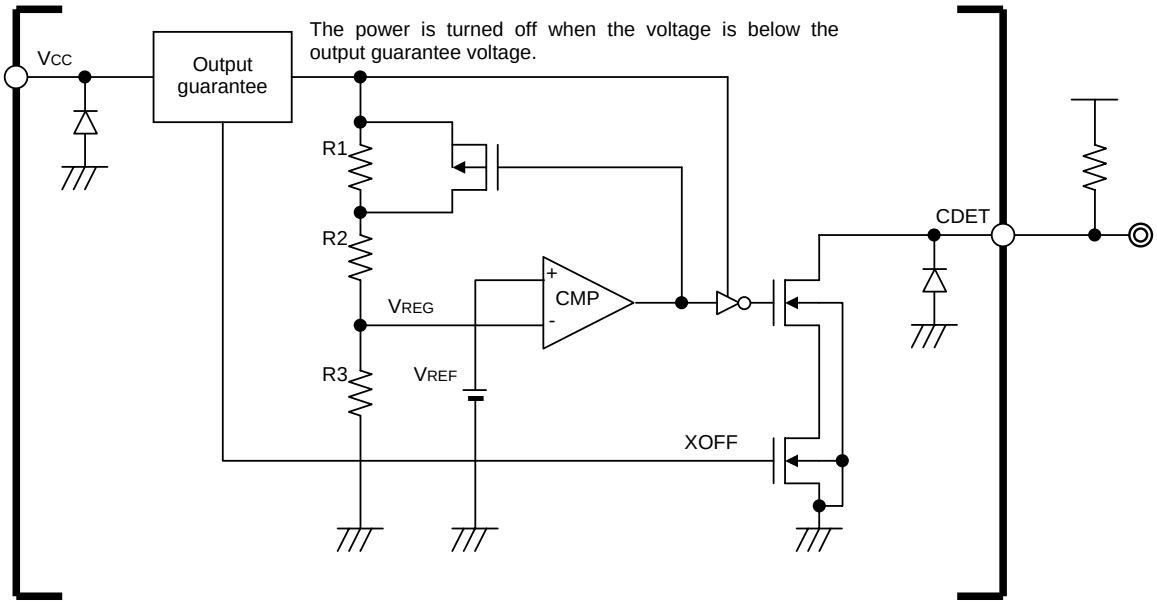


Fig.8.2.1 Block diagram for VCC power voltage monitoring circuit

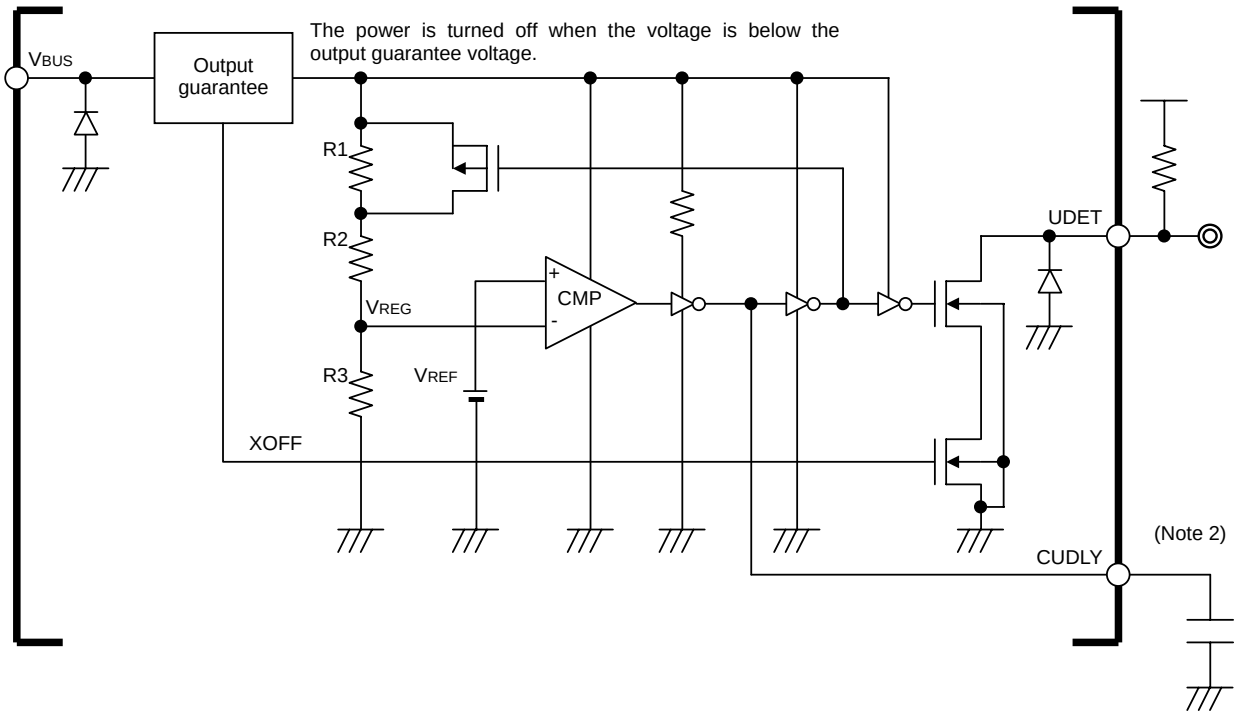


Fig.8.2.2 Block diagram for VBUS power voltage monitoring circuit

(Note 2) The release time may be specified by external capacitor only for the VBUS-system power voltage monitoring. The recommended value of the capacitor is approximately 50ms for 6800pF.

Typ.

Release delay setting time TUDLY [ms] = Set coefficient (7353) × C [μF]

In case of the recommended C=6800[pF], the release delay time is TUDLY=50[ms].

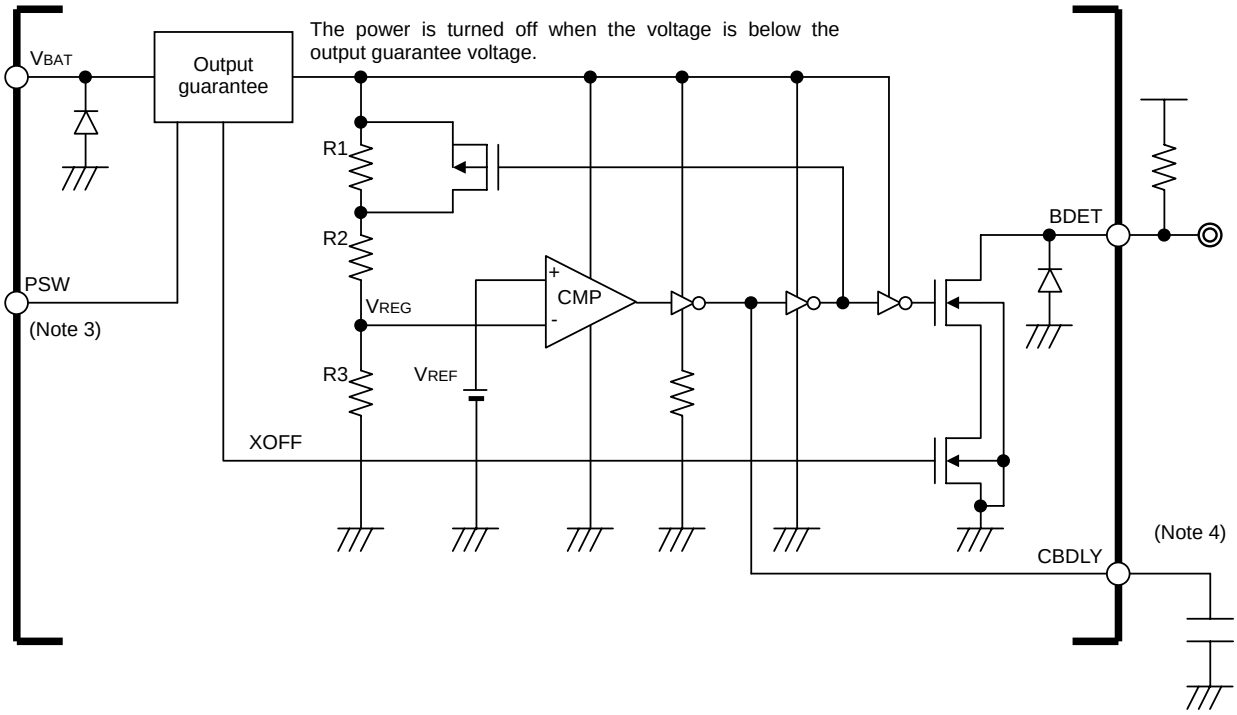


Fig.8.2.3 Block diagram for VBAT power voltage monitoring circuit

(Note 3) The power switch built in the output guarantee circuit may be turned ON/OFF by the PSW pin only for the VBAT-system power supply.

(Note 4) The detecting voltage dead time of power voltage monitoring may be specified by external capacitor only for the VBAT-system power supply. The recommended value of the capacitor is approximately 1s for 6800pF. However, when the voltage is temporarily below the output guarantee voltage, low voltage is detected even during the dead time.

Typ.
For detecting voltage = 1.6V, detecting voltage dead setting time TBDLY [S] = Set coefficient (147) × C [μF]
In case of the recommended C=6800[pF], the release delay time is TBDLY=1[S].

Typ.
For detecting voltage = 2.8V, detecting voltage dead setting time TBDLY [S] = Set coefficient (250) × C [μF]
In case of the recommended C=6800[pF], the release delay time is TBDLY=1.7[S].

8.3 Switching Control Circuit

This circuit controls output of a signal that selects optimum input power supply according to input conditions of three power supplies (V_{CC}, V_{BUS}, and V_{BAT}) and in the priority sequence set in the IC.

(1) Power input control logic

V_{CC} ①	V_{BUS} ②	V_{BAT} ③	V_{OUT} Output selection system
L	L	L	OFF
L	L	H	③
L	H	L	②
L	H	H	②(③)
H	L	L	①
H	L	H	①
H	H	L	①
H	H	H	①

(Note 5) The priority sequence may be changed with the BSEL pin.
It can be switched even during operation of IC.

(Note 6) L: Input disabled, H: Input enabled

(2) Switch configuration

Fig.8.4.1 shows the configuration diagram of power supply selection switches, that are configured outside the IC.
The O*1 (OC1, OU1, and OB1) pin performs over voltage limiter control while the O*2 (OC2, OU2, and OB2) pin controls backflow prevention.

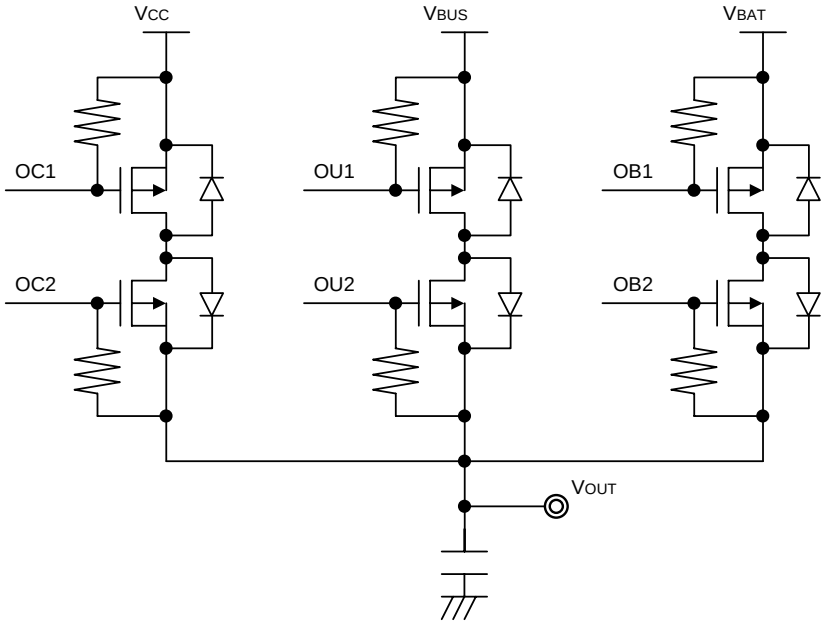
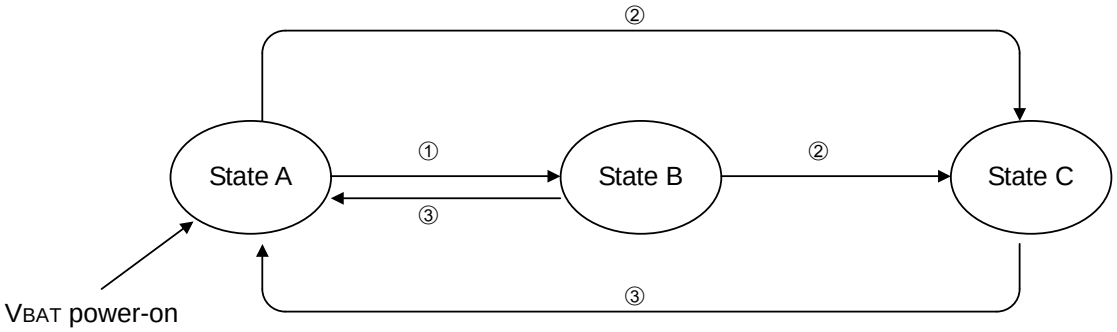


Fig.8.4.1 Switch configuration

(3) Power-on operation

Fig.8.4.2 shows an example of power-on operation from the initial state at power-on to the power selection.



Description of each state

State A: Input power not selected.
(OB1:OFF, OB2:OFF, OU1:OFF, OU2:OFF, OC1:OFF, OC2:OFF)

State B: VBAT input power supply selected, backflow from VOUT prevented
(OB1:ON, OB2:OFF, OU1:OFF, OU2:OFF, OC1:OFF, OC2:OFF)

State C: VBAT input power supply selected, full on state
(OB1:ON, OB2:ON, OU1:OFF, OU2:OFF, OC1:OFF, OC2:OFF)

Description of transition conditions

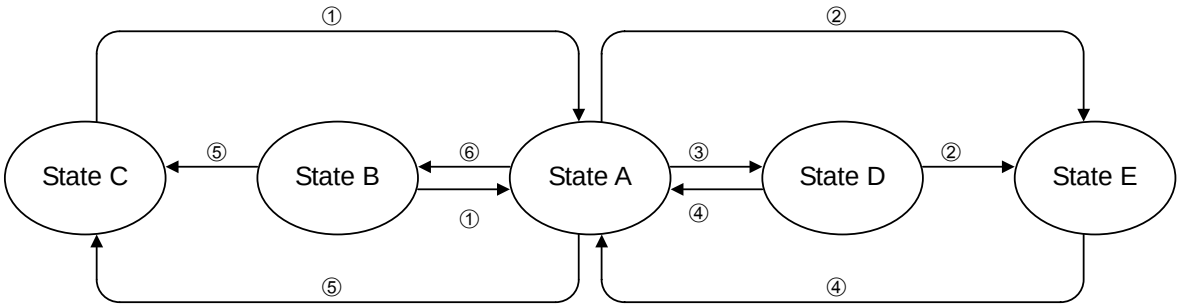
①: VBAT input enabled, backflow potential between input power supply (VBAT) and VOUT

②: VBAT input enabled, elimination of backflow potential between input power supply (VBAT) and VOUT (Typ. 19mV)

③: VBAT input disabled

Fig.8.4.2 State transition at VBAT power-on

(4) Power supply switching operation 1 (OFF-OFF switching)
Fig.8.4.3 shows an example of power supply switching operation 1 on connection / disconnection of power supply with a higher priority level.



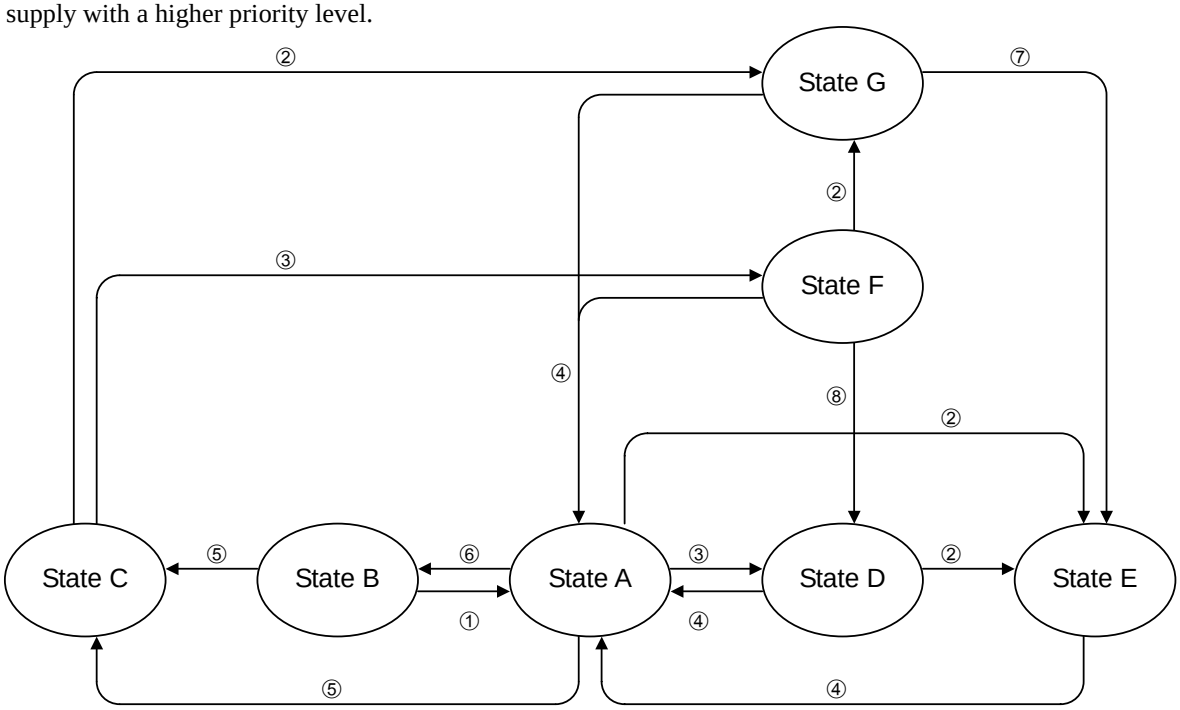
Description of each state
State A: Input power not selected.
(OB1:OFF, OB2:OFF, OU1:OFF, OU2:OFF, OC1:OFF, OC2:OFF)
State B: VBAT input power supply selected, backflow from VOUT prevented
(OB1:ON, OB2:OFF, OU1:OFF, OU2:OFF, OC1:OFF, OC2:OFF)
State C: VBAT input power supply selected, full on state
(OB1:ON, OB2:ON, OU1:OFF, OU2:OFF, OC1:OFF, OC2:OFF)
State D: VCC input power supply selected, backflow from VOUT prevented
(OB1:OFF, OB2:OFF, OU1:OFF, OU2:OFF, OC1:ON, OC2:OFF)
State E: VCC input power supply selected, full on state
(OB1:OFF, OB2:OFF, OU1:OFF, OU2:OFF, OC1:ON, OC2:ON)

Description of transition conditions
①: VCC & VBAT input enabled
②: VCC & VBAT input enabled, elimination of backflow potential between input power supply (VCC) and VOUT (Typ. 19mV)
③: VCC & VBAT input enabled, backflow potential between input power supply (VCC) and VOUT
④: VCC input disabled, VBAT input enabled
⑤: VCC input disabled, VBAT input enabled, elimination of backflow potential between input power supply (VBAT) and VOUT (Typ. 19 mV)
⑥: VCC input disabled, VBAT input enabled, backflow potential between input power supply (VBAT) and VOUT

Fig.8.4.3 VBAT ⇔ VCC power supply switching state transition 1

(5) Power supply switching operation 2 (ON-ON switching)

Fig.8.4.4 shows an example of power supply switching operation 2 on connection / disconnection of power supply with a higher priority level.



Description of each state

State A: Input power not selected.
(OB1:OFF, OB2:OFF, OU1:OFF, OU2:OFF, OC1:OFF, OC2:OFF)

State B: V_{BAT} input power supply selected, backflow from V_{OUT} prevented
(OB1:ON, OB2:OFF, OU1:OFF, OU2:OFF, OC1:OFF, OC2:OFF)

State C: V_{BAT} input power supply selected, full on state
(OB1:ON, OB2:ON, OU1:OFF, OU2:OFF, OC1:OFF, OC2:OFF)

State D: V_{CC} input power supply selected, backflow from V_{OUT} prevented
(OB1:OFF, OB2:OFF, OU1:OFF, OU2:OFF, OC1:ON, OC2:OFF)

State E: V_{CC} input power supply selected, full on state
(OB1:OFF, OB2:OFF, OU1:OFF, OU2:OFF, OC1:ON, OC2:ON)

State F: V_{BAT} and V_{CC} input power supplies selected simultaneously (ON-ON), backflow from V_{OUT} prevented on the V_{CC} side only.
(OB1:ON, OB2:ON, OU1:OFF, OU2:OFF, OC1:ON, OC2:OFF)

State G: V_{BAT} and V_{CC} input power supplies selected simultaneously (ON-ON), full on state
(OB1:ON, OB2:ON, OU1:OFF, OU2:OFF, OC1:ON, OC2:ON)

Description of transition conditions
①: VCC & VBAT input enabled
②: VCC & VBAT input enabled, elimination of backflow potential between input power supply (VCC) and VOUT (Typ. 19mV) (TBD)
③: VCC & VBAT input enabled, backflow potential between input power supply (VCC) and VOUT
④: VCC input disabled, VBAT input enabled
⑤: VCC input disabled, VBAT input enabled, elimination of backflow potential between input power supply (VBAT) and VOUT
⑥: VCC input disabled, VBAT input enabled, backflow potential between input power supply (VBAT) and VOUT
⑦: VCC & VBAT input enabled, elimination of backflow potential between input power supply (VCC) and VOUT (Typ. 19mV), simultaneous ON-time (Typ. 800µs) lapse
⑧: VCC & VBAT input enabled, backflow potential between input power supply (VCC) and VOUT (Typ. 19mV), simultaneous ON-time (Typ.800µs) lapse

Fig.8.4.4 VBAT ⇔ VCC power switching state transition 2

(Note 7) For ON-ON switching, input power supply is temporarily shorted. We recommend OFF-OFF switching, however, use ON-ON switching on your own authority after carefully evaluating the switching in the set if you want to minimize voltage drop when switching power supply. SEIKO EPSON, however, shall not be liable for any defective conditions or the like due to backflow to input power supply caused by ON-ON switching.

(Note 8) Combining the VBAT priority (BSEL=LOW) pin with the ON-ON switching (ONOFSW=HIGH) pin generates abnormal output waveforms at switching; therefore, this combination should be avoided to output normal waveforms.

(6) Overvoltage limiter control

If measures against overvoltage are required after output stage of VOUT, feed back and input voltage divided by resistance to the FB pin. To set the VOUT voltage, refer to the formula below. Set so that the total resistance of RFB1 + RFB2 is between 1 and 10 MegΩ .

$$V_{OUT}=V_{REF} \cdot ((RFB1+RFB2)/RFB2)$$

Incoming current can be prevented by connecting a capacitor for setting the soft start time to the CSFT pin as measures against incoming current at cold start (no charge in the VOUT smoothing capacitor). The setting time can be obtained from the following formula.

Typ.

Soft start setting time TSFT [ms] = Set coefficient (70) × C [μF]

For recommended C = 0.01 [μF], soft start time: TSFT = 0.7 [ms]

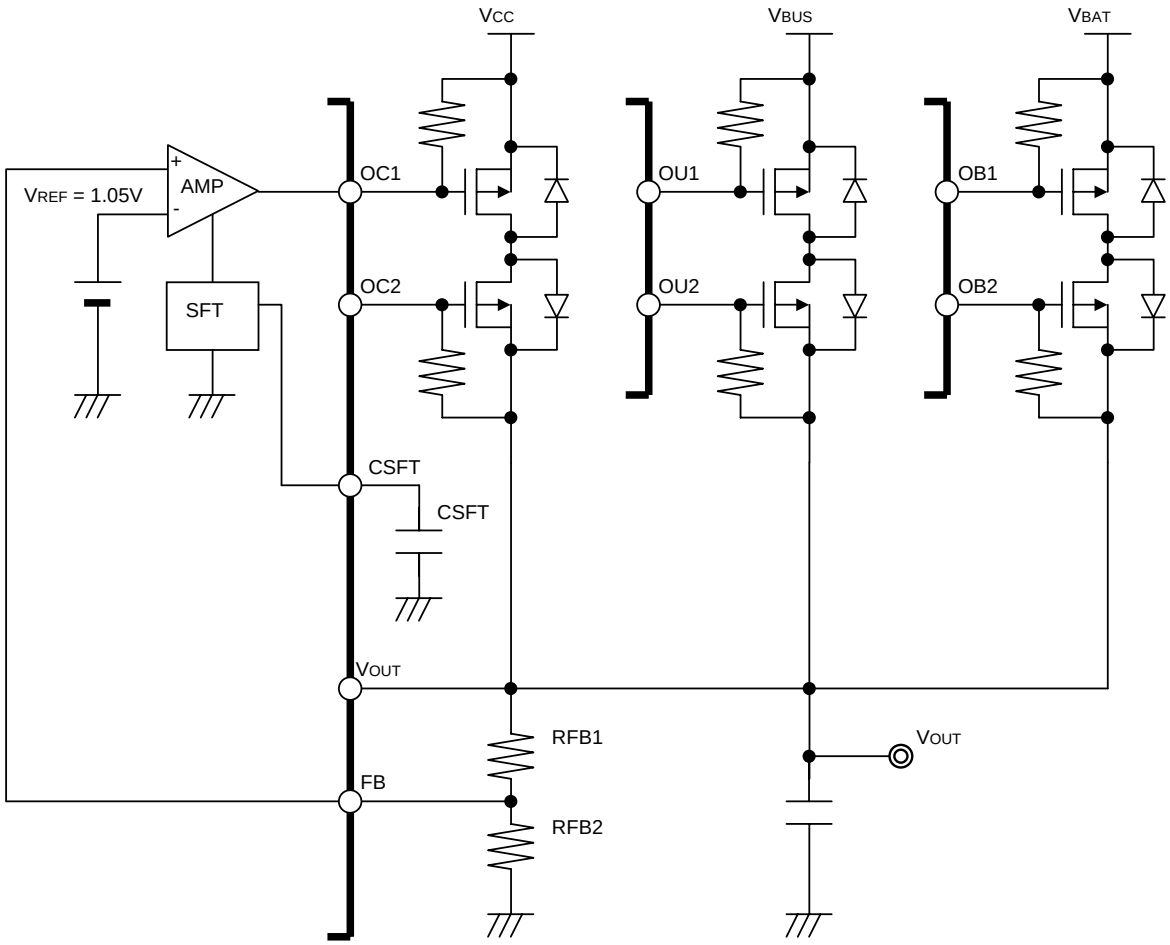


Fig.8.4.4 Overvoltage limiter circuit diagram

8.4 Recommended IC Protection Circuit

The following external circuits for protection of IC are recommended.

(1) Measures against reverse insertion of VCC power supply

Reverse insertion of power supply causes an IC breakage. Using the following external circuit configuration prevents an IC breakage.

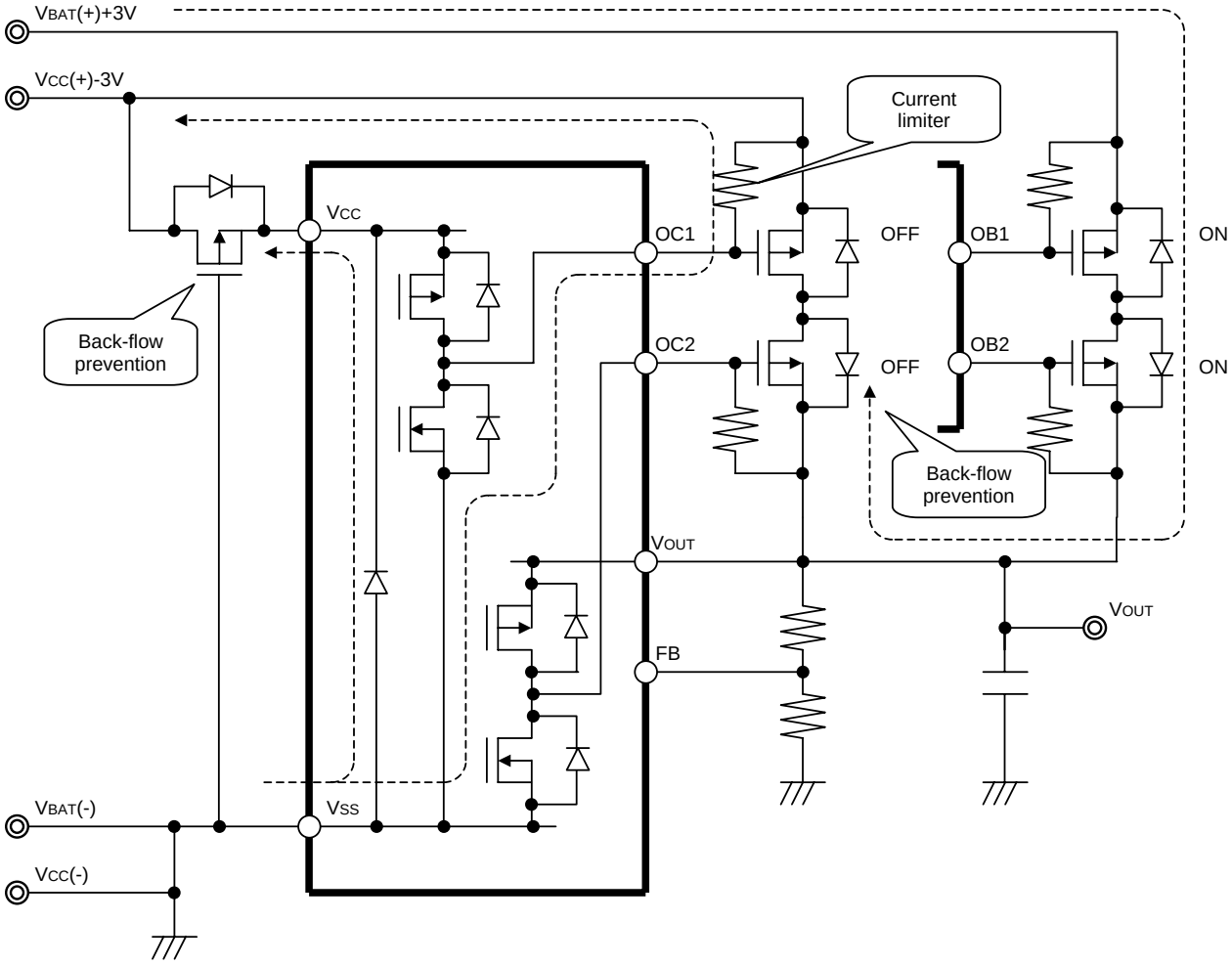


Fig.8.5.1 VCC power supply reverse-insertion support circuit

(2) Measures against input power supply floating

Causing the floating state by removing the input power supplies (VCC, VBUS, and VBAT) may eliminate the load and reach the midpoint potential. This state is not effective for the IC, so we recommend that the IC be connected to a discharge resistor. The recommended resistance value is between 1 and 2.2 MegΩ. If a lower resistance is required depending on setting conditions, however, determine the appropriate value after careful evaluation.

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

Item	Symbol	Rated value		Unit	Applicable pin	Remarks
		Min.	Max.			
Input power voltage	V_{IN}	V_{SS}-0.3	9.0	V	V_{CC}, V_{BUS}, V_{BAT}, V_{OUT}	—
Input pin voltage 1	V_{I1}	V_{SS}-0.3	V_{BAT}+0.3	V	BSEL	—
Input pin voltage 2	V_{I2}	V_{SS}-0.3	9.0	V	PSW, IQ	—
Input pin voltage 3	V_{I3}	V_{SS}-0.3	V_{DD}+0.3	V	ONOFSW	(Note 9)
Output voltage	V_O	V_{SS}-0.3	9.0	V	OC1, OC2, OU1, OU2, OB1, OB2, CDET, UDET, BDET	—
Output current	I_{OX1}	—	10	mA	OC1, OU1, OB1	—
	I_{OX2}	—	100	mA	OC2, OU2, OB2	—
	I_{XDET}	—	10	mA	CDET, UDET, BDET	—
Allowable dissipation	P_d	—	550	mW	—	—
Operating temperature	T_{opr}	-30	85	°C	—	—
Storage temperature	T_{stg}	-55	150	°C	—	—
Soldering temperature and time	T_{sol}	—	260•10	°C•s	—	—

(Note 9) V_{DD} provides the power supply with V_{CC}, V_{BUS} and V_{BAT} set to the highest power level.

(Note 10) Do not externally apply the voltage to the output pin.

(Note 11) Using with a condition exceeding the above absolute maximum rating may result in malfunction or unrecoverable damage. Moreover, normal function may be achieved temporarily but its reliability may be significantly low.

9.2 Recommended Operating Conditions

Item	Symbol	Standard value			Unit	Remarks
		Min.	Typ.	Max.		
Input voltage	V_{CC}	0.0	—	6.5	V	
	V_{BUS}	0.0	—	6.5	V	
	V_{BAT}	0.0	—	6.5	V	
	V_{OUT}	0.0	—	6.5	V	
Output voltage	OX1	0.0	—	6.5	V	OC1, OU1, OB1
	OX2	0.0	—	6.5	V	OC2, OU2, OB2
	XDET	0.0	—	6.5	V	CDET, UDET, BDET
Smoothing capacitor	CV_{CC}	—	1.0	—	µF	(Note 13)
	CV_{BUS}	—	1.0	—	µF	(Note 13)
	CV_{BAT}	—	1.0	—	µF	(Note 13)
	CV_{DD}	—	0.1	—	µF	
	CV_{OUT}	—	94	—	µF	(Note 14)
Dead time setting capacitor	CBDLY	—	6800	—	pF	TBDLY=1s
Release time setting capacitor	CUDLY	—	6800	—	pF	TUDLY=50ms
Soft start setting capacitor	CSFT	—	0.01	—	µF	TSFT=0.7ms
Pull-up resistor	ROX1	1	—	4.7	MΩ	OC1, OU1, OB1
	ROX2	1	—	4.7	MΩ	OC2, OU2, OB2
	RXDET	470	—	—	kΩ	CDET, UDET, BDET
Pull-down resistor	RV_{CC}	1	—	2.2	MΩ	V_{CC}
	RV_{BUS}	1	—	2.2	MΩ	V_{BUS}
	RV_{BAT}	1	—	2.2	MΩ	V_{BAT}
Total feedback resistor	RFB	1	—	10	MΩ	RFB1+RFB2
External MOS FET	MOS	—	—	—	—	(Note 14)

(Note 12) All the values are based on V_{SS} = 0V.

(Note 13) It is recommended to use a tantalum capacitor of ESR = 1 Ω or more.

(Note 14) Connect 47 µF capacitors in parallel to increase the capacity.

(Note 15) It is recommended to use ON Semiconductor NTHD2102P.

9.3 Electrical Characteristics

9.3.1 Overall Operations

S1F76980F0A, S1F7698F0B, S1F7698F0C — T_a=25°C unless otherwise specified

Item	Symbol	Standard value			Unit	Conditions
		Min.	Typ.	Max.		
Range of input voltage	V_{CC}	0.0	—	6.5	V	
	V_{BUS}	0.0	—	6.5	V	
	V_{BAT}	0.0	—	6.5	V	
	V_{OUT}	0.0	—	6.5	V	
V_{CC}-system consumption current 1	IoprC1	—	33	45	µA	V_{CC}=6V, V_{BUS}=V_{BAT}=0V
V_{CC}-system consumption current 2	IoprC2	—	33	55	µA	V_{CC}=6V, V_{BUS}=V_{BAT}=0V T_a=-30°C to +85°C
V_{BUS}-system consumption current 1	IoprU1	—	27	38	µA	V_{BUS}=5V, V_{CC}=V_{BAT}=0V
V_{BUS}-system consumption current 2	IoprU2	—	27	50	µA	V_{BUS}=5V, V_{CC}=V_{BAT}=0V T_a=-30°C to +85°C
V_{OUT}-system consumption current 1	IoprO1	—	1.3	2	µA	V_{CC}=V_{BUS}=V_{BAT}=5V, V_{OUT}=3.5V, FB=0V
V_{OUT}-system consumption current 2	IoprO2	—	1.3	2.4	µA	V_{CC}=V_{BUS}=V_{BAT}=5V, V_{OUT}=3.5V, FB=0V, T_a=-30°C to +85°C

S1F76980F0A — T_a=25°C unless otherwise specified

Item	Symbol	Standard value			Unit	Conditions
		Min.	Typ.	Max.		
V_{BAT}-system consumption current 1	IoprB1	—	27	46	µA	V_{BAT}=3.6V, V_{CC}=V_{BUS}=0V
V_{BAT}-system consumption current 2	IoprB2	—	27	54	µA	V_{BAT}=3.6V, V_{CC}=V_{BUS}=0V, T_a=-30°C to +85°C
V_{BAT}-system consumption current 3	IoprB3	—	0.6	2	µA	V_{BAT}=2.0V, V_{CC}=V_{BUS}=0V
V_{BAT}-system consumption current 4	IoprB4	—	0.1	1	µA	V_{BAT}=PSW=3.6V, V_{CC}=V_{BUS}=0V, T_a=-30°C to +85°C
V_{BAT}-system consumption current 5	IoprB5	—	16	32	µA	V_{BAT}=VHIZ to -BDET, V_{CC}=V_{BUS}=0V, T_a=-30°C to +85°C (Note 16)

S1F76980F0B, S1F7698F0C — T_a=25°C unless otherwise specified

Item	Symbol	Standard value			Unit	Conditions
		Min.	Typ.	Max.		
V_{BAT}-system consumption current 1	IoprB1	—	20	33	µA	V_{BAT}=2.5V, V_{CC}=V_{BUS}=0V
V_{BAT}-system consumption current 2	IoprB2	—	20	40	µA	V_{BAT}=2.5V, V_{CC}=V_{BUS}=0V, T_a=-30°C to +85°C
V_{BAT}-system consumption current 3	IoprB3	—	0.3	1	µA	V_{BAT}=1.0V, V_{CC}=V_{BUS}=0V
V_{BAT}-system consumption current 4	IoprB4	—	0.1	1	µA	V_{BAT}=PSW=2.5V, V_{CC}=V_{BUS}=0V, T_a=-30°C to +85°C
V_{BAT}-system consumption current 5	IoprB5	—	12	24	µA	V_{BAT}=VHIZ to -BDET, V_{CC}=V_{BUS}=0V, T_a=-30°C to +85°C (Note 16)

(Note 16) This value may be higher than the current value described above by detecting or releasing the output guarantee voltage near the output guarantee circuit VHIZ. If the voltage drops to below VHIZ, this value is set to the current value of V_{BAT}-system consumption current 3.

9.3.2 Vcc Voltage Monitoring Circuit Characteristics

S1F76980F0A, S1F76980F0B, S1F7698F0C Ta=25°C unless otherwise specified

Item	Symbol	Standard value			Unit	Conditions
		Min.	Typ.	Max.		
Detecting voltage	-CDET	×0.97	Set voltage	×1.03	V	
Release voltage	+CDET	×0.97	Set voltage	×1.03	V	
Output current	ICDET	0.9	1.6	—	mA	Nch open drain output, VCC=6V, CDET=1.5V
Transmission delay time	TPLHC	—	0.2	0.4	ms	Nch open drain output, (Note 32), (Note 18), S1F76980F0A
		—	0.13	0.26	ms	Nch open drain output, (Note 32), (Note 19), S1F7698F0B, S1F7698F0C
	TPHLC	—	—	100	µs	Nch open drain output, (Note 32), (Note 20), S1F76980F0A
		—	—	100	µs	Nch open drain output, (Note 32), (Note 21), S1F7698F0B, S1F7698F0C
Detecting voltage temperature characteristics	Δ-CDET /ΔTopr	—	±100	—	ppm/°C	Ta=-30°C to +85°C, (Note 17), S1F7698F0C
Release voltage temperature characteristics	Δ+CDET /ΔTopr	—	±100	—	ppm/°C	Ta=-30°C to +85°C, (Note 17), S1F7698F0C

(Note 17) The temperature characteristics are obtained from the following formula.
$\Delta CDET/\Delta Topr=(((CDETH-CDETL)/CDETM)/115) \cdot 10^{6}$
Detecting / release voltage value at CDETH: 85°C
Detecting / release voltage value at CDETL: -30°C
Detecting / release voltage value at CDETM: 25°C

(Note 18) The VCC power is used as the standard value at VCC=4.95V → 6V.

(Note 19) The VCC power is used as the standard value at VCC=2.25V → 3V.

(Note 20) The VCC power is used as the standard value at VCC=6V → 4.95V.

(Note 21) The VCC power is used as the standard value at VCC=3V → 2.25V.

9.3.3 VBUS Voltage Monitoring Circuit Characteristics

S1F76980F0A, S1F76980F0B, S1F7698F0C Ta=25°C unless otherwise specified

Item	Symbol	Standard value			Unit	Conditions
		Min.	Typ.	Max.		
Detecting voltage	-UDET	×0.97	Set voltage	×1.03	V	
Release voltage	+UDET	×0.97	Set voltage	×1.03	V	
Output current	IUDET	0.9	1.6	—	mA	Nch open drain output, VBUS=6V, UDET=1.5V
Transmission delay time	TPLHU	35	50	65	ms	Nch open drain output, (Note 32), (Note 23)
	TPHLU	—	—	100	µs	Nch open drain output, (Note 32), (Note 24)
Detecting voltage temperature characteristics	Δ-UDET /ΔTopr	—	±100	—	ppm/°C	Ta=-30°C to +85°C, (Note 22)
Release voltage temperature characteristics	Δ+UDET /ΔTopr	—	±100	—	ppm/°C	Ta=-30°C to +85°C, (Note 22)

(Note 22) The temperature characteristics are obtained from the following formula.
$\Delta UDET/\Delta Topr=(((UDETH-UDETL)/UDETM)/115) \cdot 10^{6}$
Detecting / release voltage value at UDETH: 85°C
Detecting / release voltage value at UDETL: -30°C
Detecting / release voltage value at UDETM: 25°C

(Note 23) This is the standard value for the release delay capacitor at CUDLY=6800pF, VBUS=3.75V → 5V, and Ta=25°C.
The capacity accuracy of capacitor is not included in the standard values. We recommend that you select highly accurate capacitors.

(Note 24) This is the standard value for the release delay capacitor at CUDLY=6800pF and VBUS=5V → 3.75V.

9.3.4 V_{BAT} Voltage Monitoring Circuit Characteristics

S1F76980F0A, S1F7698F0B, S1F7698F0C T_a=25°C unless otherwise specified

Item	Symbol	Standard value			Unit	Conditions
		Min.	Typ.	Max.		
Detecting voltage	-BDET	×0.97	Set voltage	×1.03	V	
Release voltage	+BDET	×0.97	Set voltage	×1.03	V	
Output guarantee voltage	VHIZ	—	2.25	—	V	S1F76980F0A
		—	1.15	—	V	S1F76980F0B, S1F76980F0C
Output current	IBDET	0.9	1.6	—	mA	Nch open drain output, V_{BAT}=6V, BDET=1.5V
Transmission delay time	TPLHB	—	0.19	0.38	ms	Nch open drain output, (Note 32), (Note 27), S1F7698F0A
		—	0.13	0.26	ms	Nch open drain output, (Note 32), (Note 28), S1F7698F0B, S1F7698F0C
	TPHLB	0.85	1.70	3.40	S	Nch open drain output, (Note 32), (Note 26), S1F7698F0A
		0.5	1	2	S	Nch open drain output, (Note 32), (Note 26), S1F7698F0B, S1F7698F0C
Detecting voltage temperature characteristics	Δ-BDET /ΔT_{opr}	—	±100	—	ppm/°C	T_a=-30°C to +85°C, (Note 25), S1F7698F0C
Release voltage temperature characteristics	Δ+BDET /ΔT_{opr}	—	±100	—	ppm/°C	T_a=-30°C to +85°C, (Note 25), S1F7698F0C

(Note 25) The temperature characteristics are obtained from the following formula.
$\Delta BDET/\Delta Topr=(((BDETH-BDETL)/BDETM)/115) \cdot 10^{6}$
Detecting / release voltage value at BDETH: 85°C
Detecting / release voltage value at BDETL: -30°C
Detecting / release voltage value at BDETM: 25°C

(Note 26) This is the standard value for the dead time setting capacitor at CBDLY=6800pF, V_{BAT}=4.2V → 2.75V (F0A)/3V → 1.55V (F0B, F0C), and T_a=25°C. The capacity accuracy of capacitor is not included in the standard values. We recommend that you select highly accurate capacitors.

(Note 27) This is the standard value for the dead time setting capacitor at CBDLY=6800pF and V_{BAT}=2.75V→4.2V.

(Note 28) This is the standard value for the dead time setting capacitor at CBDLY=6800pF and V_{BAT}=1.55V→3V.

9.3.5 Overvoltage Limiter Characteristics

S1F76980F0A, S1F76980F0B, S1F7698F0C T_a=25°C unless otherwise specified

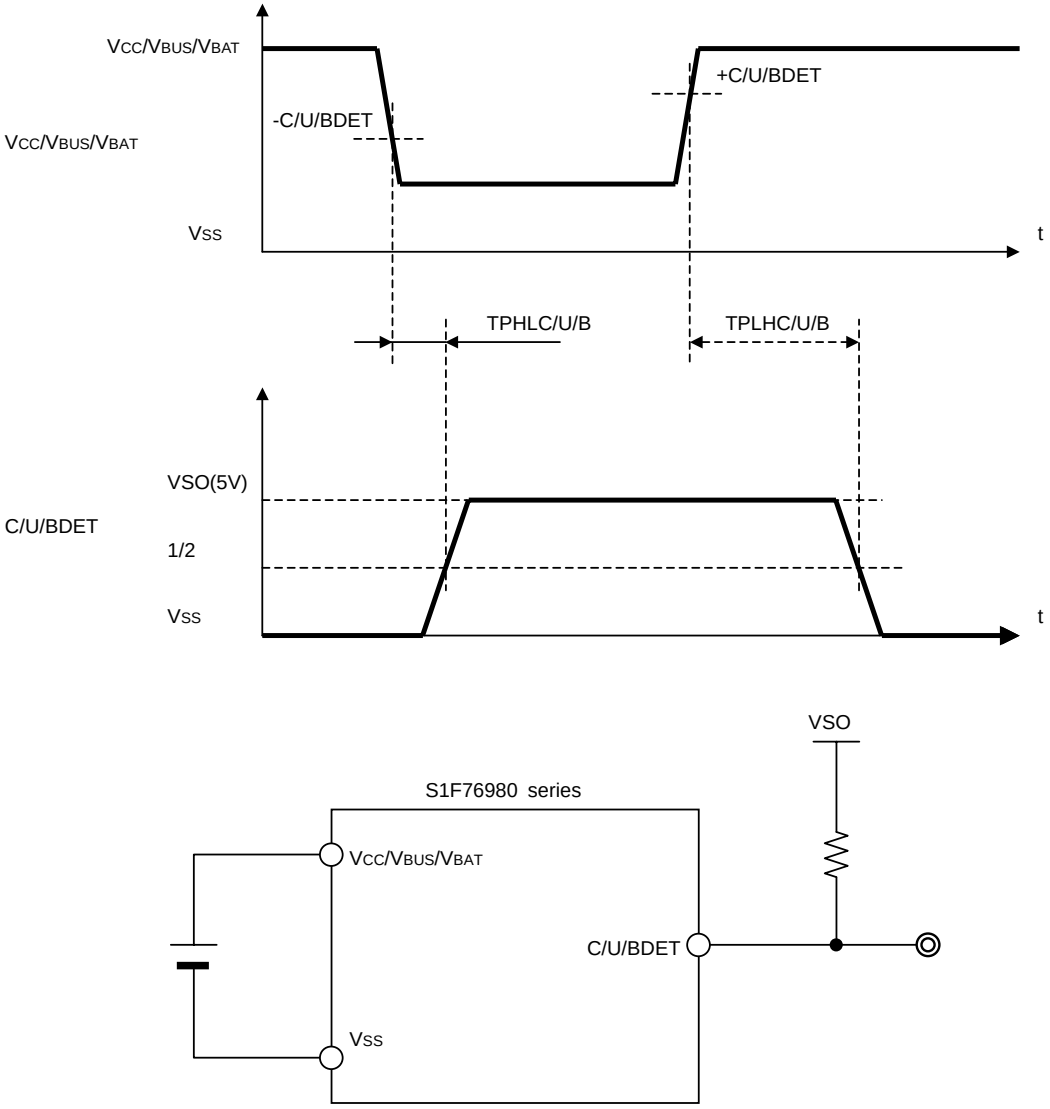
Item	Symbol	Standard value			Unit	Conditions
		Min.	Typ.	Max.		
Range of input voltage	V_{IN}	—	—	6.5	V	
Output voltage	V_{OUT}	×0.95	Set voltage	×1.05	V	Set by feedback resistor. (Note 31)
Output load current	IV_{OUT}	0.05	—	500	mA	V_{IN}-V_{OUT}=0.5V
Input stability	$\Delta V_{OUT}/\Delta V_{IN}$	-0.2	0.1	0.2	%/V	V_{OUT}+0.5V≤V_{IN}≤6.5V
Load stability	$\Delta V_{OUT}/\Delta IV_{OUT}$	0	0.5	1	mV	V_{IN}-V_{OUT}=0.5V 1mA≤IV_{OUT}≤100mA
Output voltage temperature coefficient	$\Delta V_{OUT}/\Delta T_{opr}$	—	±100	—	ppm/°C	V_{IN}-V_{OUT}=1.0V, IV_{OUT}=100mA, T_a=-30°C to +85°C, (Note 21)

(Note 29) These characteristics are applicable when the recommended parts are connected. If you use parts other than recommended ones, be sure to carefully evaluate them.

(Note 30) The temperature characteristics are obtained from the following formula.
$\Delta V_{OUT}/\Delta Topr=(((V_{OUTH}-V_{OUTL})/V_{OUTM})/115) \cdot 10^6$
Output voltage value at V_{OUTH}: 85°C
Output voltage value at V_{OUTL}: -30°C
Output voltage value at V_{OUTM}: 25°C

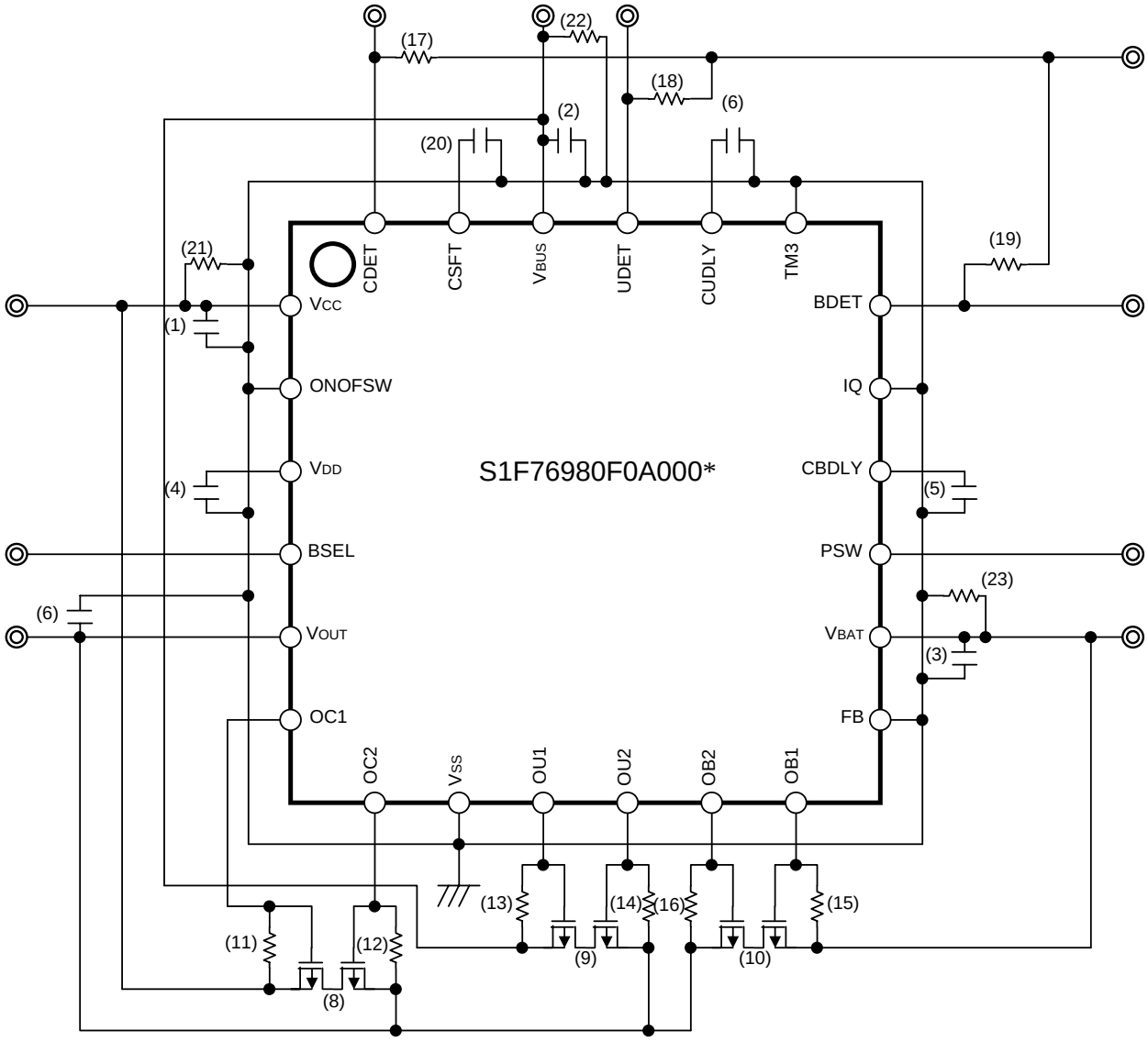
(Note 31) The standard value does not include an error by the feedback resistance voltage dividing ratio.

(Note 32) Measurement of transmission delay time (Nch open drain output)



10. EXTERNAL CONNECTION DIAGRAMS

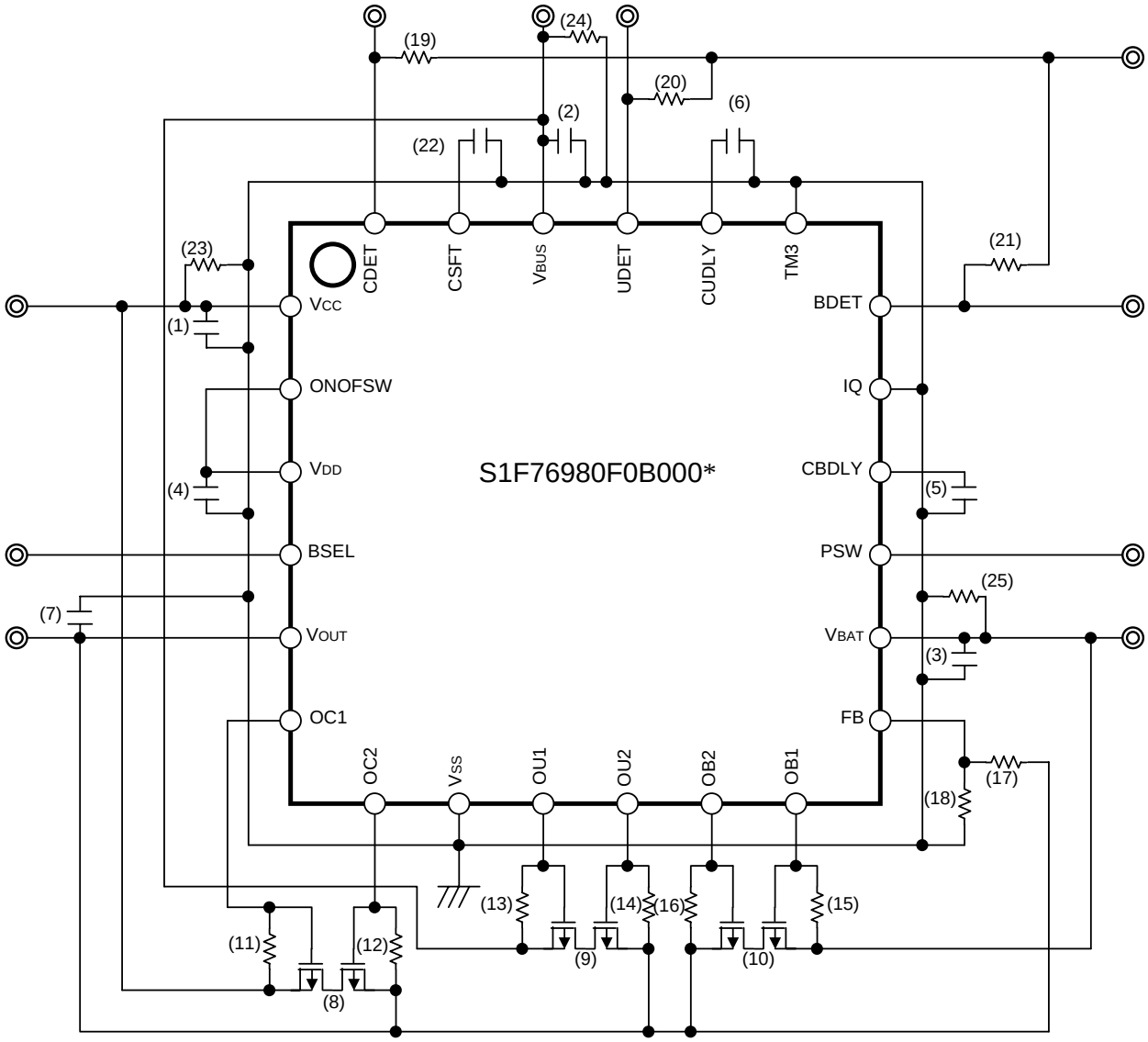
10.1 S1F76980F0A000B Recommended Connection (For 1-cell Li-ion, OFF-OFF switching, overvoltage limiter not used)



(1) CV_{CC}= (2) CV_{BUS}= (3) CV_{BAT}=1.0µF(ESR≥1Ω, tantalum), (4) CV_{DD}=0.1µF, (5) CBDLY=6800pF,
(6) CUDLY=6800pF, (7) CV_{OUT}=94µF (Connect 47µF capacitors in parallel.)
(8)(9)(10) MOS FET=NTHD2102P (Manufactured by ON Semiconductor.)
(11) ROC1= (12) ROC2= (13) ROU1= (14) ROU2= (15) ROB1= (16) ROB2=2.2MegΩ
(17) RCDET= (18) RUDET= (19) RBDET=470kΩ, (20) CSFT=0.01µF
(21) RV_{CC}= (22) RV_{BUS}= (23) RV_{BAT}=1MegΩ

(Note 33) The recommended connection diagram is carefully evaluated, ensure to verify characteristics by installing the machine onto the set before using it.

10.2 S1F76980F0B/C000B Recommended Connection (For 2-cell dry battery, ON-ON switching, overvoltage limiter used)



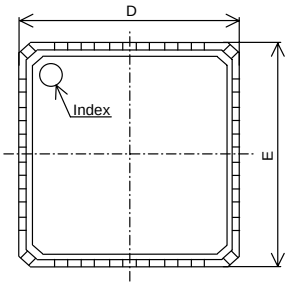
(1) CVCC= (2) CVBUS= (3) CVBAT=1.0µF (ESR≥1Ω, tantalum), (4) CVDD=0.1µF, (5) CBDLY=6800pF
(6) CUDLY=6800pF, (7) CVOUT=94µF (Connect 47µF capacitors in parallel.)
(8)(9)(10) MOS FET=NTHD2102P (Manufactured by ON Semiconductor.)
(11) ROC1= (12) ROC2= (13) ROU1= (14) ROU2= (15) ROB1= (16) ROB2=2.2MegΩ
(17) RFB1=1.0MegΩ, (18) RFB2=0.47MegΩ (Internal reference = 1.05V, VOUT = 3.284V targeted.)
(19) RCDET= (20) RUDET= (21) RBDET=470kΩ, (22)CSFT=0.01µF
(23) RVCC= (24) RVBUS= (25) RVBAT=1MegΩ

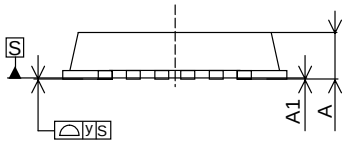
(Note 34) The recommended connection diagram is carefully evaluated, ensure to verify characteristics by installing the machine onto the set before using it.

11. DIMENSIONAL OUTLINE DRAWING (QFN4-24)

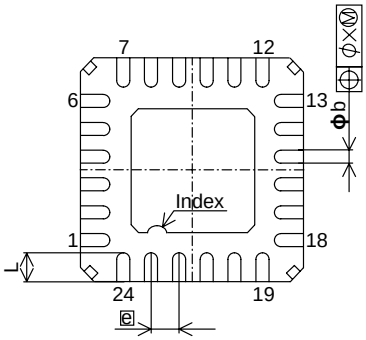
Top View

Reference





Bottom View

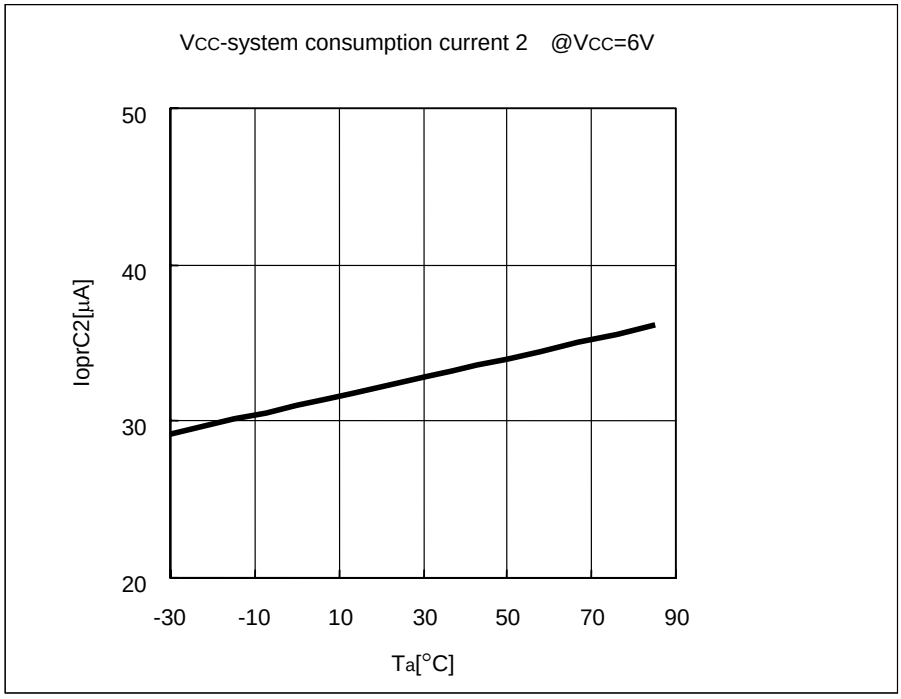


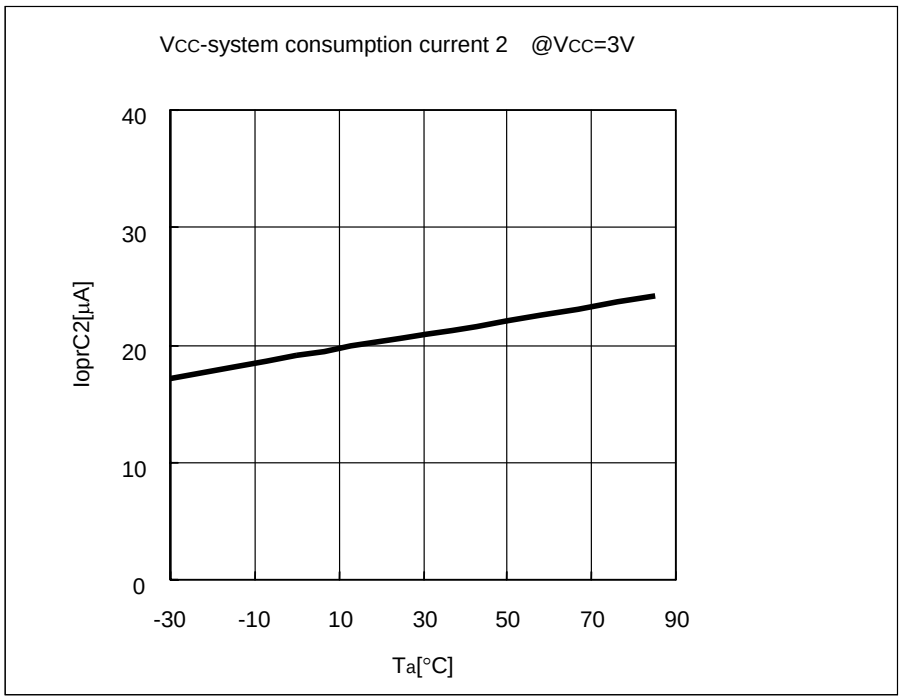
Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	4	—
E	—	4	—
A	—	—	1
A_1	0	—	—
b	0.17	—	0.3
e	—	0.5	—
L	0.3	—	0.5
x	—	—	0.1
y	—	—	0.05

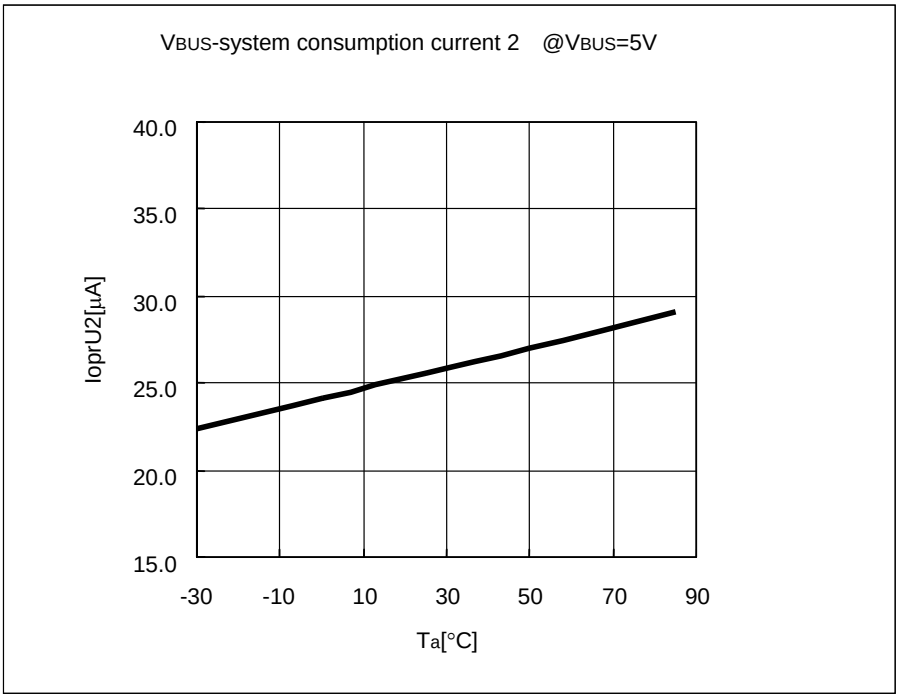
1 = 1 mm

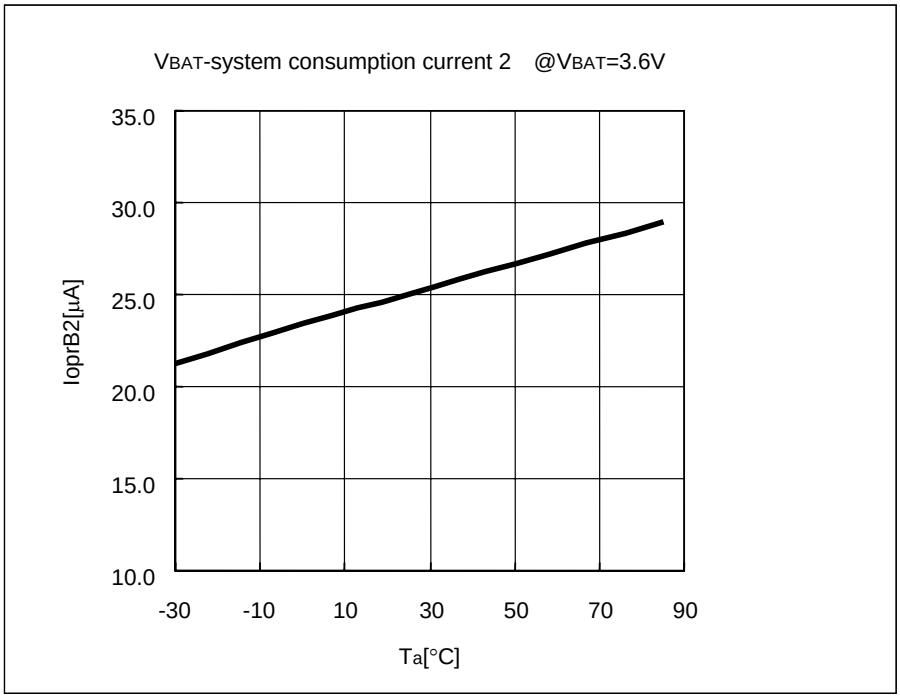
12. CHARACTERISTIC DATA

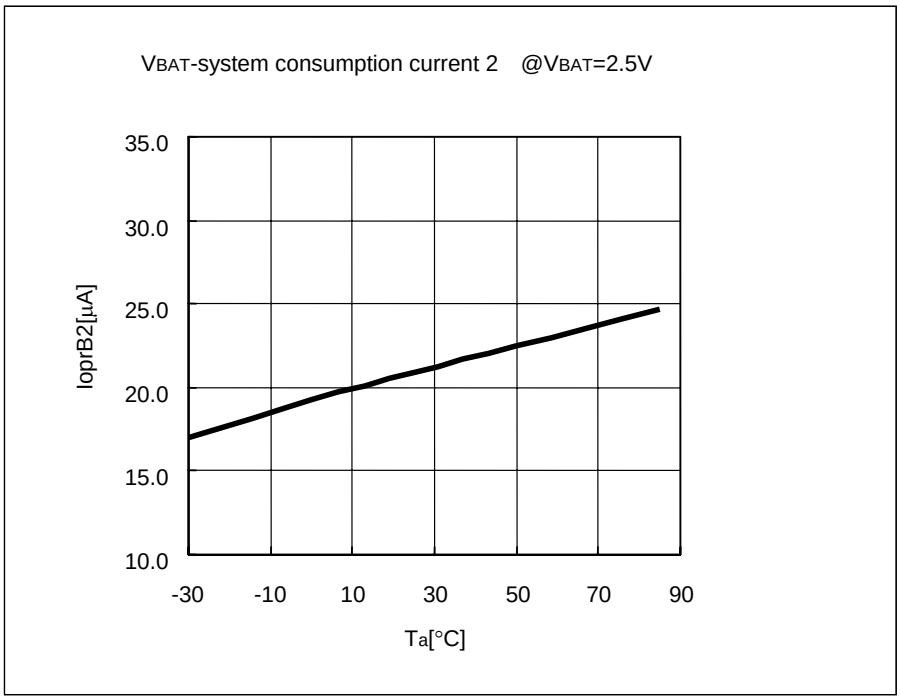
12.1 S1F76980F0C000* Characteristic Data

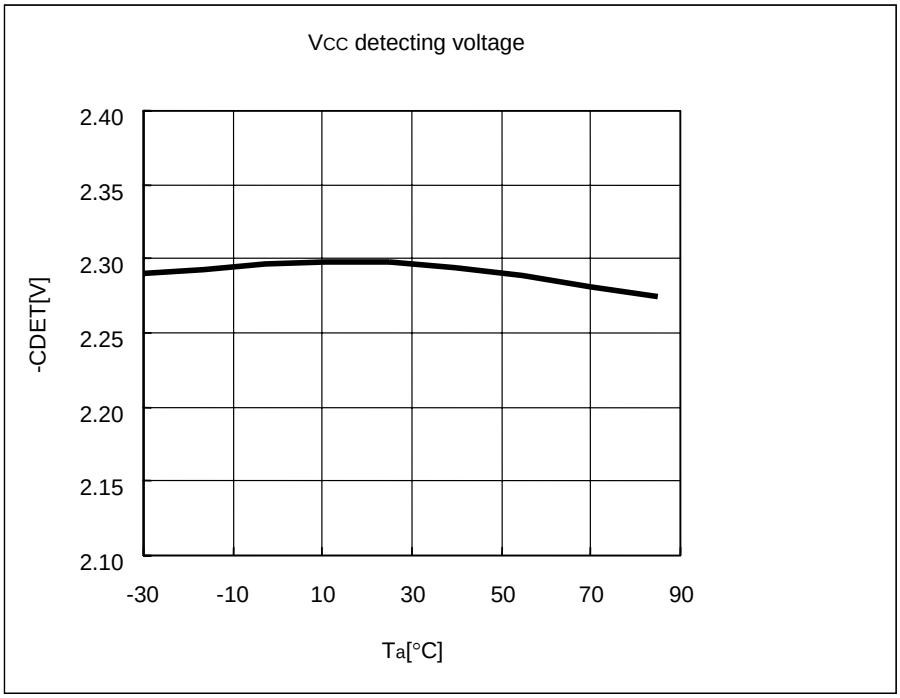


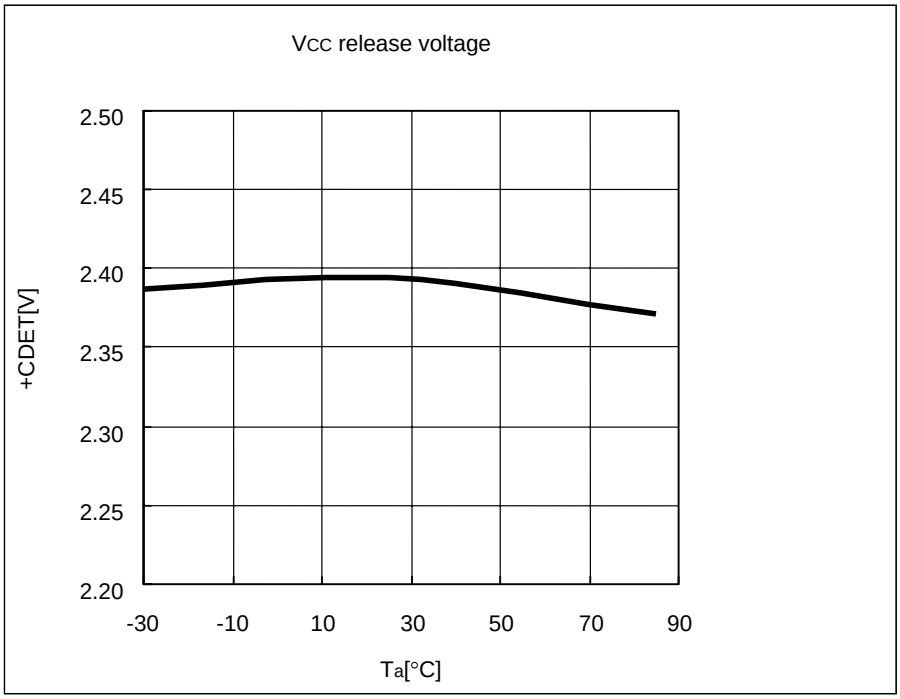


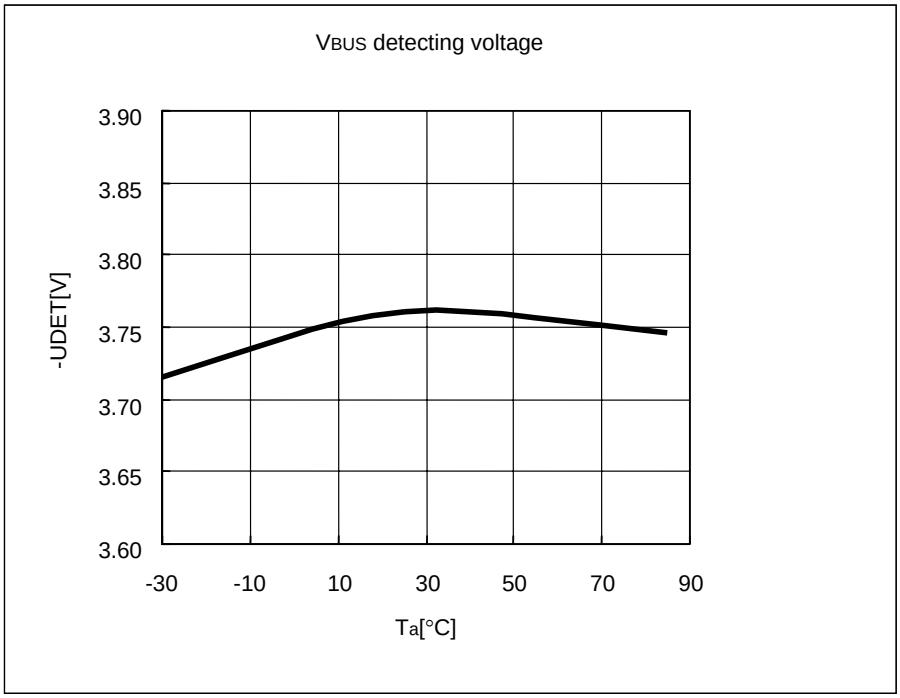


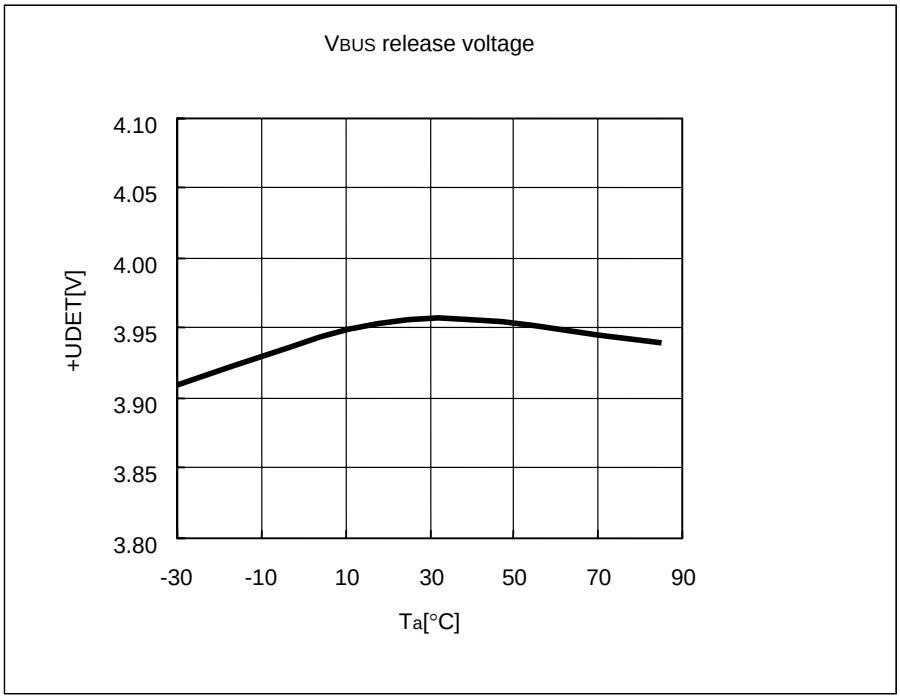


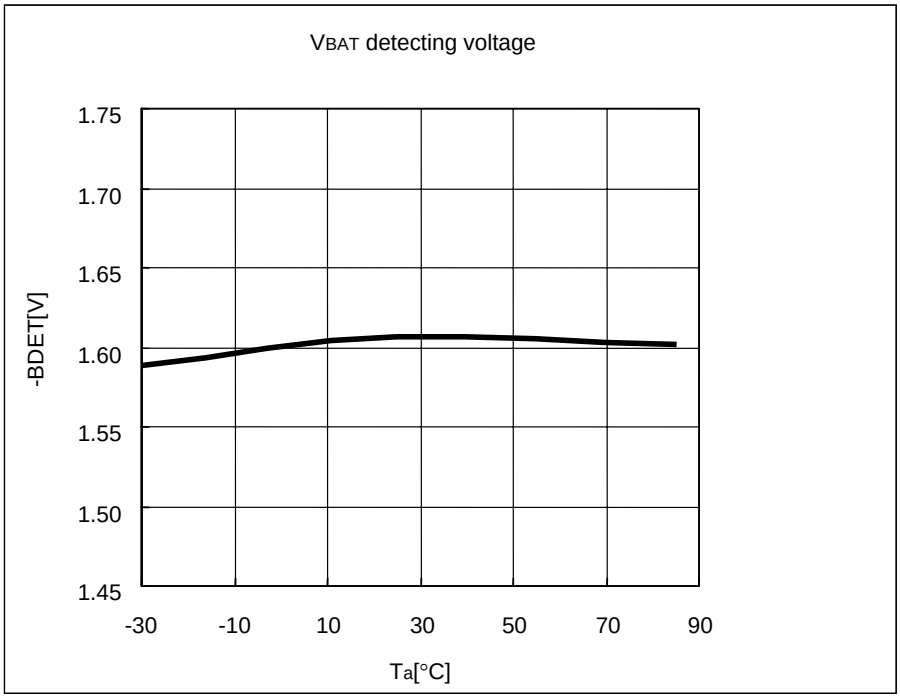


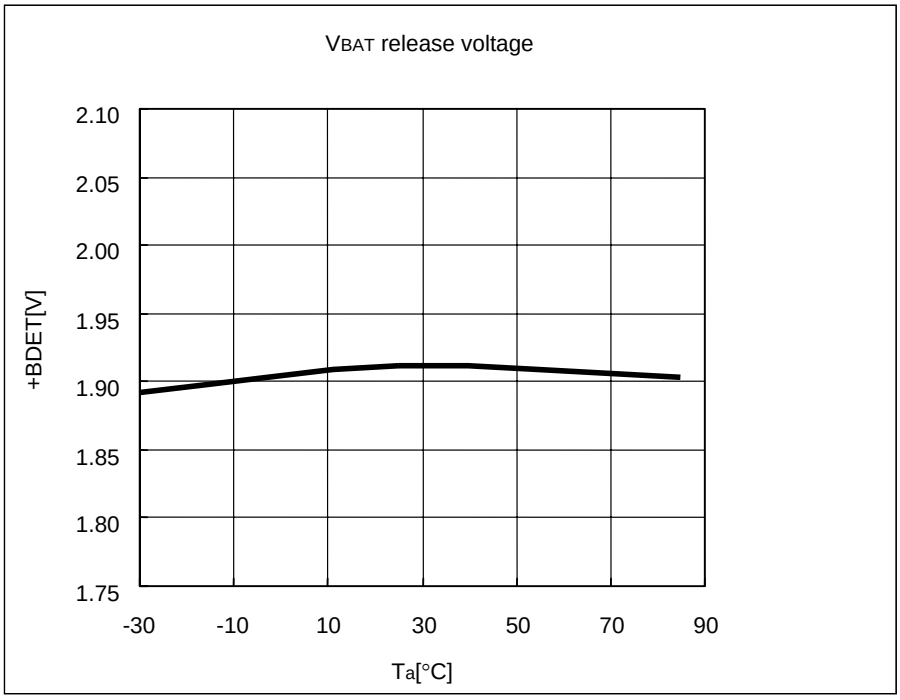


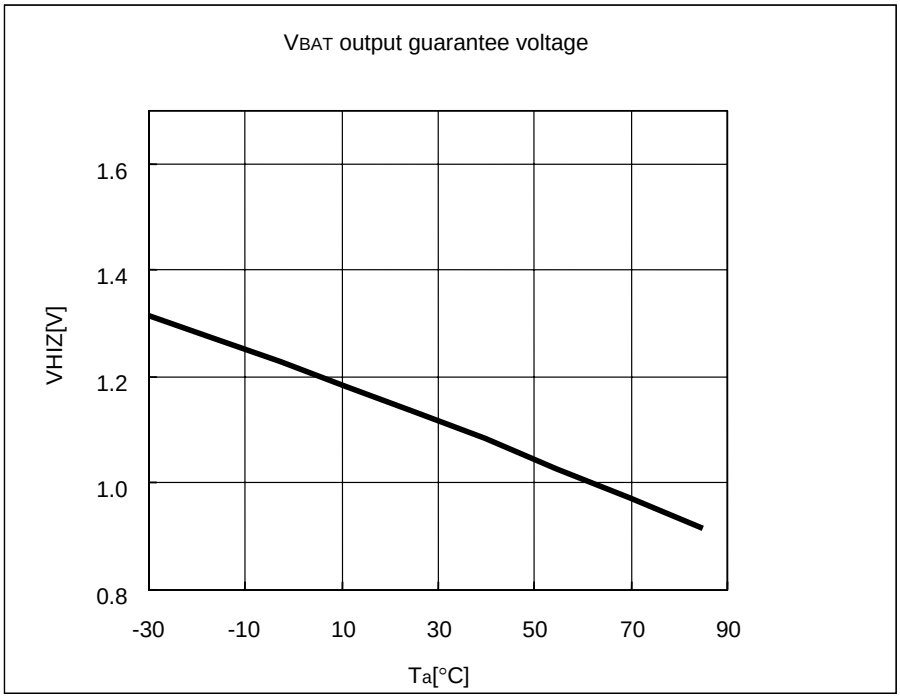












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