

# RM3283

## Dual ARINC 429 Line Receiver

### Features

- Two separate analog receiver channels
- Converts ARINC 429 levels to serial data
- Built-in TTL compatible complete channel test inputs
- TTL and CMOS compatible outputs
- Low power dissipation
- Internal bandgap
- Short circuit protected
- Available in 20-Lead ceramic DIP

### Description

The RM3283 consists of two analog ARINC 429 receivers which take differentially encoded ARINC level data and convert it to serial TTL level data. The RM3283 provides two complete analog ARINC receivers and no external components are required.

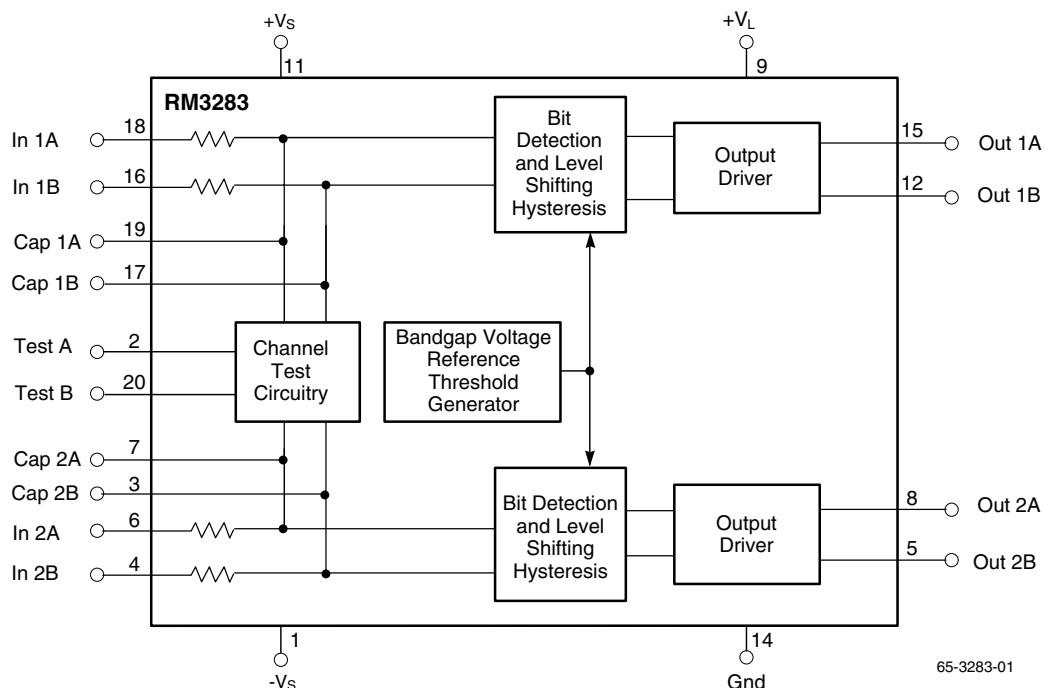
Input level shifting thin film resistors and bipolar technology allow ARINC input voltage transients up to  $\pm 100V$  without damage to the RM3283.

Each channel is identical, featuring symmetrical propagation delays for better high speed performance. Input common mode rejection is excellent and threshold voltage is stable, independent of supply voltage. Data outputs are TTL and CMOS compatible.

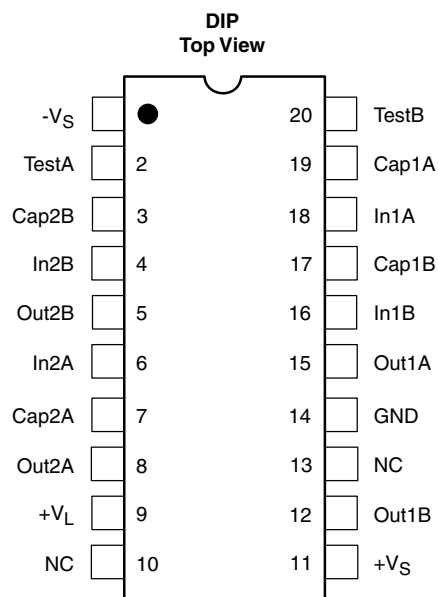
Two TTL compatible test inputs used to test the ARINC channels are available. They can be used to override the ARINC input data and set the channel outputs to a known state.

The Fairchild RM3182A line driver is the companion chip to the RM3283 line receiver. Together they provide the analog functions needed for the ARINC 429 interface. Digital data processing involving serial-to-parallel conversion and clock recovery can be accomplished using one of the ARINC interface IC's available or by an equivalent gate array implementation.

### Block Diagram



## Pin Assignments



65-3283-02

## Functional Description

The RM3283 contains two discrete ARINC 429 receiver channels. Each channel contains three main sections: a resistor input network, a window comparator, and a logic output buffer stage. The first stage provides overvoltage protection and biases the signal using voltage dividers and current sources, providing excellent input common mode rejection. The test inputs are provided to set the outputs to a predetermined state for built-in channel test capability. If the test inputs are not used, they should be grounded.

The window comparator section detects data from the resistor input network. A Logic 1 corresponds to ARINC “High” state (OUTA) and a Logic 0, to ARINC “Low” state (OutB). An ARINC “Null” state at the inputs forces both outputs to Logic 0. Threshold and hysteresis voltages are generated by a bandgap voltage reference to maintain stable switching characteristics over temperature and power supply variations.

The output stage generates a TTL compatible logic output capable of driving 3mA of load.

## Absolute Maximum Ratings

Parameter		Min.	Max.	Units
Supply Voltage (VCC to VEE)			+36	V
VLOGIC Voltage			+7	V
Logic Input Voltage		-0.3	VLOGIC + 0.3	V
Temperature Range	Storage	-65	+150	°C
	Operating	-55	+125	°C
Junction Temperature		-55	+175	°C
Lead Soldering Temperature	60 sec., DIP, LCC		+300	°C
	10 sec., SOIC		+260	°C

## Thermal Characteristics (Still air, soldered on a PC board)

Parameter	DIP
Maximum Junction Temperature	+175°C
Thermal Resistance, $\theta_{JC}$	70°C/W
Thermal Resistance, $\theta_{JC}$	28°C/W <sup>1</sup>

**Note:**

1. MIL-STD-1835.

## DC Electrical Characteristics

$T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $\pm 12\text{V} \leq V_S \leq \pm 15\text{V}$ ,  $V_L = +5\text{V}$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{CC}$ (+ $V_S$ )	Test inputs = 0V			4.3	6.0	mA
$I_{EE}$ (- $V_S$ )	Test inputs = 0V			10.1	12.0	mA
$I_L$ ( $V_L$ )	Test inputs = 5V			14.0	17.5	mA
$V_{TL}$ <sup>2</sup>	V(A)-V(B)	Low threshold	4.7	5.0	5.3	V
$V_{TH}$ <sup>2</sup>	V(A)-V(B)	High threshold	5.7	6.0	6.3	V
$V_{IN}$	V(A)-V(B)	OutA and OutB = 0	-2.5	0	2.5	V
$V_{IC}$ <sup>3</sup>	V(A) and V(B)-GND	Maximum common mode frequency = 80 kHz		±5		V
$R_I$	Input resistance, Input A to Input B		35	50		k $\Omega$
$R_H$	Input resistance, Input A to Gnd		20	25		k $\Omega$
$R_G$	Input resistance, B to Gnd	Filter caps disconnected	20	25		k $\Omega$
$C_I$ <sup>1,4</sup>	Input capacitance, A to B				10	pF
$C_H$ <sup>1,4</sup>	Input capacitance, A to Gnd	Filter caps disconnected			10	pF
$C_G$ <sup>1,4</sup>	Input capacitance, B to Gnd	Filter caps disconnected			10	pF
<b>Test Inputs (TestA, TestB)</b>						
$V_{IH}$ <sup>5</sup>	Logic 1 input voltage		2.7			V
$V_{IL}$ <sup>5</sup>	Logic 0 input voltage		0		0.8	V
$I_{IH}$	Logic 1 input current	$V_{IH} = 5\text{V}$		120	300	$\mu\text{A}$
$I_{IL}$	Logic 0 input current	$V_{IL} = 0.8\text{V}$		15	40	$\mu\text{A}$
<b>Outputs</b>						
$V_{OH}$	$I_{OH} = 100 \mu\text{A}$	$T_A = 25^\circ\text{C}$	4.0	4.3		V
	$I_{OH} = 2.8 \text{ mA}$	Full temperature range	3.5	4.0		V
$V_{OL}$	$I_{OL} = 100 \mu\text{A}$	$T_A = 25^\circ\text{C}$		0.02	0.1	V
	$I_{OL} = 2.0 \text{ mA}$	Full temperature range		0	0.8	V
$T_r$ <sup>6</sup>	Rise Time	$C_L = 50 \text{ pF}$ , @ $25^\circ\text{C}$		50	70	ns
$T_f$ <sup>6</sup>	Fall Time	$C_L = 50 \text{ pF}$ , @ $25^\circ\text{C}$		40	70	ns
$T_{PLH}$	Propagation delay Output low to high	$C_L = 50 \text{ pF}$ , $f = 400 \text{ kHz}$ Filter caps = 39 pF		700		ns
$T_{PHL}$	Output high to low	$T_A = 25^\circ\text{C}$		700		ns

**Notes:**

1. As stated in ARINC429.
2.  $V_T$  refers to the threshold voltage at which the channels output switches from low to high or from high to low.
3. Common mode voltage present at both ARINC inputs.
4. Guaranteed by design.
5. Test inputs should be connected to ground if not used.
6. Sample tested.

### Typical Performance Characteristics

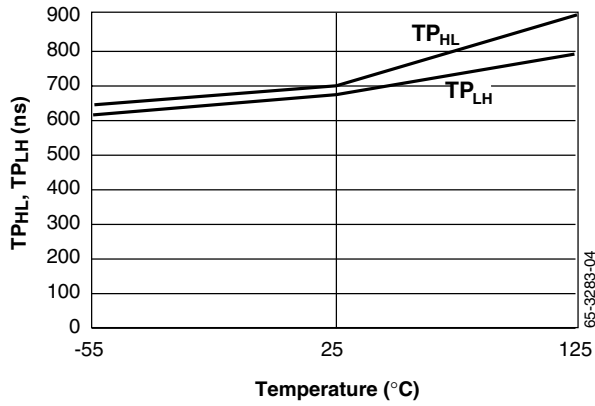


Figure 1. Propagation Delay vs. Temperature  
 $C_L = 50 \text{ pF}$ ,  $C_{FILTER} = 39 \text{ pF}$

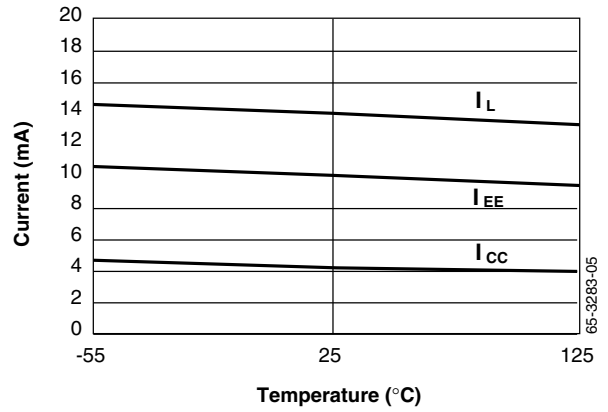


Figure 2. Supply Current vs. Temperature

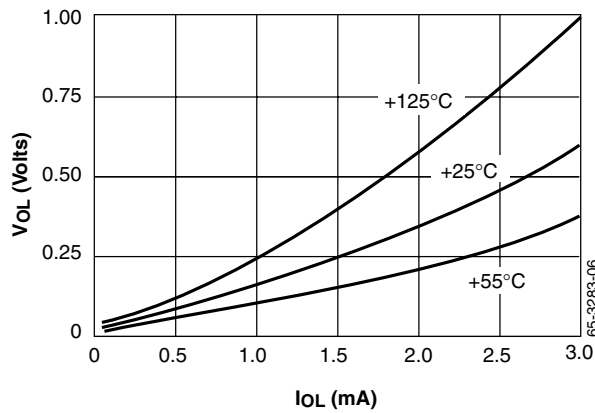


Figure 3. Output Voltage Low vs. Output Current

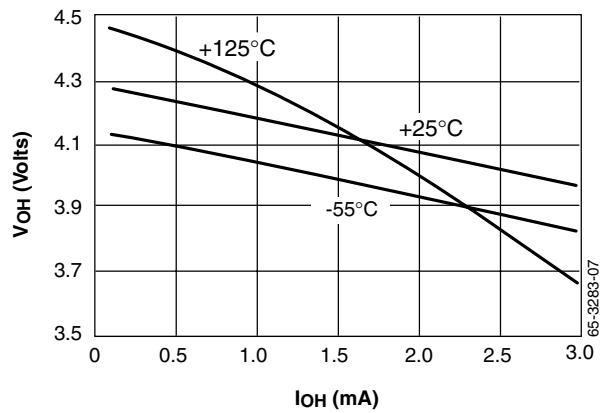


Figure 4. Output Voltage High vs. Output Current

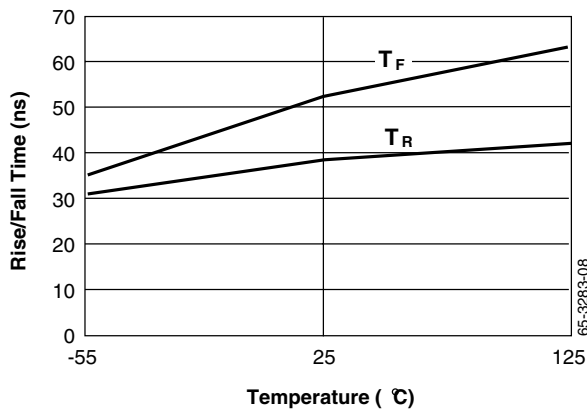


Figure 5.  $T_R$  and  $T_F$  vs. Temperature

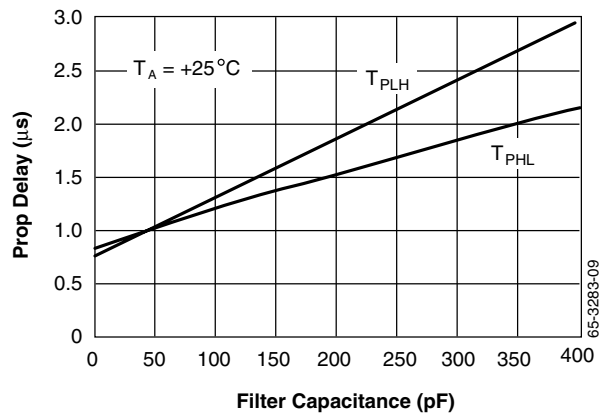


Figure 6. Propagation Delay vs. Filter Capacitance  
 $T_A = 25^\circ\text{C}$

### AC Test Waveforms

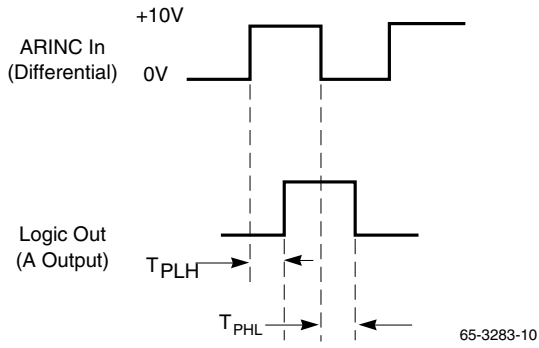


Figure 7. Propagation Delay

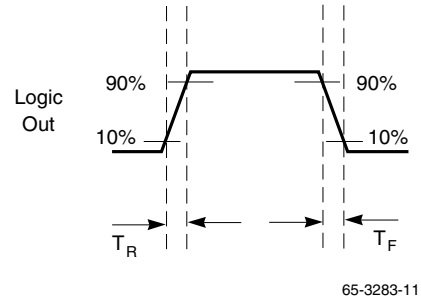
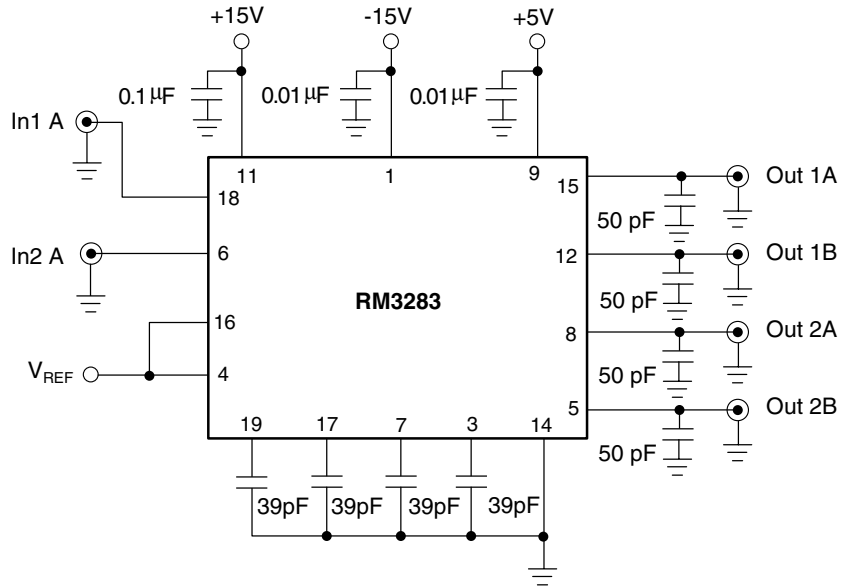


Figure 8. Rise/Fall Times

### Test Circuit



**Notes:**

1.  $V_{IN}$  = 400 kHz square wave, -3.5V to +3.5V.
2. Set  $V_{REF}$  = +3.5 V to test  $V_{OUT1}$  and  $V_{OUT3}$ .  
Set  $V_{REF}$  = -3.5 V to test  $V_{OUT2}$  and  $V_{OUT4}$ .
3. 50 pF load capacitance includes probe and wiring capacitance.

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Figure 9. AC Test Schematic Diagram

## Truth Table

ARINC nputs V(A) - V(B)	Test Inputs		Outputs		Output State
	TESTA	TESTB	OUTA	OUTB	
Null	0	0	0	0	Null
Low	0	0	0	1	Low
High	0	0	1	0	High
X	0	1	0	1	Low
X	1	0	1	0	High
X	1	1	0	0	Null

## Applications Discussion

The standard connections for the RM3283 are shown in Figure 10. Dual supplies from  $\pm 12$  to  $\pm 15$  VDC are recommended for the  $\pm V_S$  supplies. Decoupling of all supplies should be done near the IC to avoid propagation of noise spikes due to switching transients. The ground connection should be sturdy and isolated from large switching currents to provide as quiet a ground reference as possible.

The noise filter capacitors are optional and are added to provide extra noise immunity by limiting bandwidth of the input signal before it reaches the window comparator stage. Two capacitors are required for each channel and they must all be the same value. The suggested capacitor value for a 100 kHz operation is 39 pF. For lower data rates, larger values of capacitance may be used to yield better node perfor-

mance. To get optimum performance, the following equation can be used to calculate capacitor value for a specific data rate:

$$C_{\text{FILTER}} = \frac{3.95 \times 10^{-6}}{F_O}$$

Where  $C_{\text{FILTER}}$  is the capacitor value in pF, and  $F_O$  is the input frequency ( $10 \text{ kHz} \leq F_O \leq 150 \text{ kHz}$ ).

The RM3283 can be used with the Fairchild RM3182A line driver to provide a complete analog ARINC 429 interface. A simple application which can be used for systems requiring a repeater-type circuit for long transmissions is given in Figure 11. More RM3182A drivers may be added to test multiple ARINC channels, as shown.

# Applications

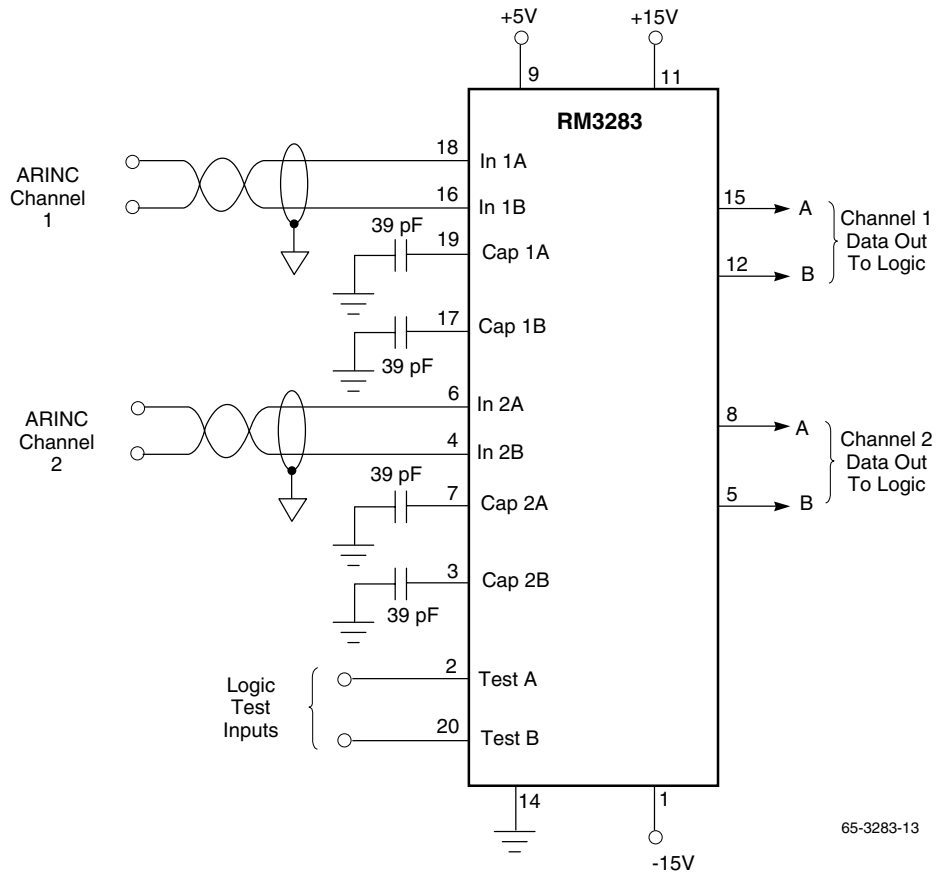


Figure 10. ARINC Receiver Standard Connections

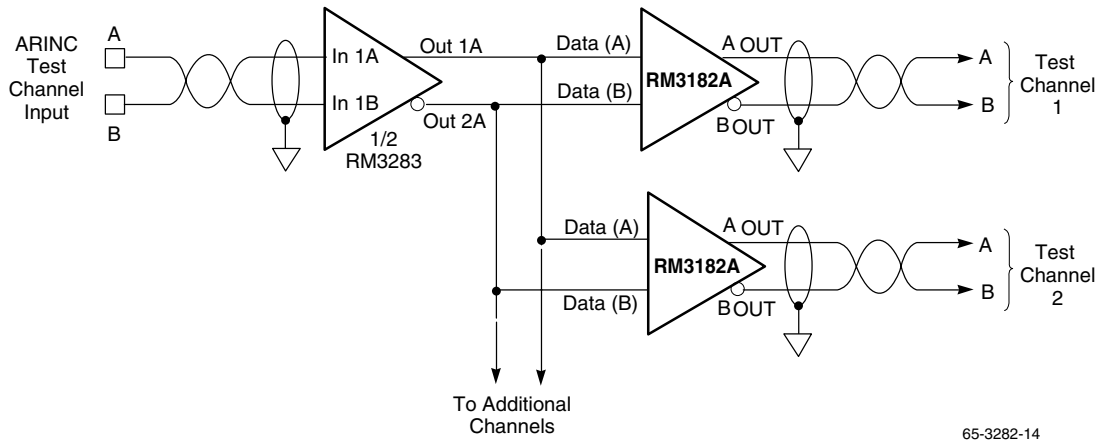


Figure 11. Repeater Circuit

Applications (continued)

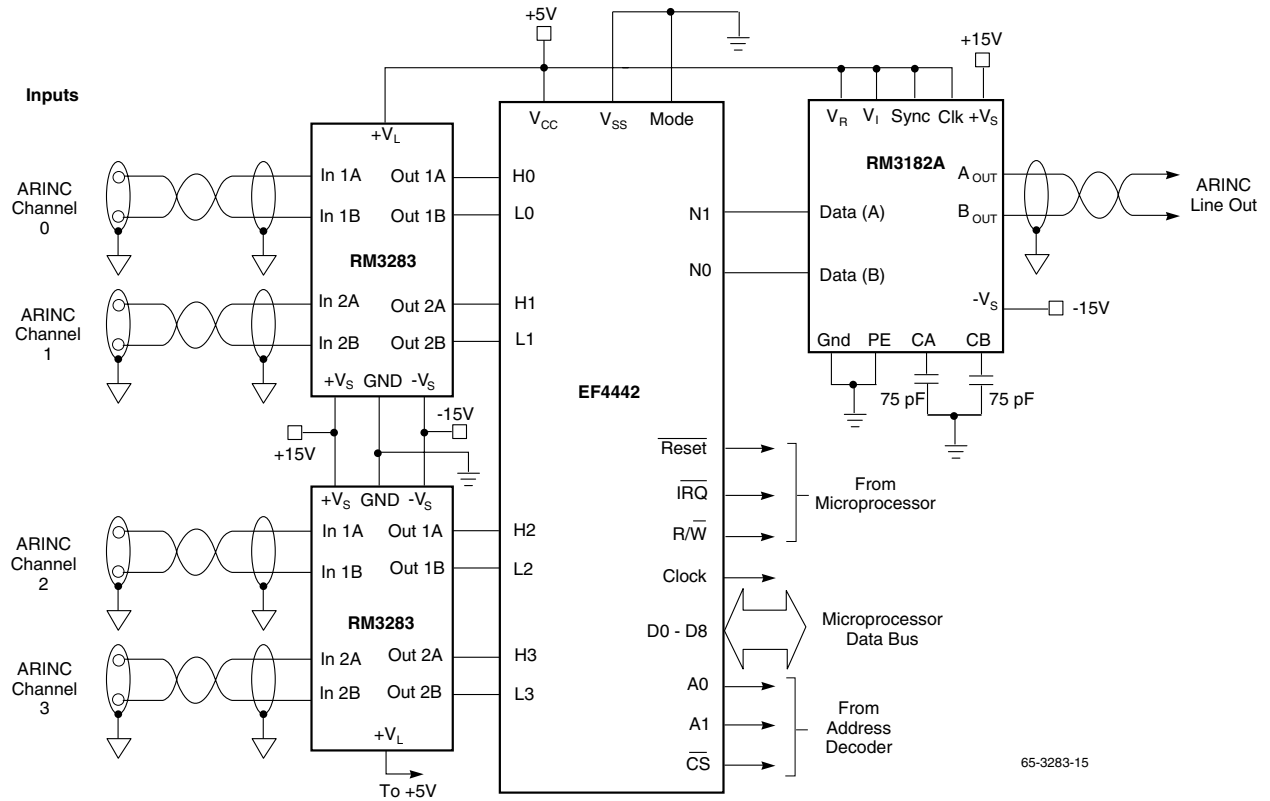


Figure 12. Four-Channel ARINC Receiver Circuit

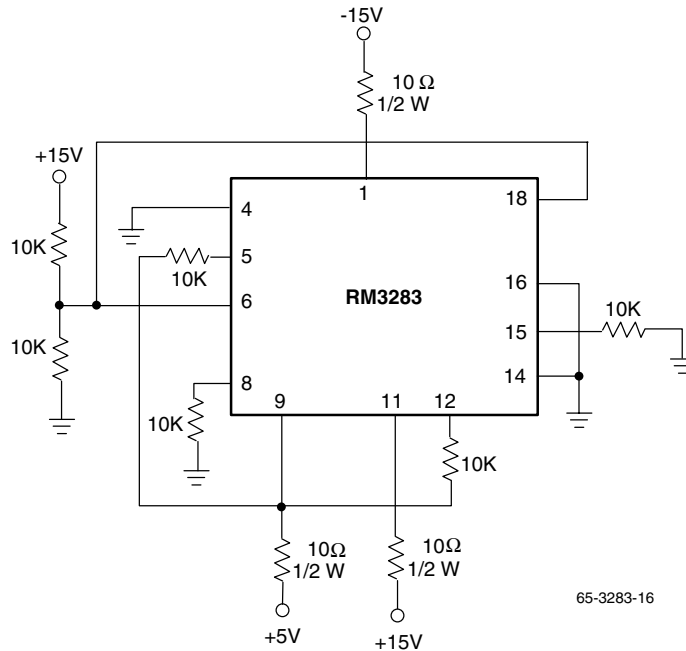


Figure 13. Burn-In Circuit



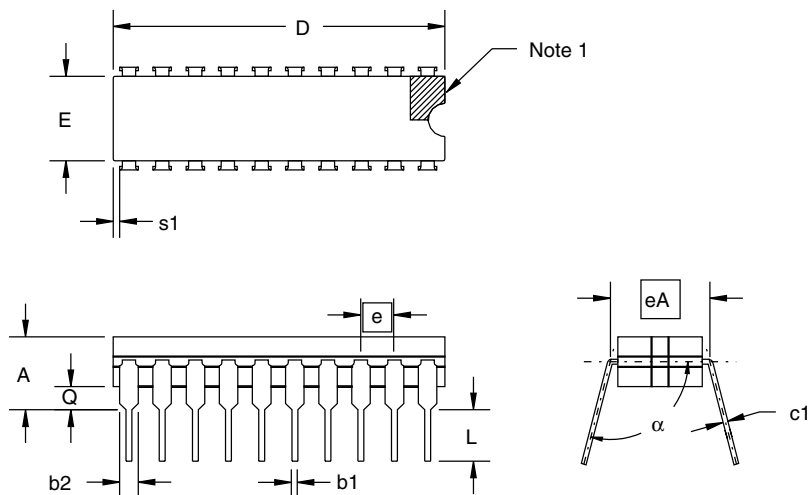
# Mechanical Dimensions

## 20-Lead Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.060	—	25.92	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
$\alpha$	90°	105°	90°	105°	

**Notes:**

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023(.58mm) for leads number 1, 10, 11 and 20 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within  $\pm .010$  (.25mm) of its exact longitudinal position relative to pins 1 and 20.
6. Applies to all four corner's (leads number 1, 10, 11, and 20).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when " $\alpha$ " is 90°.
8. All leads – Increase maximum limit by .003(.08mm) measured at the center of the flat, when lead finish is applied.
9. Eighteen spaces.



## Ordering Information

Part Number	Package	Operating Temperature Range
RM3283D	20 Lead Ceramic DIP	-55°C to +125°C

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