DATA SHEET

BUW12F; BUW12AF
Silicon diffused power transistors

Product specification
Supersedes data of February 1996
File under Discrete Semiconductors, SC06

1997 Aug 14

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Silicon diffused power transistors BUW12F; BUW12AF

DESCRIPTION

High-voltage, high-speed, glass-passivated NPN power transistor in a SOT199 package.

APPLICATIONS

- Converters
- Inverters
- Switching regulators
- Motor control systems.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter
mb	mounting base; electrically isolated

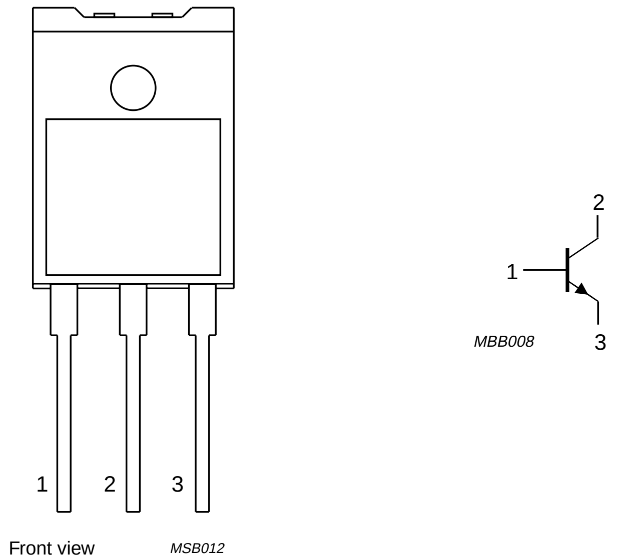


Fig.1 Simplified outline (SOT199) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0$		
	BUW12F		850	V
	BUW12AF		1000	V
V_{CEO}	collector-emitter voltage	open base		
	BUW12F		400	V
	BUW12AF		450	V
V_{CEsat}	collector-emitter saturation voltage	see Figs 6 and 10	1.5	V
I_{Csat}	collector saturation current			
	BUW12F		6	A
	BUW12AF		5	A
I_C	collector current (DC)	see Figs 2 and 5	8	A
I_{CM}	collector current (peak value)	see Fig 2	20	A
P_{tot}	total power dissipation	$T_h \leq 25$ °C; see Fig.4	34	W
t_f	fall time	resistive load; see Figs 12 and 13	0.8	µs

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to external heatsink	note 1	3.7	K/W
		note 2	2.8	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient		35	K/W

Notes

1. Mounted **without** heatsink compound and 30 ±5 N force on centre of package.
2. Mounted **with** heatsink compound and 30 ±5 N force on centre of package.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0			
	BUW12F		–	850	V
	BUW12AF		–	1000	V
V_{CEO}	collector-emitter voltage	open base			
	BUW12F		–	400	V
	BUW12AF		–	450	V
I_{Csat}	collector saturation current	V_{CE} = 1.5 V			
	BUW12F		–	6	A
	BUW12AF		–	5	A
I_C	collector current (DC)	see Figs 2 and 5	–	8	A
I_{CM}	collector current (peak value)	see Fig 2	–	20	A
I_B	base current (DC)		–	4	A
I_{BM}	base current (peak value)		–	6	A
P_{tot}	total power dissipation	$T_h \leq 25$ °C; see Fig.4; note 1	–	34	W
		$T_h \leq 25$ °C; see Fig.4; note 2	–	45	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

Notes

1. Mounted **without** heatsink compound and 30 ±5 N force on centre of package.
2. Mounted **with** heatsink compound and 30 ±5 N force on centre of package.

ISOLATION CHARACTERISTICS

SYMBOL	PARAMETER	MAX.	UNIT
V_{isolM}	isolation voltage from all terminals to external heatsink (peak value)	1500	V
C_{isol}	isolation capacitance from collector to external heatsink	21	pF

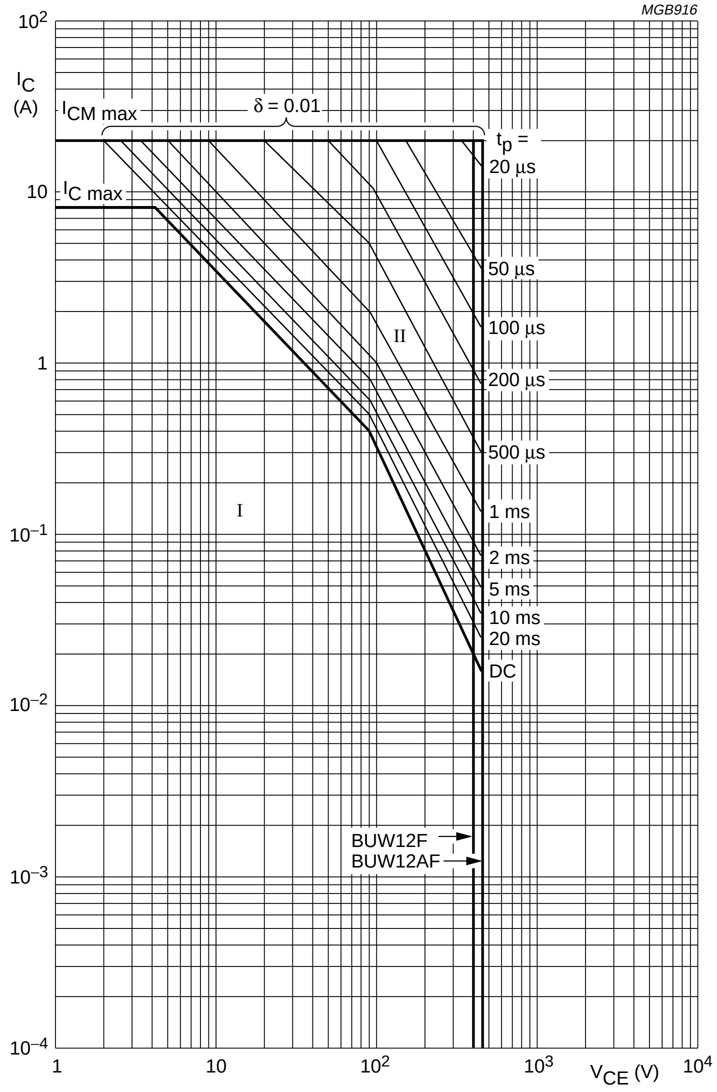
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CEOsust}$	collector-emitter sustaining voltage	I_C = 100 mA; I_{Boff} = 0; L = 25 mH; see Figs 8 and 9				
	BUW12F		400	–	–	V
	BUW12AF		450	–	–	V
V_{CEsat}	collector-emitter saturation voltage					
	BUW12F	I_C = 6 A; I_B = 1.2 A; see Figs 6 and 10	–	–	1.5	V
	BUW12AF	I_C = 5 A; I_B = 1 A; see Figs 6 and 10	–	–	1.5	V
V_{BEsat}	base-emitter saturation voltage					
	BUW12F	I_C = 6 A; I_B = 1.2 A; see Fig.6	–	–	1.5	V
	BUW12AF	I_C = 5 A; I_B = 1 A; see Fig.6	–	–	1.5	V
I_{CES}	collector-emitter cut-off current	$V_{CE} = V_{CESMmax}$; V_{BE} = 0; note 1	–	–	1	mA
		$V_{CE} = V_{CESMmax}$; V_{BE} = 0; T_j = 125 °C; note 1	–	–	3	mA
I_{EBO}	emitter-base cut-off current	V_{EB} = 9 V; I_C = 0	–	–	10	mA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 10 mA; see Fig.11	10	18	35	
		V_{CE} = 5 V; I_C = 1 A; see Fig.11	10	20	35	
Switching times resistive load (see Figs 12 and 13)						
t_{on}	turn-on time					
	BUW12F	I_{Con} = 6 A; $I_{Bon} = I_{Boff}$ = 1.2 A	–	–	1	µs
	BUW12AF	I_{Con} = 5 A; $I_{Bon} = I_{Boff}$ = 1 A	–	–	1	µs
t_s	storage time					
	BUW12F	I_{Con} = 6 A; $I_{Bon} = I_{Boff}$ = 1.2 A	–	–	4	µs
	BUW12AF	I_{Con} = 5 A; $I_{Bon} = I_{Boff}$ = 1 A	–	–	4	µs
t_f	fall time					
	BUW12F	I_{Con} = 6 A; $I_{Bon} = I_{Boff}$ = 1.2 A	–	–	0.8	µs
	BUW12AF	I_{Con} = 5 A; $I_{Bon} = I_{Boff}$ = 1 A	–	–	0.8	µs
Switching times inductive load (see Figs 14 and 15)						
t_s	storage time					
	BUW12F	I_{Con} = 6 A; I_B = 1.2 A; V_{CL} = 250 V; T_c = 100 °C	–	1.9	2.5	µs
	BUW12AF	I_{Con} = 5 A; I_B = 1 A; V_{CL} = 300 V; T_c = 100 °C	–	1.9	2.5	µs
t_f	fall time					
	BUW12F	I_{Con} = 6 A; I_B = 1.2 A; V_{CL} = 250 V; T_c = 100 °C	–	200	300	ns
	BUW12AF	I_{Con} = 5 A; I_B = 1 A; V_{CL} = 300 V; T_c = 100 °C	–	200	300	ns

Note

1. Measured with a half-sinewave voltage (curve tracer).



Mounted **without** heatsink compound and 30 ±5 N force on centre of package.

T_{mb} < 25 °C.

I - Region of permissible DC operation.

II - Permissible extension for repetitive pulse operation.

Fig.2 Forward bias SOAR.

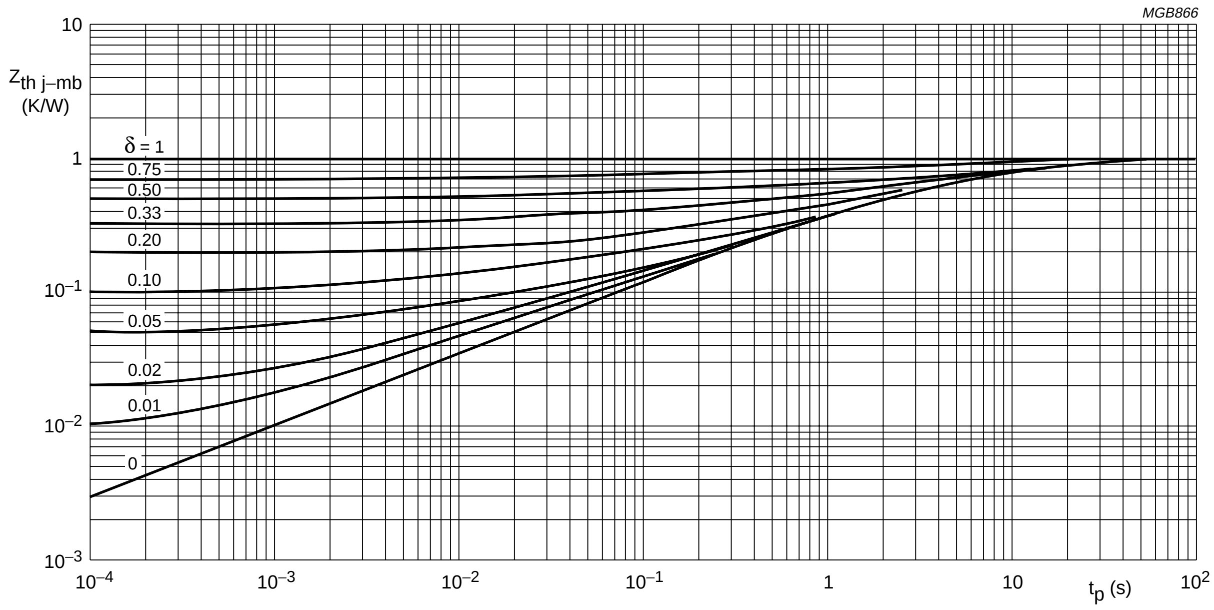


Fig.3 Transient thermal impedance.

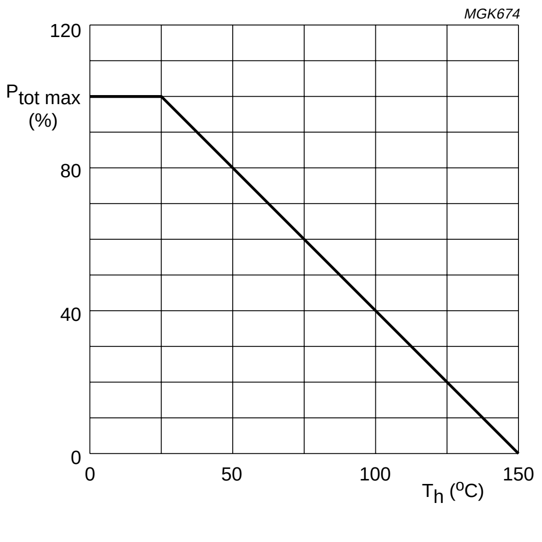
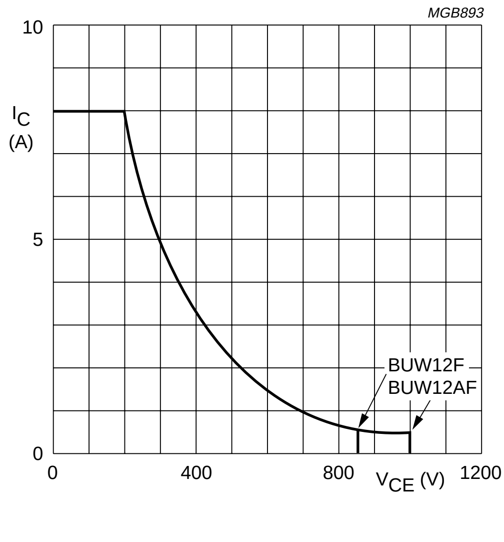
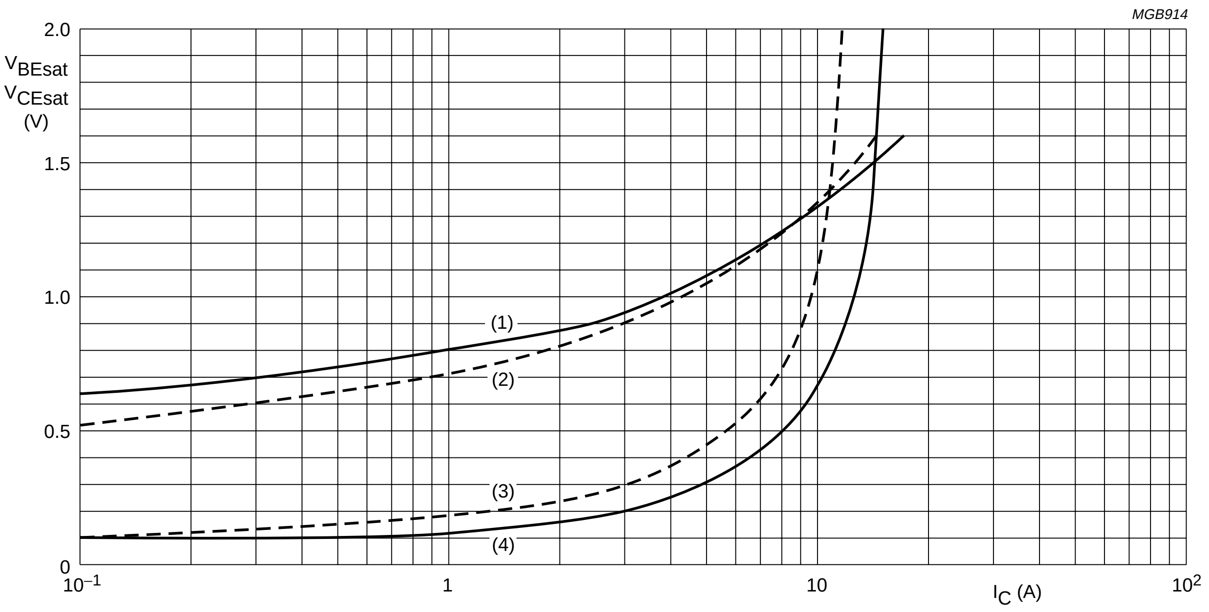


Fig.4 Power derating curve.



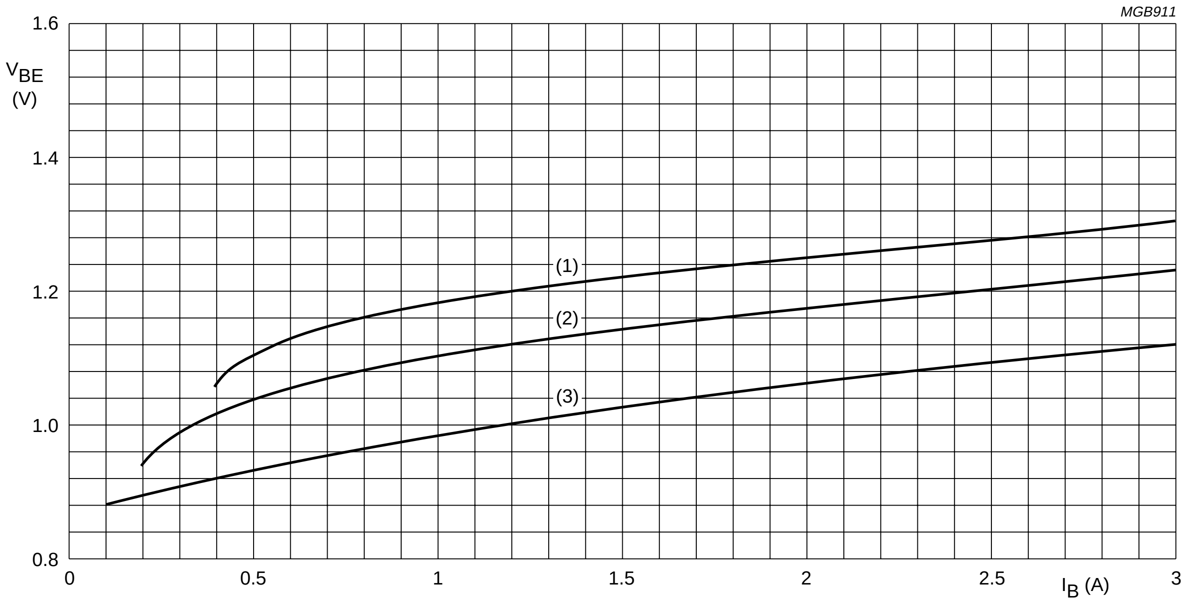
$T_c \leq 100$ °C; V_{BE} = –1 to –5 V.

Fig.5 Reverse bias SOAR.



$I_C/I_B = 5$.
(1) V_{BE}; T_j = 25 °C.
(2) V_{BE}; T_j = 100 °C.
(3) V_{CE}; T_j = 100 °C.
(4) V_{CE}; T_j = 25 °C.

Fig.6 Base-emitter and collector-emitter saturation voltages as functions of collector current; typical values.



T_j = 25 °C.
(1) I_C = 8 A.
(2) I_C = 6 A.
(3) I_C = 3 A.

Fig.7 Base-emitter voltage as a function of base current; typical values.

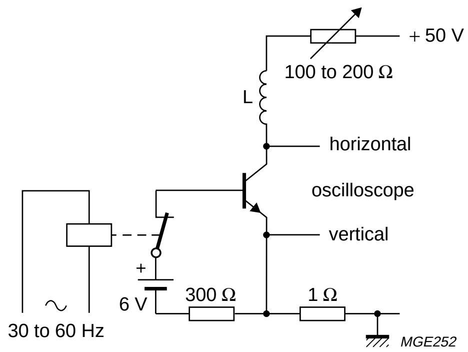


Fig.8 Test circuit for collector-emitter sustaining voltage.

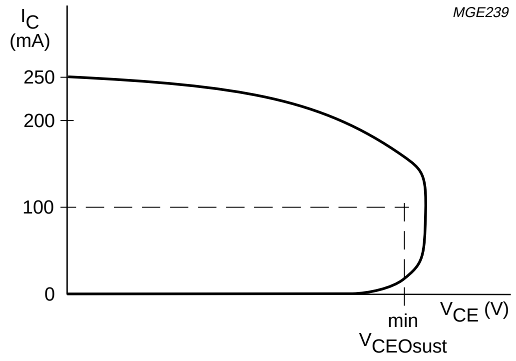
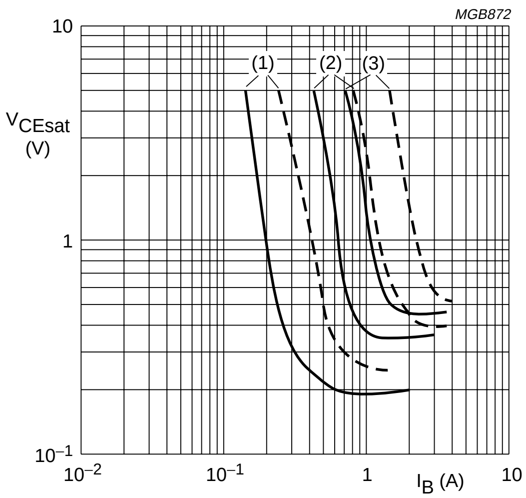
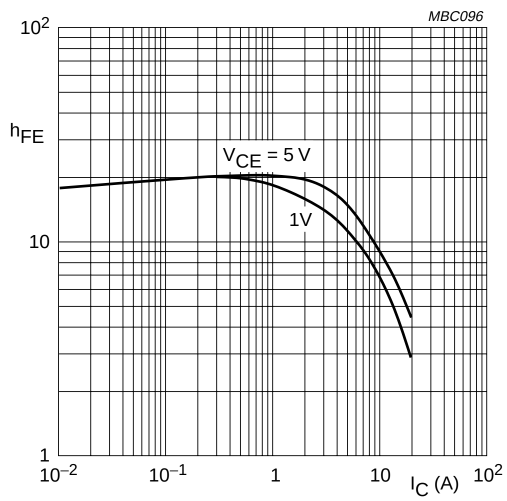


Fig.9 Oscilloscope display for collector-emitter sustaining voltage.



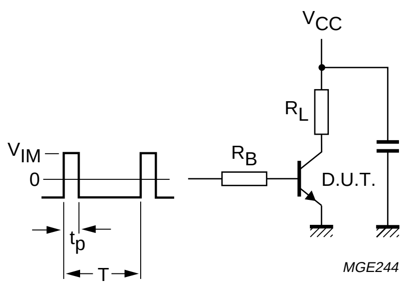
T_j = 25 °C.
(1) I_C = 3 A.
(2) I_C = 6 A.
(3) I_C = 8 A.

Fig.10 Collector-emitter saturation voltage as a function of base current.



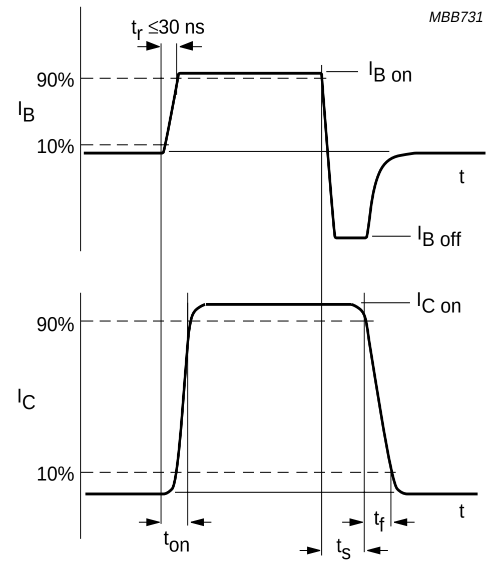
T_j = 125 °C.

Fig.11 DC current gain; typical values.



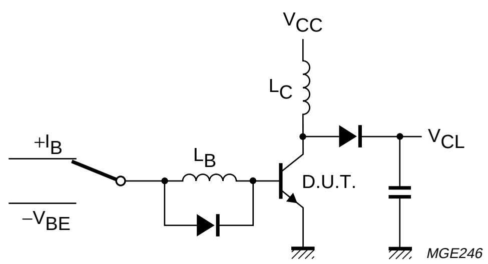
V_{CC} = 250 V; t_p = 20 µs; V_{IM} = –6 to +8 V; t_p/T = 0.01.
The values of R_B and R_L are selected in accordance with I_{Con} and I_{Bon} requirements.

Fig.12 Test circuit resistive load.



t_r ≤ 20 ns.

Fig.13 Switching time waveforms with resistive load.



V_{CL} = up to 1000 V; V_{CC} = 30 V; V_{BE} = –1 V to –5 V; L_B = 1 µH; L_C = 200 µH.

Fig.14 Test circuit inductive load and reverse bias SOAR.

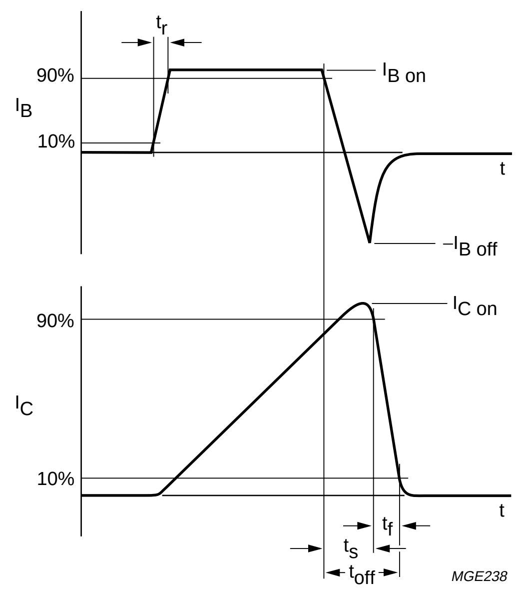
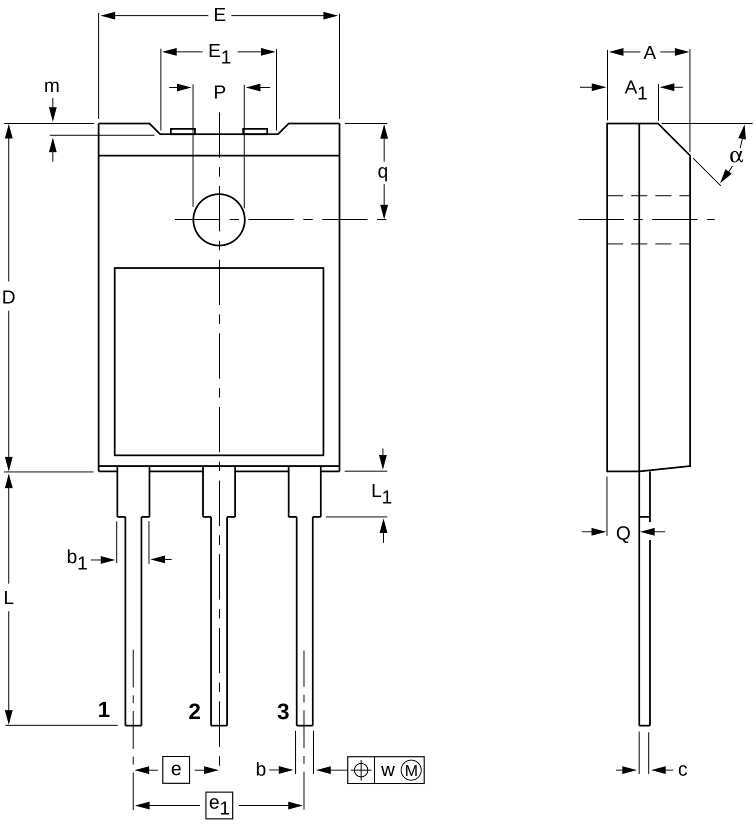


Fig.15 Switching time waveforms with inductive load.

PACKAGE OUTLINE

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads (in-line) **SOT199**

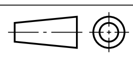


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	E	E_1	e	e_1	L	L_1(1)	m	P	Q	q	w	α
mm	5.2 4.8	3.4 3.0	1.2 1.0	2.1 1.9	0.6 0.5	21.5 20.5	15.3 14.7	7.8 6.8	5.45	10.9	16.5 15.7	3.7 3.3	0.8 0.6	3.3 3.1	2.1 1.9	6.2 5.8	0.4	45°

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT199						97-06-27

Silicon diffused power transistors BUW12F; BUW12AF

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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