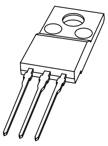


PHE13005X

Silicon diffused power transistor

Rev. 01 — 15 May 2008 **Product data sheet**

1. Product profile

1.1 General description

High voltage, high speed, planar passivated NPN power switching transistor in a full pack plastic package.

1.2 Features

- Low thermal resistance
- Isolated package
- Fast switching

1.3 Applications

- Electronic lighting ballasts
- Inverters
- DC-to-DC converters
- Motor control systems

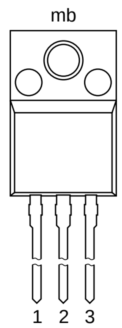
1.4 Quick reference data

- $V_{CESM} \leq 700$ V; $V_{BE} = 0$ V
- $P_{tot} \leq 26$ W; $T_h \leq 25$ °C
- $I_C \leq 4$ A; DC
- $h_{FE} = 17$ (typical); $I_C = 2$ A; $V_{CE} = 5$ V

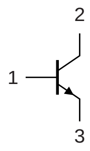
2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	base		
2	collector		
3	emitter		
mb	isolated		



SOT186A (TO-220F)



3. Ordering information

Table 2. Ordering information

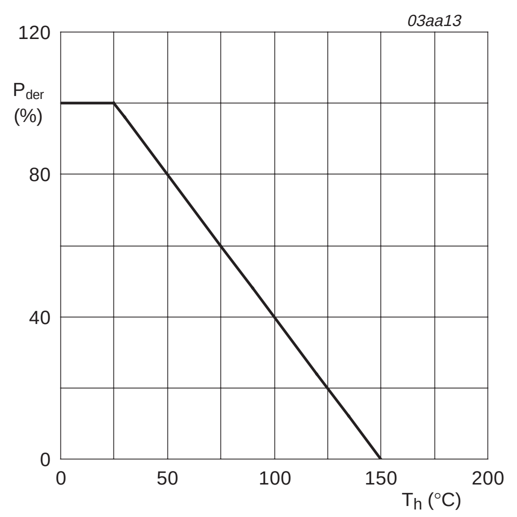
Type number	Package		
	Name	Description	Version
PHE13005X	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 'full pack'	SOT186A

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V	-	700	V
V_{CBO}	collector-base voltage	open emitter	-	700	V
V_{CEO}	collector-emitter voltage	open base	-	400	V
I_C	collector current	DC	-	4	A
I_{CM}	peak collector current		-	8	A
I_B	base current	DC	-	2	A
I_{BM}	peak base current		-	4	A
P_{tot}	total power dissipation	$T_h \leq 25$ °C; see Figure 1	-	26	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	150	°C



With heatsink compound

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig 1. Normalized total power dissipation as a function of heatsink temperature

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; see Figure 2	-	-	4.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W

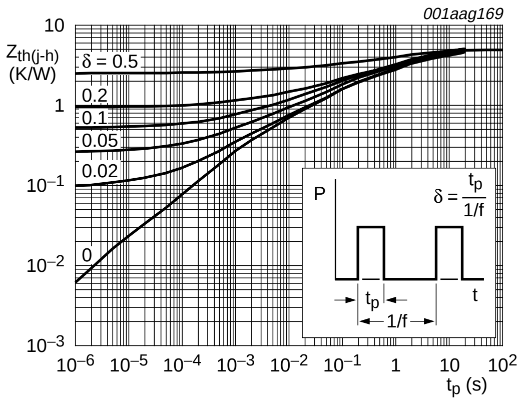


Fig 2. Transient thermal impedance from junction to heatsink as a function of pulse duration

6. Isolation characteristics

Table 5. Isolation limiting values and characteristics

T_h = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all three terminals to external heatsink; f = 50 Hz to 60 Hz; sinusoidal waveform; relative humidity ≤ 65 %; clean and dust free	-	-	2500	V
C_{isol}	isolation capacitance	from pin 2 to external heatsink; f = 1 MHz	-	10	-	pF

7. Characteristics

Table 6. Characteristics

T_{mb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{CES}	collector-emitter cut-off current	V_{BE} = 0 V; V_{CE} = V_{CESM}	[1]	-	-	1	mA
		V_{BE} = 0 V; V_{CE} = V_{CESM}; T_j = 100 °C	[1]	-	-	5	mA
I_{CBO}	collector-base cut-off current	V_{BE} = 0 V; V_{CE} = V_{CESM}	[1]	-	-	1	mA
I_{CEO}	collector-emitter cut-off current	V_{CEO} = $V_{CEO(max)}$ = 400 V	[1]	-	-	0.1	mA
I_{EBO}	emitter-base cut-off current	V_{EB} = 9 V; I_C = 0 A		-	-	1	mA
V_{CEOsus}	collector-emitter sustaining voltage	I_B = 0 A; I_C = 10 mA; L_C = 25 mH; see Figure 3 and 4		400	-	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 1 A; I_B = 0.2 A; see Figure 10		-	0.1	0.5	V
		I_C = 2 A; I_B = 0.5 A; see Figure 10 and 12		-	0.2	0.6	V
		I_C = 4 A; I_B = 1 A; see Figure 10 and 12		-	0.3	1	V
V_{BEsat}	base-emitter saturation voltage	I_C = 1 A; I_B = 0.2 A		-	0.85	1.2	V
		I_C = 2 A; I_B = 0.5 A; see Figure 11		-	0.92	1.6	V
h_{FE}	DC current gain	I_C = 1 A; V_{CE} = 5 V; see Figure 9		10	20	60	
		I_C = 2 A; V_{CE} = 5 V; see Figure 9		8	17	40	
Dynamic characteristics							
t_s	storage time	Resistive load; I_{Con} = 2 A; I_{Bon} = –I_{Boff} = 0.4 A; R_L = 75 Ω; V_{CC} = 250 V; see Figure 5 and 6		-	2.7	4	µs
		Inductive load; I_{Con} = 2 A; L_B = 1 µH; V_{BE} = –5 V; see Figure 7 and 8					
		I_{Bon} = 0.4 A		-	1.2	2	µs
		I_{Bon} = 0.4 A; T_j = 100 °C		-	1.4	4	µs
t_f	fall time	Resistive load; I_{Con} = 2 A; I_{Bon} = –I_{Boff} = 0.4 A; R_L = 75 Ω; V_{CC} = 250 V; see Figure 5 and 6		-	0.3	0.9	µs
		Inductive load; I_{Con} = 2 A; L_B = 1 µH; V_{BE} = –5 V; I_{Bon} = 0.4 A; see Figure 7 and 8					
		I_{Bon} = 0.4 A		-	0.1	0.5	µs
		I_{Bon} = 0.4 A; T_j = 100 °C		-	0.16	0.9	µs

[1] Measured with half sine-wave voltage (curve tracer).

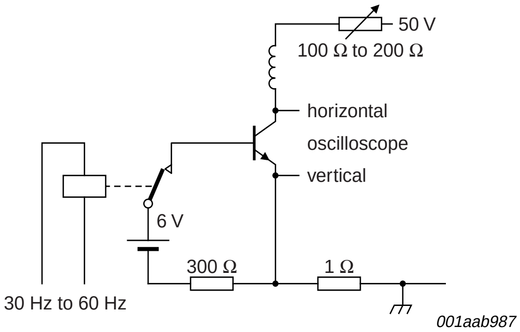


Fig 3. Test circuit for collector-emitter sustaining voltage

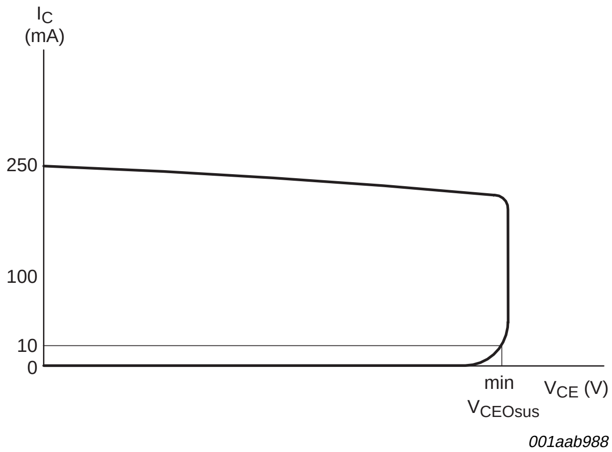
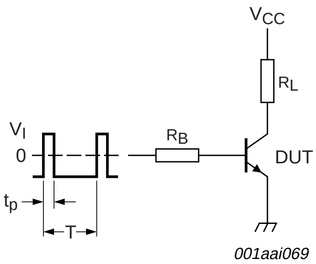


Fig 4. Oscilloscope display for collector-emitter sustaining voltage test waveform



V_I = –6 V to +8 V; V_{CC} = 250 V; t_p = 20 µs;

$\delta = t_p / T = 0.01$.

R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig 5. Test circuit for resistive load switching

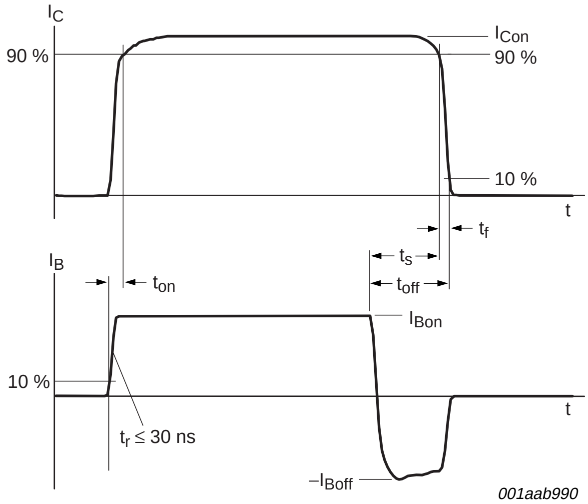
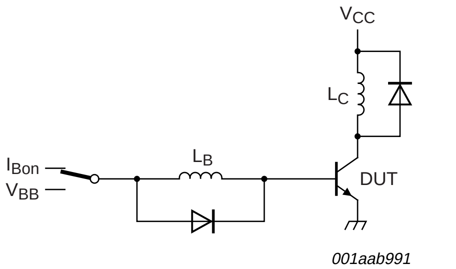


Fig 6. Switching times definitions for resistive load



V_{CC} = 300 V; V_{BB} = –5 V; L_C = 200 µH; L_B = 1 µH

Fig 7. Test circuit for inductive load switching

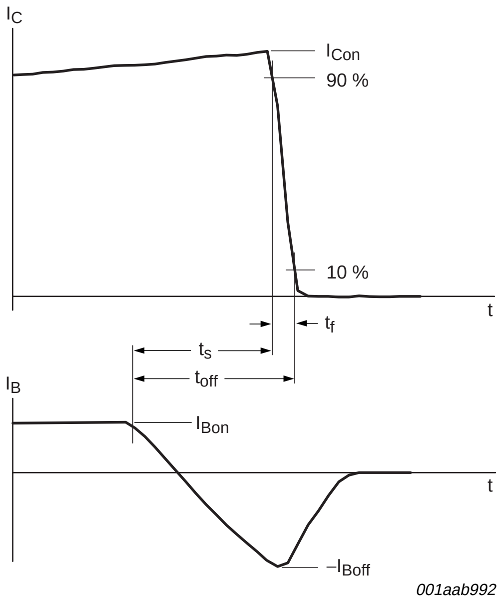
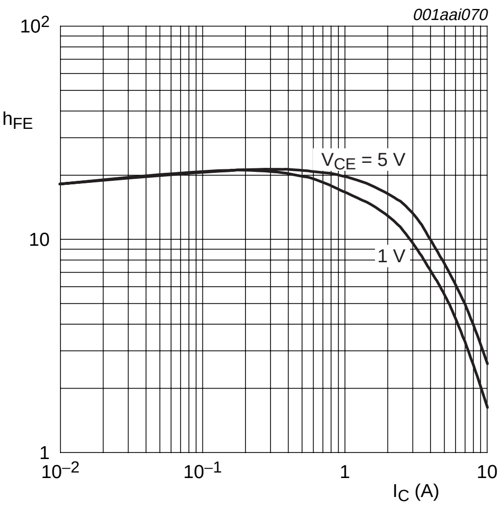
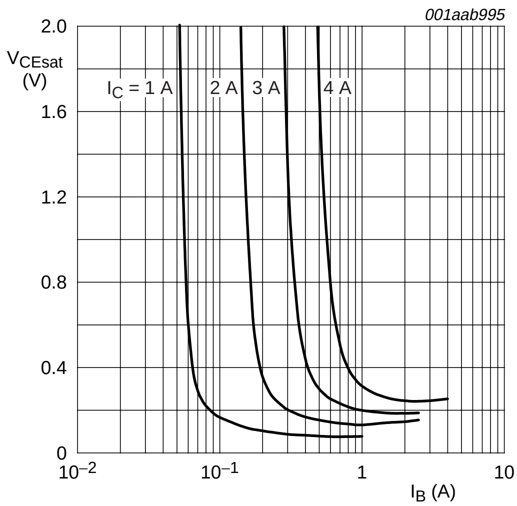


Fig 8. Switching times definitions for inductive load



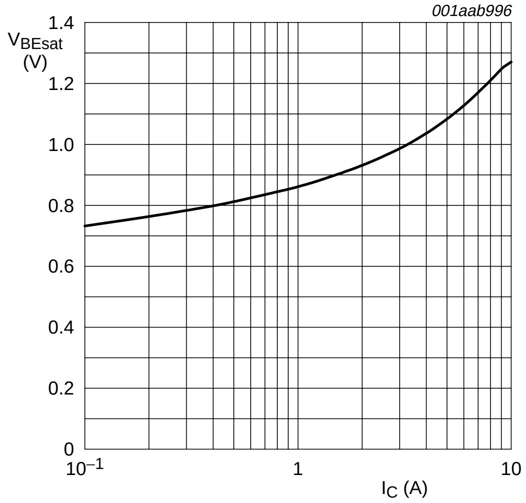
T_j = 25 °C

Fig 9. DC current gain as a function of collector current; typical values



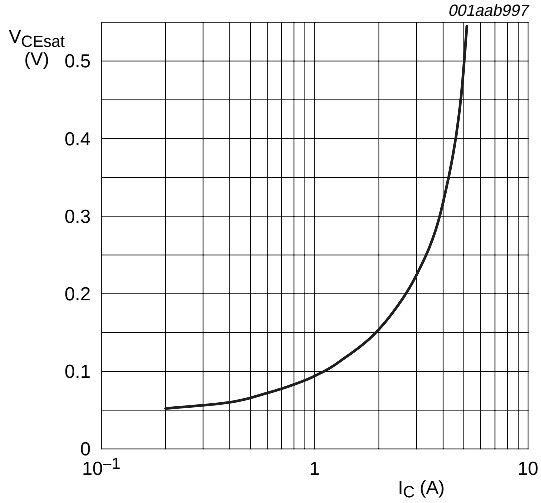
T_j = 25 °C

Fig 10. Collector-emitter saturation voltage; typical values



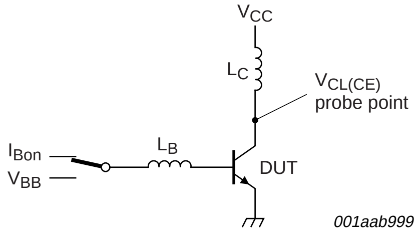
$I_C/I_B = 4$

Fig 11. Base-emitter saturation voltage; typical values



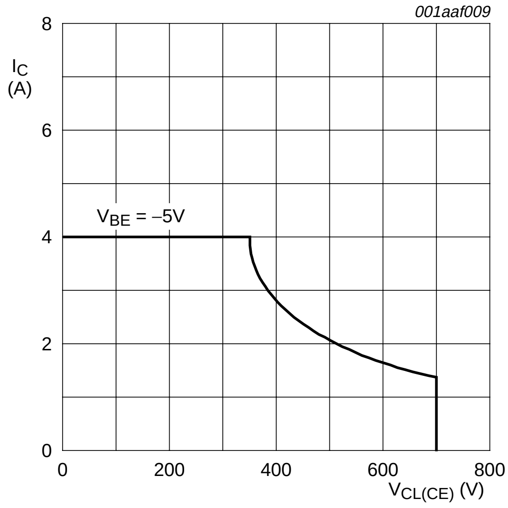
$I_C/I_B = 4$

Fig 12. Collector-emitter saturation voltage as a function of collector current; typical values



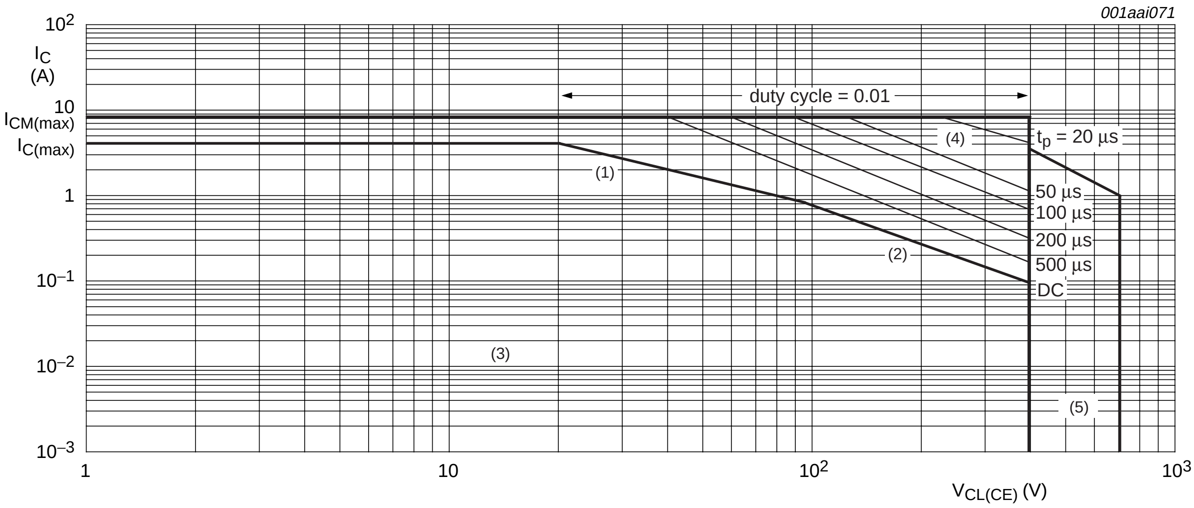
$V_{CL(CE)} \leq 1000$ V; $V_{CC} = 150$ V; $V_{BB} = -5$ V;
$L_B = 1$ µH; $L_C = 200$ µH

Fig 13. Test circuit for reverse bias safe operating area



$T_j \leq T_{j(max)}$

Fig 14. Reverse bias safe operating area



$T_h \leq 25$ °C.

Mounted with heatsink compound and (30 ± 5) N force on the center of the envelope.

(1) P_{tot} maximum and P_{tot} peak maximum lines.

(2) Second breakdown limits.

(3) Region of permissible DC operation.

(4) Extension of operating region for repetitive pulse operation.

(5) Extension of operating region during turn-on in single transistor converters provided that $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0.6$ µs.

Fig 15. Forward bias safe operating area

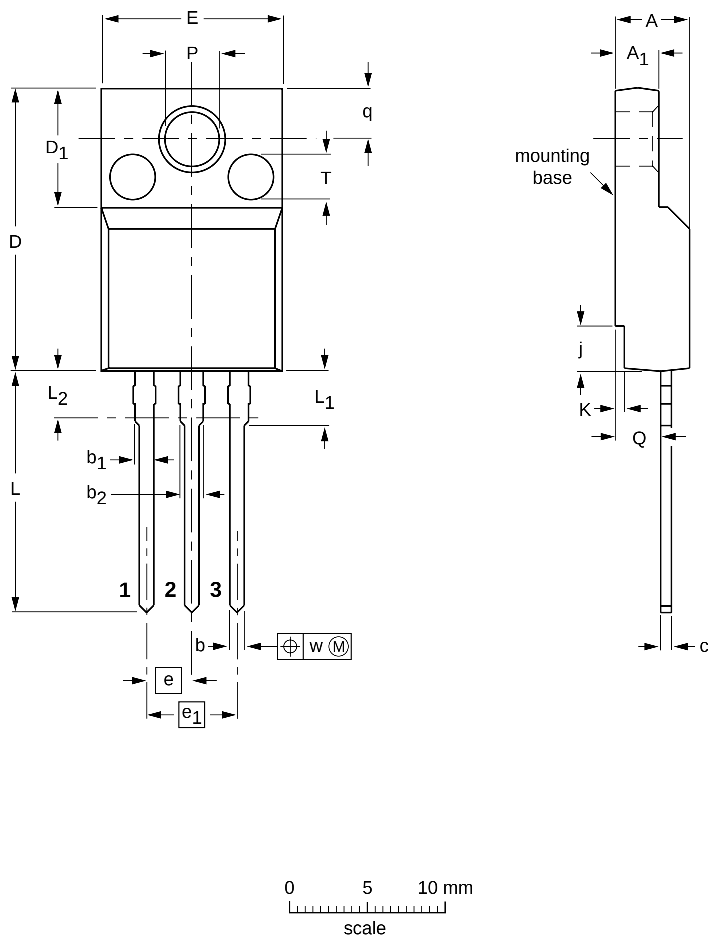
8. Package information

Epoxy meets requirements of UL94 V-0 at 3.175 mm.

9. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	$L_2^{(1)}$ max.	P	Q	q	$T^{(2)}$	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

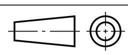
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				~~02-04-09~~ 06-02-14

Fig 16. Package outline SOT186A (3-lead TO-220F)

10. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHE13005X_1	20080515	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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13. Contents

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