

# NSS12200LT1G

## 12 V, 4.0 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's e<sup>2</sup>PowerEdge family of low  $V_{CE(sat)}$  transistors are miniature surface mount devices featuring ultra low saturation voltage ( $V_{CE(sat)}$ ) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e<sup>2</sup>PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

- This is a Pb-Free Device

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	-12	Vdc
Collector-Base Voltage	$V_{CBO}$	-12	Vdc
Emitter-Base Voltage	$V_{EBO}$	-7.0	Vdc
Collector Current - Continuous	$I_C$	-2.0	A
Collector Current - Peak	$I_{CM}$	-4.0	A
Electrostatic Discharge	ESD	HBM Class 3B MM Class C	

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$ (Note 1)	460	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 1)	270	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$ (Note 2)	540	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 2)	230	$^\circ\text{C}/\text{W}$
Total Device Dissipation (Single Pulse < 10 sec.)	$P_{D\text{single}}$ (Note 3)	710	mW
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

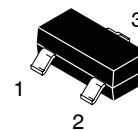
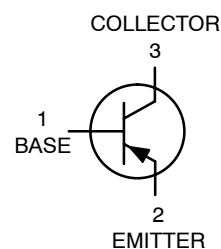
1. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces.
2. FR-4 @ 500 mm<sup>2</sup>, 1 oz. copper traces.
3. Thermal response.



ON Semiconductor®

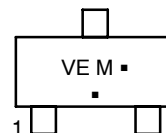
<http://onsemi.com>

**-12 VOLTS**  
**4.0 AMPS**  
**PNP LOW  $V_{CE(sat)}$  TRANSISTOR**  
**EQUIVALENT  $R_{DS(on)}$  65 mΩ**



SOT-23 (TO-236)  
CASE 318  
STYLE 6

### DEVICE MARKING



VE = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or overbar may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NSS12200LT1G	SOT-23 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NSS12200LT1G

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Collector – Emitter Breakdown Voltage (I <sub>C</sub> = -10 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	-12	-	-	Vdc
Collector – Base Breakdown Voltage (I <sub>C</sub> = -0.1 mA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	-12	-	-	Vdc
Emitter – Base Breakdown Voltage (I <sub>E</sub> = -0.1 mA, I <sub>C</sub> = 0)	V <sub>(BR)EBO</sub>	-7.0	-	-	Vdc
Collector Cutoff Current (V <sub>CB</sub> = -12 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	-	-	-0.1	μAdc
Emitter Cutoff Current (V <sub>EB</sub> = -7.0 Vdc)	I <sub>EBO</sub>	-	-	-0.1	μAdc

### ON CHARACTERISTICS

DC Current Gain (Note 4) (I <sub>C</sub> = -10 mA, V <sub>CE</sub> = -2.0 V) (I <sub>C</sub> = -500 mA, V <sub>CE</sub> = -2.0 V) (I <sub>C</sub> = -1.0 A, V <sub>CE</sub> = -2.0 V) (I <sub>C</sub> = -2.0 A, V <sub>CE</sub> = -2.0 V)	h <sub>FE</sub>	250 250 200 150	- 300 - -	- - - -	
Collector – Emitter Saturation Voltage (Note 4) (I <sub>C</sub> = -0.1 A, I <sub>B</sub> = -0.010 A) (Note 5) (I <sub>C</sub> = -1.0 A, I <sub>B</sub> = -0.100 A) (I <sub>C</sub> = -1.0 A, I <sub>B</sub> = -0.010 A) (I <sub>C</sub> = -2.0 A, I <sub>B</sub> = -0.200 A)	V <sub>CE(sat)</sub>	- - - -	-0.008 -0.065 -0.100 -0.130	-0.011 -0.090 -0.120 -0.180	V
Base – Emitter Saturation Voltage (Note 4) (I <sub>C</sub> = -1.0 A, I <sub>B</sub> = -0.01 A)	V <sub>BE(sat)</sub>	-	-	-0.900	V
Base – Emitter Turn-on Voltage (Note 4) (I <sub>C</sub> = -1.0 A, V <sub>CE</sub> = -2.0 V)	V <sub>BE(on)</sub>	-	-	-0.900	V
Cutoff Frequency (I <sub>C</sub> = -100 mA, V <sub>CE</sub> = -5.0 V, f = 100 MHz)	f <sub>T</sub>	100	-	-	MHz
Input Capacitance (V <sub>EB</sub> = -0.5 V, f = 1.0 MHz)	C <sub>ibo</sub>	-	-	350	pF
Output Capacitance (V <sub>CB</sub> = -3.0 V, f = 1.0 MHz)	C <sub>obo</sub>	-	-	120	pF

### SWITCHING CHARACTERISTICS

Delay (V <sub>CC</sub> = -10 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>d</sub>	-	-	60	ns
Rise (V <sub>CC</sub> = -10 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>r</sub>	-	-	120	ns
Storage (V <sub>CC</sub> = -10 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>s</sub>	-	-	250	ns
Fall (V <sub>CC</sub> = -10 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>f</sub>	-	-	130	ns

4. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.  
 5. Guaranteed by design but not tested.

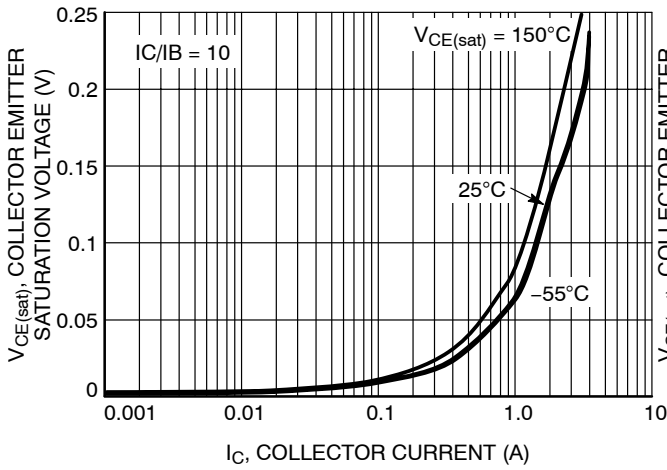


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

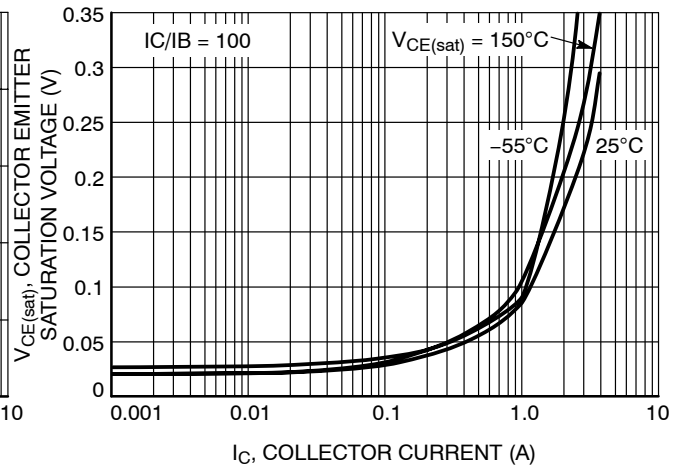


Figure 2. Collector Emitter Saturation Voltage vs. Collector Current

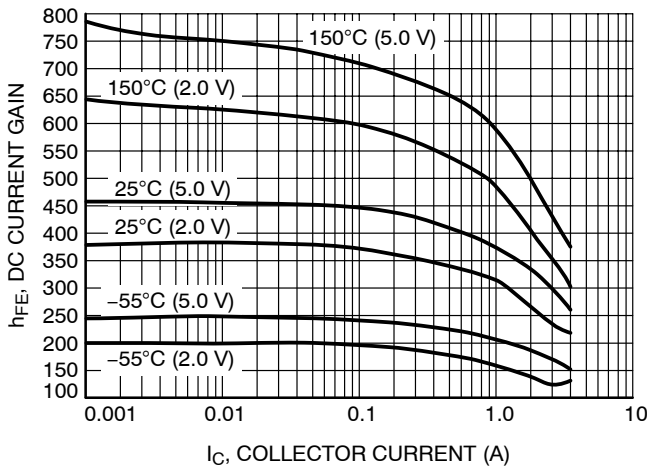


Figure 3. DC Current Gain vs. Collector Current

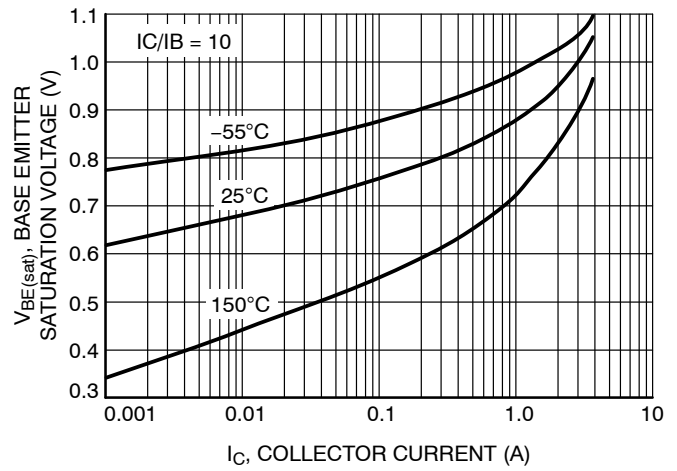


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

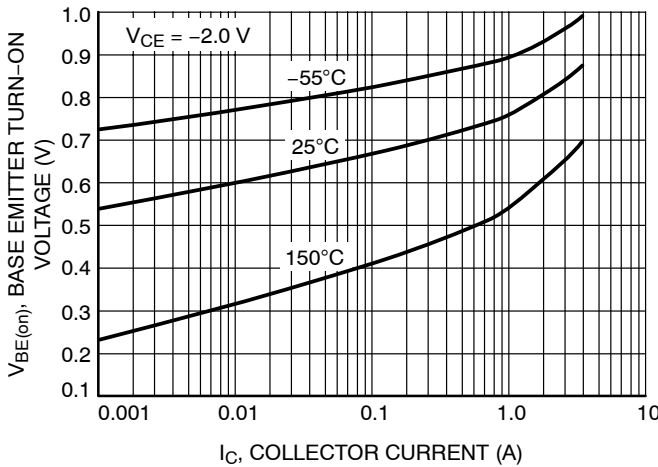


Figure 5. Base Emitter Turn-On Voltage vs. Collector Current

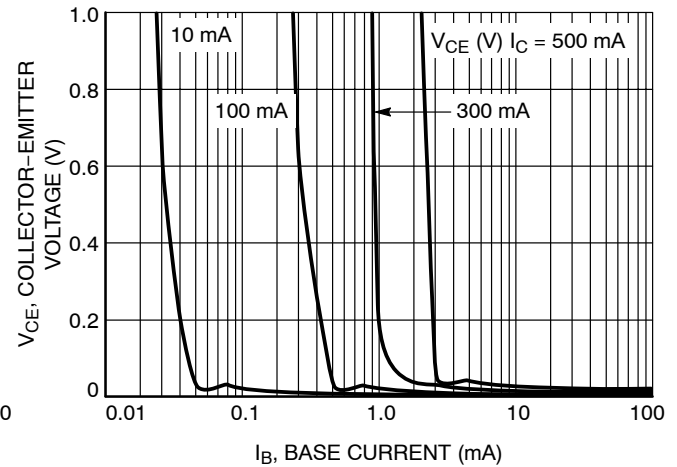
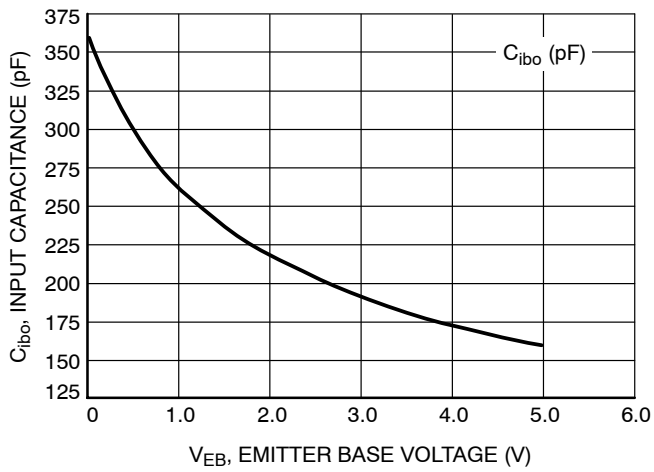
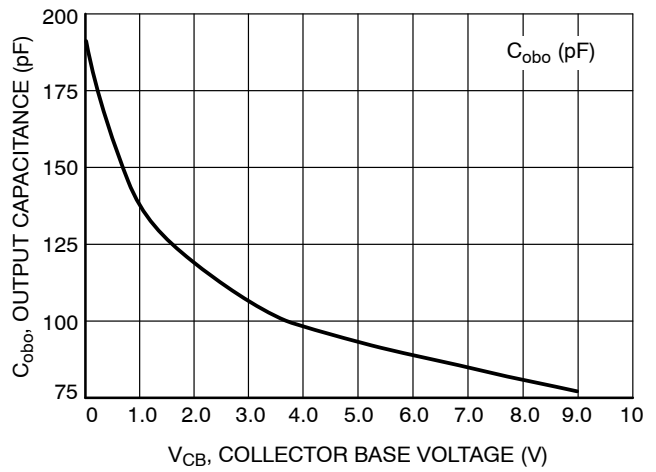


Figure 6. Saturation Region

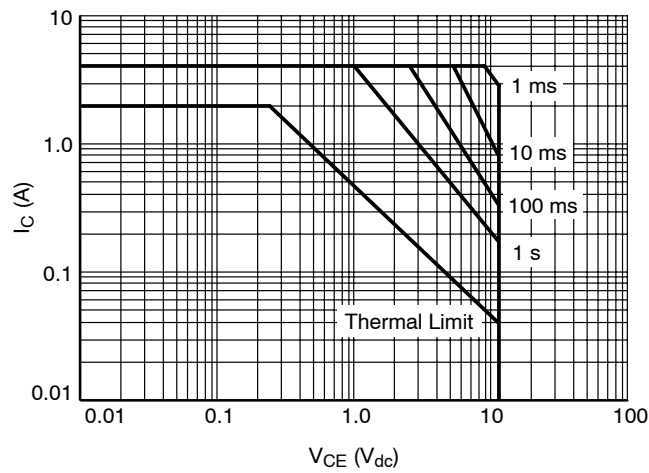
# NSS12200LT1G



**Figure 7. Input Capacitance**



**Figure 8. Output Capacitance**

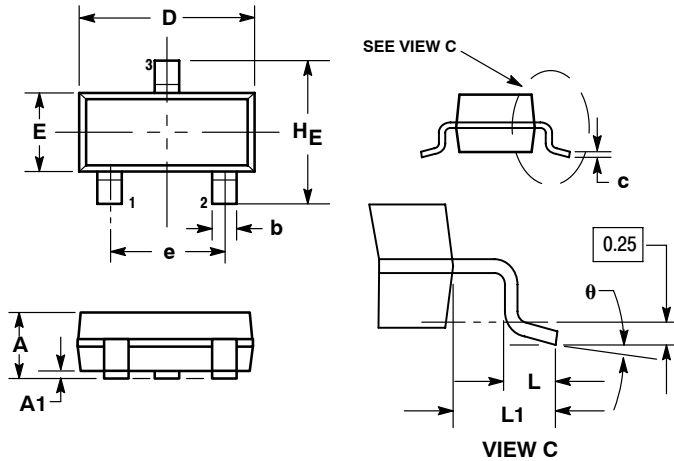


**Figure 9. Safe Operating Area**

# NSS12200LT1G

## PACKAGE DIMENSIONS

SOT-23 (TO-236)  
CASE 318-08  
ISSUE AN



NOTES:

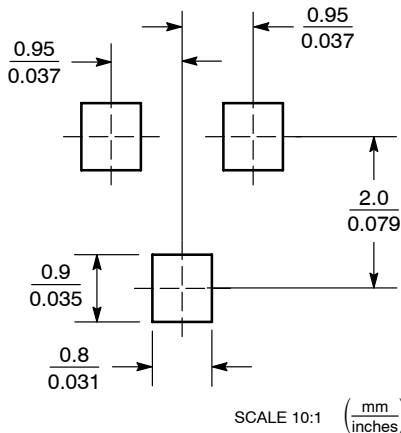
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:

- PIN 1: BASE
- EMITTER
- COLLECTOR

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5773-3850

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)  
Order Literature: <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative

NSS12200L/D