NSL35TT1

High Current Surface Mount PNP Silicon Low $V_{CE(sat)}$ Transistor for Battery Operated Applications

ON Semiconductor™

http://onsemi.com

35 VOLTS
1.0 AMPS
PNP TRANSISTOR

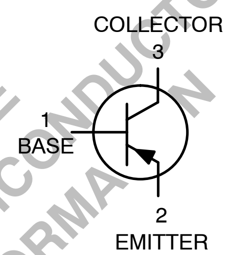
MAXIMUM RATINGS (T_A = 25°C)

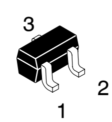
Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	−35	Vdc
Collector-Base Voltage	V_{CBO}	−50	Vdc
Emitter-Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Peak − Continuous	I_C	−1.0 −500	Adc mAdc
Electrostatic Discharge	ESD	HBM Class 3B MM Class C	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1)	210 1.7	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (Note 1)	595	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2)	365 2.9	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (Note 2)	340	°C/W
Thermal Resistance, Junction to Lead #3	$R_{\theta JL}$	205	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

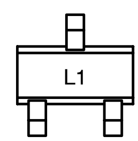
1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 X 1.0 inch Pad





CASE 463
SOT−416/SC−75
STYLE 1

DEVICE MARKING



L1 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NSL35TT1	SOT−416	3000/Tape & Reel

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (I_C = −10 mAdc, I_B = 0)	$V_{(BR)CEO}$	−35	−45	–	Vdc
Collector – Base Breakdown Voltage (I_C = −0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	−50	−65	–	Vdc
Emitter – Base Breakdown Voltage (I_E = −0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	−7.0	–	Vdc
Collector Cutoff Current (V_{CB} = −35 Vdc, I_E = 0)	I_{CBO}	–	−0.03	−0.1	μAdc
Collector−Emitter Cutoff Current (V_{CES} = −30 Vdc)	I_{CES}	–	−0.03	−0.1	μAdc
Emitter Cutoff Current (V_{EB} = −4.0 Vdc)	I_{EBO}	–	−0.01	−0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (Note 3)	h_{FE}				
(I_C = −100 mA, V_{CE} = −1.0 V)		100	180	–	
(I_C = −100 mA, V_{CE} = −2.0 V)		100	180	–	
(I_C = −250 mA, V_{CE} = −2.0 V)		100	150	–	
Collector – Emitter Saturation Voltage (Note 3)	$V_{CE(sat)}$				V
(I_C = −50 mA, I_B = −0.5 mA)		–	−0.090	−0.130	
(I_C = −100 mA, I_B = −1.0 mA)		–	−0.200	−0.350	
(I_C = −250 mA, I_B = −2.5 mA)		–	−0.320	−0.450	
(I_C = −250 mA, I_B = −5.0 mA)		–	−0.170	–	
(I_C = −500 mA, I_B = −50 mA)		–	−0.270	−0.350	
Base – Emitter Saturation Voltage (Note 3) (I_C = −150 mA, I_B = −20 mA)	$V_{BE(sat)}$	–	−0.81	−0.9	V
Base – Emitter Turn−on Voltage (Note 3) (I_C = −150 mA, V_{CE} = −3.0 V)	$V_{BE(on)}$	–	−0.81	−0.875	V
Input Capacitance (V_{EB} = 0 V, f = 1.0 MHz)	C_{ibo}	–	45	–	pF
Output Capacitance (V_{CB} = 0 V, f = 1.0 MHz)	C_{obo}	–	18	–	pF
Turn−On Time (I_{BI} = −50 mA, I_C = −500 mA, R_L = 3.0 Ω)	t_{on}	–	40	–	ns
Turn−Off Time (I_{B1} = I_{B2} = −50 mA, I_C = −500 mA, R_L = 3.0 Ω)	t_{off}	–	70	–	ns

3. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

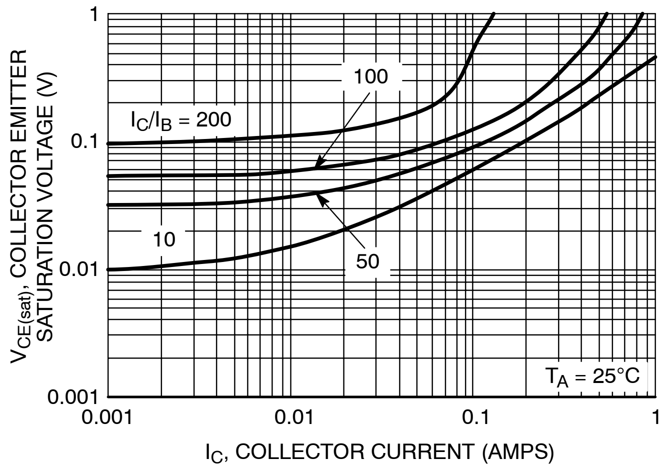


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

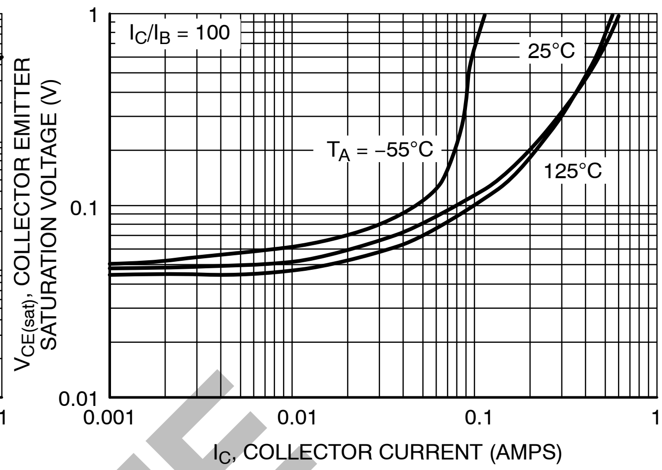


Figure 2. Collector Emitter Saturation Voltage vs. Collector Current

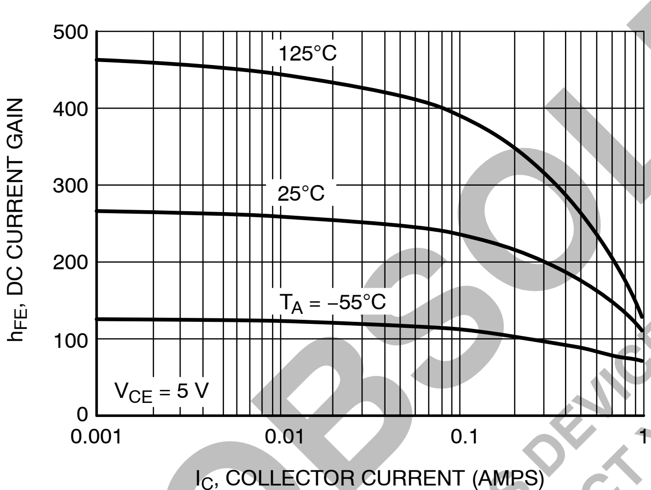


Figure 3. DC Current Gain

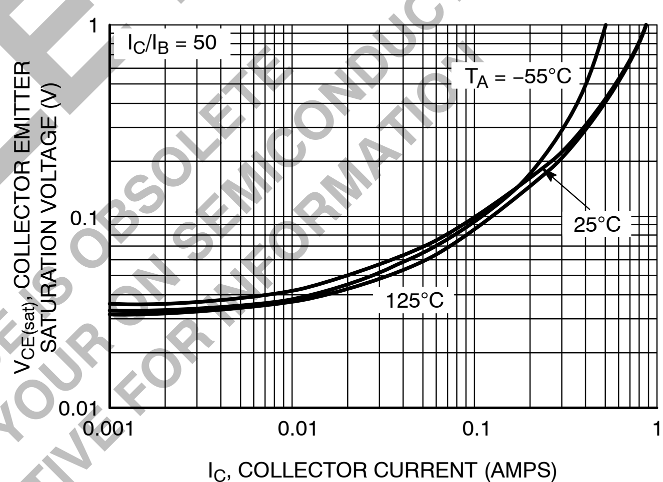


Figure 4. Collector Emitter Saturation Voltage vs. Collector Current

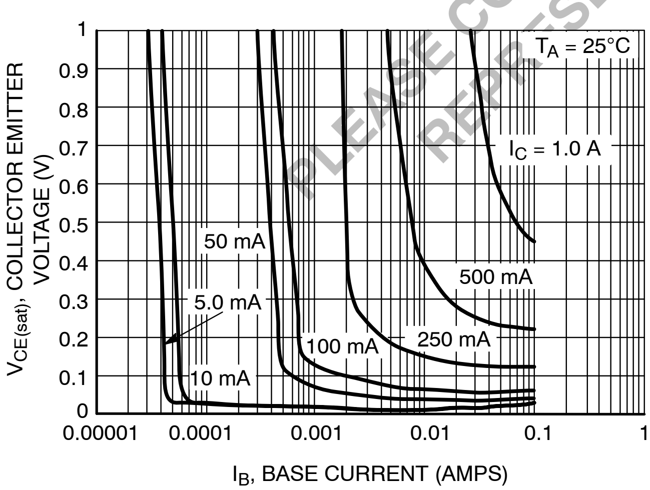


Figure 5. Collector Emitter Saturation Voltage vs. Base Current

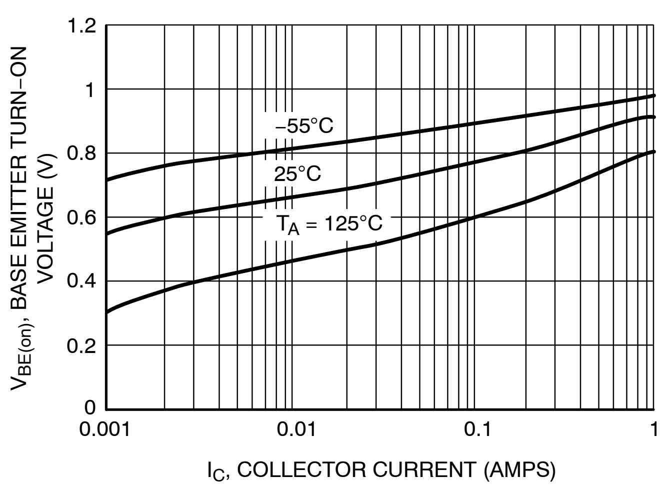


Figure 6. Base Emitter Saturation Voltage vs. Collector Current

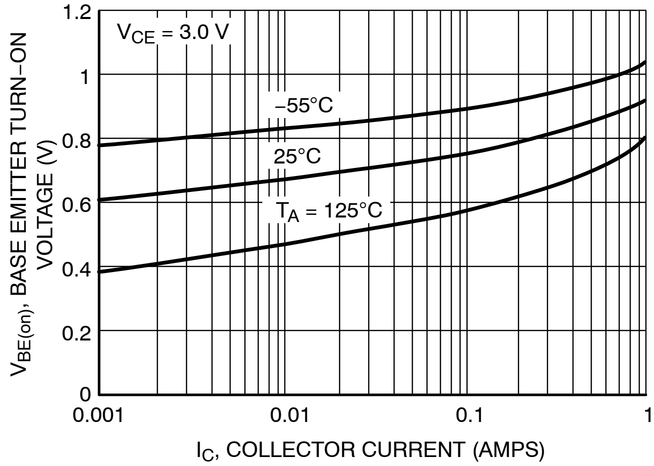


Figure 7. Base Emitter Turn−On Voltage vs. Collector Current

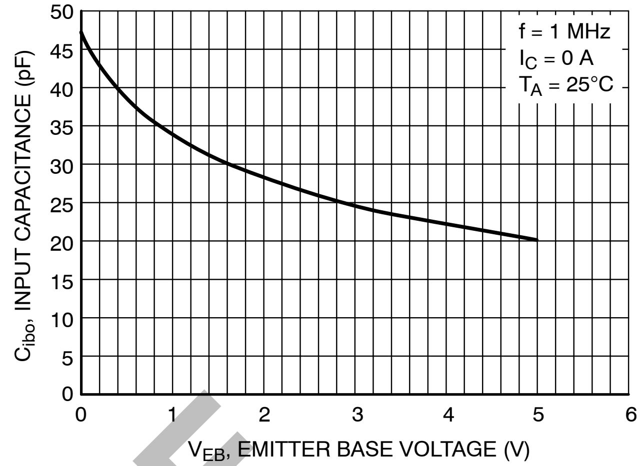


Figure 8. Input Capacitance

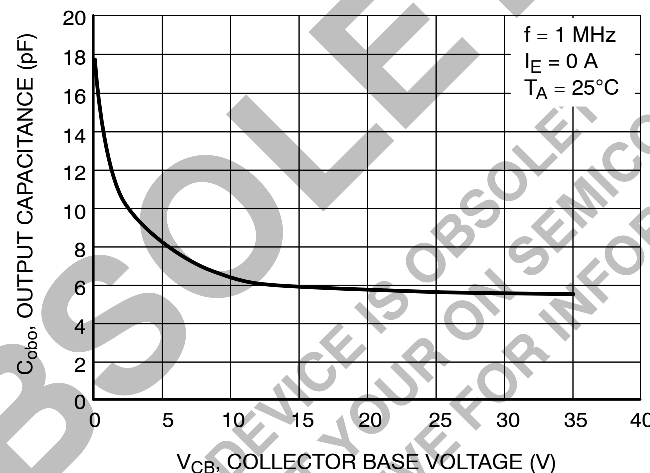


Figure 9. Output Capacitance

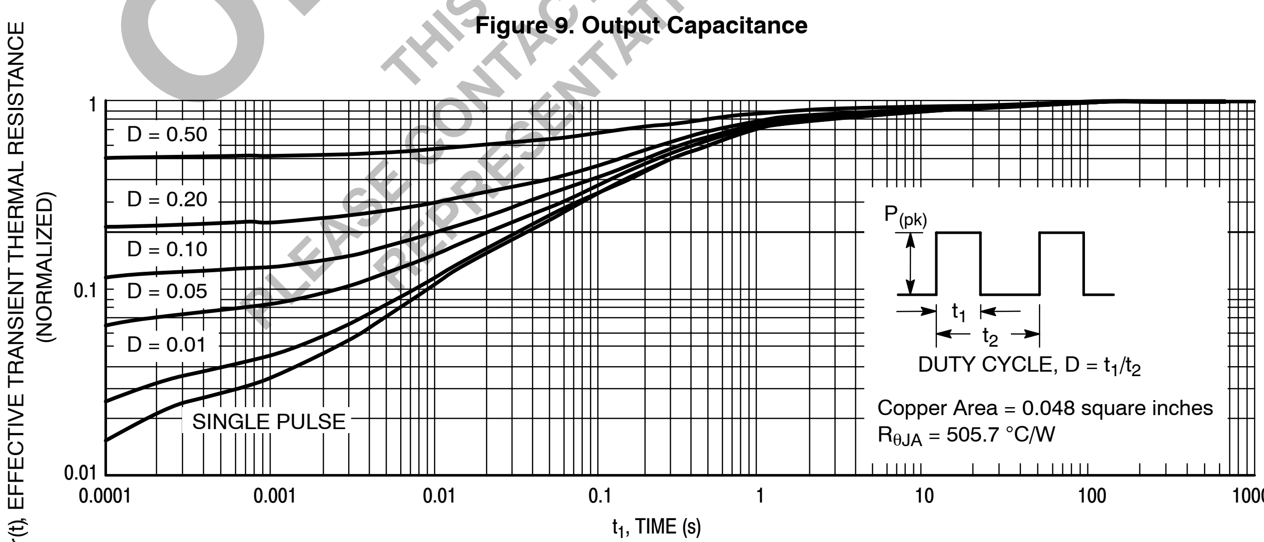
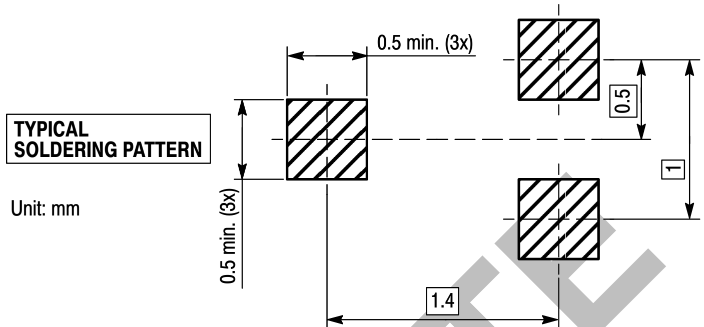


Figure 10. Normalized Thermal Response

INFORMATION FOR USING THE SOT−416 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT−416/SC−90 POWER DISSIPATION

The power dissipation of the SOT−416/SC−90 is a function of the pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R\theta_{JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 125 milliwatts.

$$P_D = \frac{150°C - 25°C}{833°C/W} = 150 \text{ milliwatts}$$

The 833°C/W assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, a higher power dissipation can be achieved using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the surface mounted package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 11 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177−189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

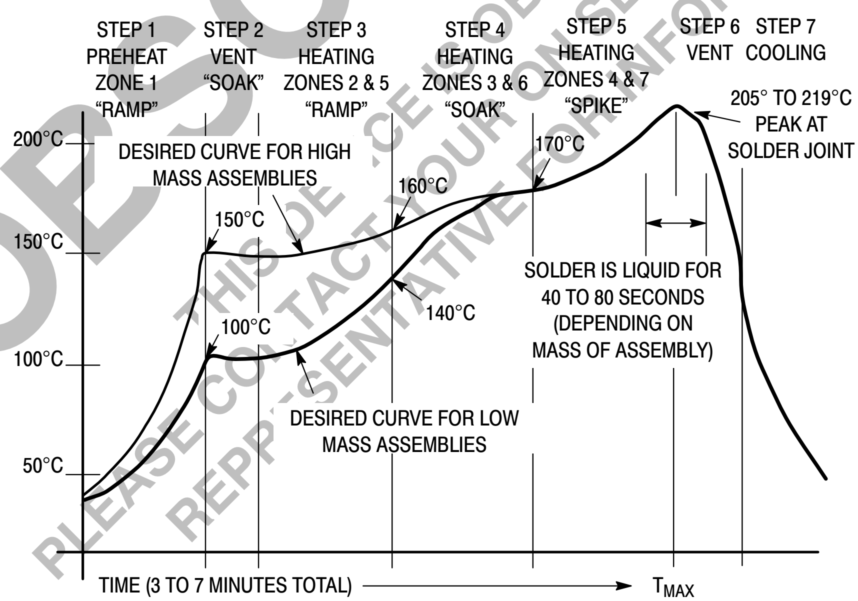
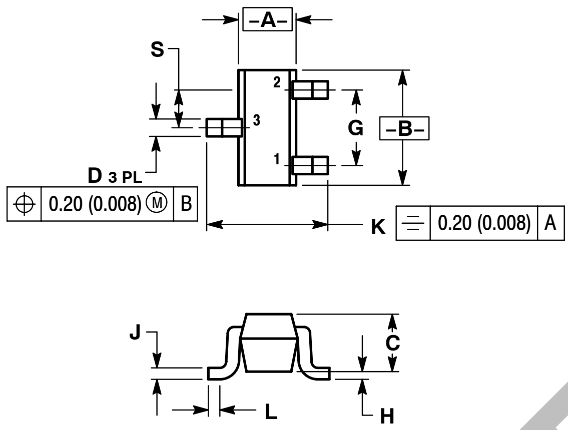


Figure 11. Typical Solder Heating Profile

PACKAGE DIMENSIONS

SC−75/SOT−416
CASE 463−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	0.70	0.80	0.028	0.031
B	1.40	1.80	0.055	0.071
C	0.60	0.90	0.024	0.035
D	0.15	0.30	0.006	0.012
G	1.00 BSC		0.039 BSC	
H	---	0.10	---	0.004
J	0.10	0.25	0.004	0.010
K	1.45	1.75	0.057	0.069
L	0.10	0.20	0.004	0.008
S	0.50 BSC		0.020 BSC	

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

Thermal Clad is a trademark of the Bergquist Company.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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