QST102

Capacitive touch sensor device
2 keys with individual key state outputs

Features

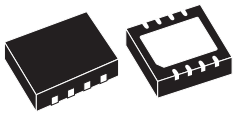
- Patented charge-transfer design
- Two independent QTouch™ keys
- Individual key state output
- Fully “debounced” results
- Self-calibration and drift compensation
- Spread-spectrum bursts to reduce EMI
- Patented AKS™ Adjacent Key Suppression
- Serial validation interface (SVI)
- ECOPACK® (RoHS compliant) packages

Applications

This device specifically targets human interfaces and front panels for a wide range of applications such as PC peripherals, home entertainment systems, gaming devices, lighting and appliance controls, remote controls, etc.

QST devices are designed to replace mechanical switching/control devices and the reduced number of moving parts in the end product provides the following advantages:

- Lower customer service costs
- Reduced manufacturing costs
- Increased product lifetime



VFQFPN8 (DFN8)

Description

The QST102 is the ideal solution for the design of capacitive touch sensing user interfaces.

Touch-sensitive controls are increasingly replacing electromechanical switches in home appliances, consumer and mobile electronics, and in computers and peripherals. Capacitive touch controls allow designers to create stylish, functional, and economical designs which are highly valued by consumers, often at lower cost than the electromechanical solutions they replace.

The QST102 QTouch™ sensor IC is a pure digital solution based on Quantum's patented charge-transfer (QProx™) capacitive technology.

QTouch™ and QProx™ are trademarks of the Quantum Research Group.

Table 1. Device summary

Feature	QST102AU6
Operating supply voltage	2.4V to 5.5V
Supported interface	Individual key state output
Operating temperature	–40° to +85° C
Package	DFN8 (4.5 x 3.5 mm)

Contents

1 Device overview

The QST102 capacitive touch sensor IC is a pure digital solution based on Quantum's patented charge-transfer (QProx™) capacitive technology.

This technology allows users to create simple touch panel sensing electrode interfaces for conventional or flexible printed circuit boards (PCB/FPCB). Sensing electrodes are part of the PCB layout (copper pattern or printed conductive ink) and may be used in various shapes (circle, rectangular, etc.).

By implementing the QProx™ charge-transfer algorithm, the QST102 detects finger presence (human touch) near electrodes behind a dielectric (glass, plastic, wood, etc.). Only one external sampling capacitor by channel is used in the measuring circuitry to control the detection.

QST technology also incorporates advanced processing techniques such as drift compensation, auto-calibration, noise filtering, and Quantum's patented Adjacent Key Suppression™ (AKS™) to ensure maximum usability and control integrity.

In order to meet environmental requirements, ST offers this device in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

2 Pin description

Figure 1. 8-pin VFQFPN8 (DFN8) package pinout

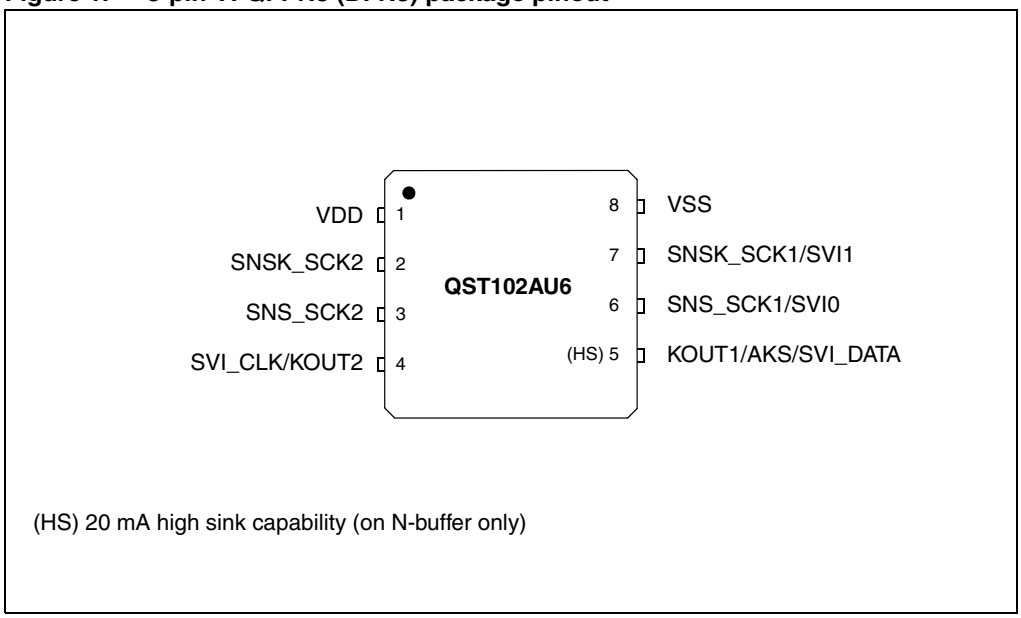


Table 2. Device pin description

Pin no.	Pin name	Type (1)	Function	If unused
1	VDD	S	Supply voltage	
2	SNSK_SCK2	SNS	Key 2 sense pin to C_S/R_S	Open
3	SNS_SCK2	SNS	Key 2 sense pin to C_S	Open
4	KOUT2/SVI_CLK (2)	PP	Key 2 output and Serial Validation Interface clock output	1nF capacitor
5	KOUT1/AKS/SVI_DATA (3)	PP	Key 1 output, AKS option resistor and Serial Validation Interface data output	Option resistor
6	SNS_SCK1/SVI0	SNS	Key 1 sense pin to C_S and Serial Validation Interface input 0	Open
7	SNSK_SCK1/SVI1	SNS	Key 1 sense pin to C_S/R_S and Serial Validation Interface input 1	Open
8	VSS	S	Ground voltage	

1. S: supply pin, PP: Output push-pull pin and SNS: Capacitive sensing pin
2. To ensure correct reset of device, a 1nF capacitor must be connected to this pin. During reset phase, this pin must not be driven.
3. During the reset phase, this pin is floating and its state depends on the option resistor.

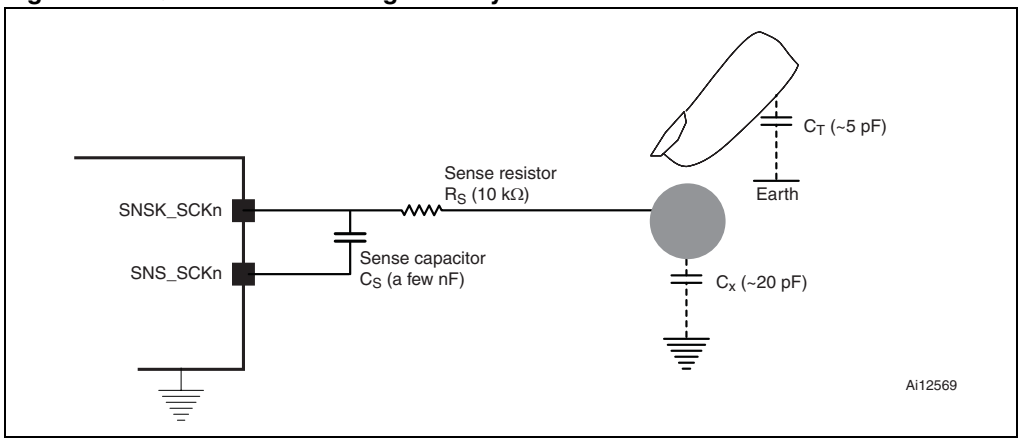
3 QST touch sensing technology

3.1 Functional description

QST devices employ bursts of charge-transfer cycles to acquire signals. Burst mode permits low power operation, dramatically reduces RF emissions, lowers susceptibility to RF fields, and yet permits excellent speed. Signals are processed using algorithms pioneered by Quantum which are specifically designed to provide reliable, trouble-free operation over the life of the product.

The QST switches and charge measurement hardware functions are all internal to the device. An external C_S capacitor accumulates the charge from sense-plate C_X, which is then measured. Larger values of C_X cause the charge transferred into C_S to rise more rapidly, reducing available resolution. As a minimum resolution is required for proper operation, this can result in dramatically reduced gain. Larger values of C_S reduce the rise of differential voltage across it, increasing available resolution by permitting longer QST bursts. The value of C_S can thus be increased to allow larger values of C_X to be tolerated. The device is responsive to both C_X and C_S, and changes in either can result in substantial changes in sensor gain.

Figure 2. QTouch™ measuring circuitry



3.2 Spread-spectrum operation

The bursts operate over a spread of frequencies, so that external fields will have minimal effect on key operation and emissions are very weak. Spread-spectrum operation works with the Detection Integrator mechanism (DI) to dramatically reduce the probability of false detection due to noise.

3.3 Faulty and unused keys

Any sensing channel that does not have its sense capacitor (C_S) fitted is assumed to be either faulty or unused. This channel takes no further part in operation unless a Master-commanded recalibration operation shows it to have an in-range burst count again. Faulty, unused or disabled keys are still bursted but not processed to avoid modifying the sensitivity of active keys.

This is important for sensing channels that have an open or short circuit fault across C_S. Such channels would otherwise cause very long acquire bursts, and in consequence would slow the operation of the entire QST device.

To optimize touch response time and device power consumption, if some keys are not used, we recommend to try suppressing the ones which belong to the same burst. Bursts which do not have any keys implemented will then not be processed.

3.4 Detection threshold levels

The key capacitance change induced by the presence of a finger is sensed by the variation in the number of charge transfer pulses to load the capacitor. The difference in the pulse count number is compared to a threshold in order to detect the key as pressed or not.

Two different thresholds, one for detection and one for the end of detection, create an hysteresis in order to prevent erratic behavior.

The default threshold levels and hysteresis values are described in*Section 6.6: Capacitive sensing characteristics on page 19*.

3.5 Detection integrator filters

The Detection Integrator (DI) filter mechanism works together with spread spectrum operation to dramatically reduce the effects of noise on key states. The DI mechanism requires a specified number of measurements that qualify as detections (and these must occur in a row) or the detection will not be reported.

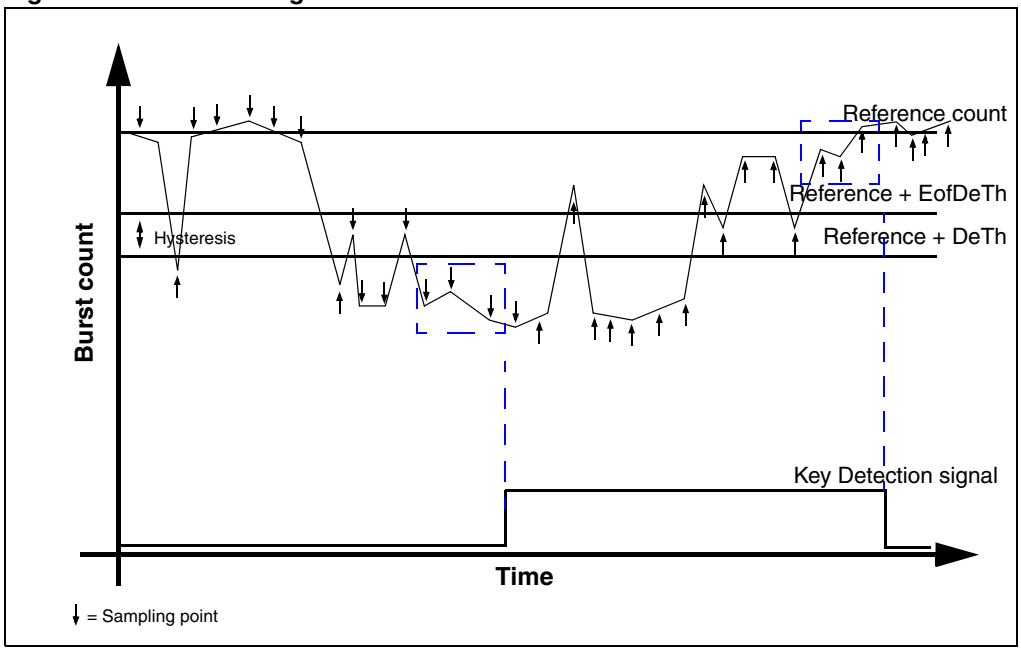
In a similar manner, the end of a touch (loss of signal) also has to be confirmed over several measurements. It is called the End of Detection Integrator (EDI).

This process acts as a type of “debounce” mechanism against noise.

The default DI and EDI values for confirming start of touch and end of touch are described in *Section 6.6: Capacitive sensing characteristics on page 19*.

Figure 3 shows an example of detection with DI=2 and EDI=2 meaning 3 consecutive samples are necessary to trigger the key detection or end of detection

Figure 3. Detection signals



3.6 Self-calibration

On power-up, all keys are self-calibrated to provide reliable operation under almost any conditions. The calibration phase is used to compute a reference value per key which is then used by the process determining if a key is touched or not. The reference is an average of 8 single acquisitions. As a result, the calibration time of the system can be simply calculated using the following formula: t_{CAL} = 8 * Burst_Period. The methodology used to measure the burst period is described in application note AN2547. For a maximum calibration duration (t_{CAL}), please refer to *Section 6.6: Capacitive sensing characteristics on page 19*.

3.7 Fast positive recalibration

The device autorecalibrates a key when its signal reflects a decrease in capacitance higher than a fixed threshold (PosRecalTh) for a defined number of acquisitions (PosRecalI).

3.8 Max on-duration

The device can time out and automatically recalibrate each key independently after a fixed duration of continuous touch detection. This prevents the keys from becoming ‘stuck on’ due to foreign objects or other sudden influences. This is known as the Max On-Duration feature.

After recalibration, the key will continue to operate normally, even if partially or fully obstructed. Max On-Duration works independently per channel: a timeout on one channel has no effect on another channel.

3.9 Drift compensation

Signal drift can occur because of changes in C_X, C_S, and V_{DD} over time. Depending on the C_S type and quality, the signal may vary substantially with temperature and veiling. If keys are subject to extremes of temperature or humidity, the signal can also drift. It is crucial that drift be compensated, otherwise false detections, non detections, and sensitivity shifts will follow.

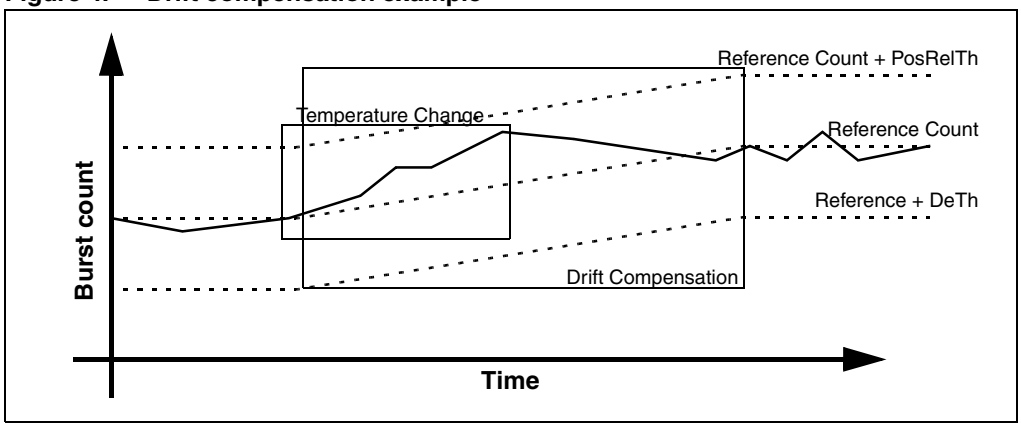
Drift compensation slowly corrects the reference level of each key while no detection is in effect. The rate of reference adjustment must be performed slowly or else legitimate detections can also be ignored. The device compensates drift on each channel independently using a maximum compensation rate to the reference level.

Once a touch is sensed, the drift compensation mechanism ceases since the signal is legitimately high, and therefore should not cause the reference level to change.

The signal drift compensation is “asymmetric”: the reference level compensates drift in one direction faster than it does in the other. Specifically, it compensates faster for increasing signals than for decreasing signals. Decreasing signals should not be compensated for quickly, since an approaching finger could be compensated for partially or entirely while approaching the sense electrode. However, an obstruction over the sense pad, for which the sensor has already made full allowance, could suddenly be removed leaving the sensor with an artificially elevated reference level and thus become insensitive to touch. In this latter case, the sensor will compensate for the object's removal very quickly, usually in only a few seconds.

Figure 4 illustrates an example of the drift compensation algorithm following a temperature change.

Figure 4. Drift compensation example



3.10 Adjacent key suppression (AKS™)

Adjacent key suppression (AKS™) is a Quantum-patented feature which prevents multiple keys from responding to a single touch. This can happen with closely spaced keys, or a scroll wheel that has buttons very near it.

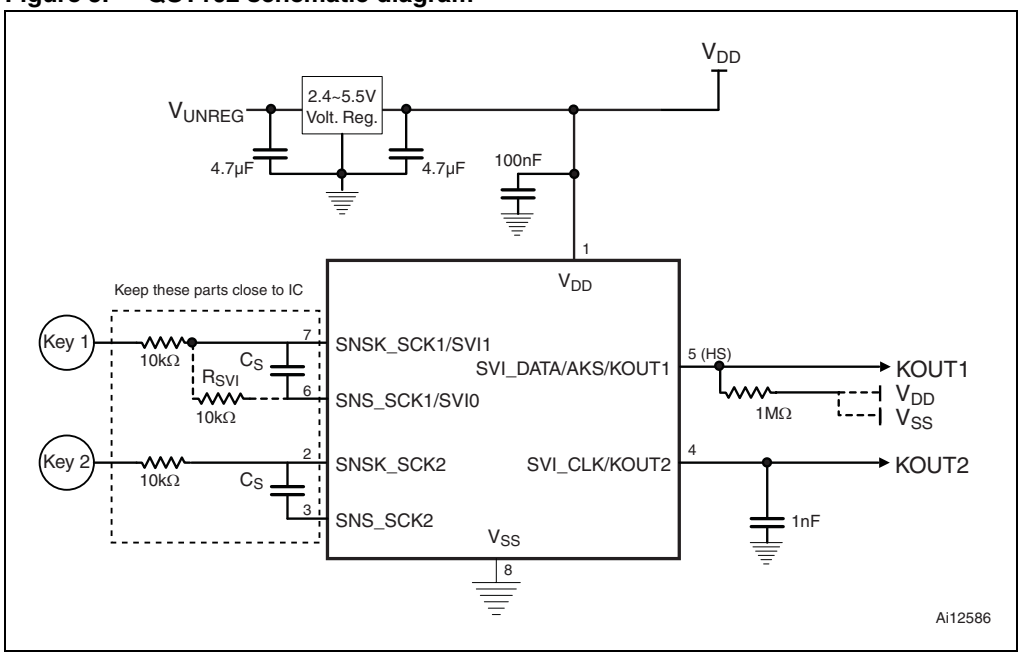
The device supports Locking AKS mode where once a key is considered as “touched”, all other keys are locked in an untouched state. To unlock these keys, the touched key must return to an untouched state. Then, the key having the lowest key ID number is declared as the “touched” one.

4 Device operating mode

4.1 Main features

- Pins KOUT1 and KOUT2 directly reflect the state of keys
- Selectable locking adjacent key suppression (AKS™)
- Max On-Duration feature
- Serial validation interface (SVI)

Figure 5. QST102 schematic diagram



4.2 Power-up

At power-up the device configures itself. During this phase, it reads the AKS option through the option resistor on pin KOUT1.

4.3 KOUT output

KOUT*n* output pins directly reflect the state of the corresponding key. These pins are push-pull outputs.

During QST device reset phase:

- pin KOUT1 is floating and its state depends on the option resistor
- pin KOUT2 is output push pull high

KOUT*n* output pins are active high, meaning when the key is “touched”, the pin outputs a ‘1’.

4.4 Adjacent key suppression (AKS™)

The adjacent key suppression (AKS™) function is enabled using the AKS option resistor (pin KOUT1/AKS) as described in *Table 3*.

Table 3. AKS truth table

KOUT1/AKS	Description
V_{SS}	Disabled
V_{DD}	Global locking AKS on all available keys

4.5 Max on-duration

The Max On-Duration time is set to 30 seconds. This means that a continuous “touched” detection for 30 seconds on a key triggers a recalibration. When such an event occurs, only the “stuck” key is recalibrated.

4.6 Serial validation interface (SVI)

The serial validation interface (SVI) acts as an SPI master device. It provides access to the following internal device information:

- device identifier string sent once after the Reset phase
- internal system parameters sent after each acquisition
  - key states
  - key references
  - key signals

This data access facilitates system tuning an can be used as a debug interface.

To enter SVI mode, before power-up connect resistor R_{SVI} between SVI input 0 and SVI input 1 pins as shown in *Figure 5*. Then, within 10 seconds following power-up disconnect resistor R_{SVI} in order to not modify Key 1 electrode calibration and operation.

After this 10-second delay, the device operates normally with SVI data and clock signals being output on pins KOUT1 and KOUT2, respectively.

Please refer to *RM0014: QST serial validation interface reference manual* for more information about the SVI operating mode.

5 Design guidelines

5.1 C_S sense capacitor

The C_S sense capacitors accumulate the charge from the key electrodes and determine sensitivity. Higher values of C_S make the corresponding sensing channel more sensitive. The values of C_S can differ for each channel, permitting differences in sensitivity from key to key or to balance unequal sensitivities. Unequal sensitivities can occur due to key size and placement differences and stray wiring capacitances. More stray capacitance on a sense trace will desensitize the corresponding key. Increasing the C_S for that key will compensate for the loss of sensitivity.

The C_S capacitors can be virtually any plastic film or low- to medium-K ceramic capacitor. The normal C_S range is 1nF to 50nF depending on the sensitivity required: larger values of C_S require better quality to ensure reliable sensing. In certain circumstances the normal C_S range may be exceeded. Acceptable capacitor types for most uses include PPS film, polypropylene film, and NP0 and X5R / X7R ceramics. Lower grades than X5R or X7R are not recommended.

5.2 Sensitivity tuning

Sensitivity can be altered to suit various applications and situations on a channel-by-channel basis. The easiest and most direct way to impact sensitivity is to alter the value of each C_S: more C_S yields higher sensitivity. Each channel has its own C_S value and can therefore be independently adjusted.

5.2.1 Increasing sensitivity

Sensitivity can also be increased by using larger electrode areas, reducing panel thickness, or using a panel material with a higher dielectric constant.

5.2.2 Decreasing sensitivity

In some cases the circuit may be too sensitive. Gain can be lowered further by a number of strategies:

- making the electrode smaller
- making the electrode into a sparse mesh using a high space-to-conductor ratio
- decreasing the C_S capacitors

5.2.3 Key balance

A number of factors can cause sensitivity imbalances. Notably, SNS wiring to electrodes can have differing stray amounts of capacitance to ground. Increasing load capacitance will cause a decrease in gain. Key size differences, and proximity to other metal surfaces can also impact gain.

The keys may thus require “balancing” to achieve similar sensitivity levels. This can be best accomplished by trimming the values of the C_S capacitors to achieve equilibrium. The R_S resistors have no effect on sensitivity and should not be altered. Load capacitances to ground can also be added to overly sensitive channels to reduce their gain.

These should be in the order of a few picofarads.

5.3 Power supply

If the power supply fluctuates slowly with temperature, the QST device compensates automatically for these changes with only minor changes in sensitivity. However, if the supply voltage drifts or shifts quickly, the drift compensation mechanism is not able to keep up, causing sensitivity anomalies or false detections.

The power supply should be locally regulated, using a three-terminal regulator. If the supply is shared with another electronic system, care should be taken to ensure that the supply is free of digital spikes, sags and surges which can cause adverse effects. It is not recommended to include a series inductor in the power supply to the QST device.

For proper operation, a 0.1 µF or greater bypass capacitor must be used between V_{DD} and V_{SS}. The bypass capacitor should be routed with very short tracks to the device's V_{DD} and V_{SS} pins.

The PCB should, if possible, include a copper pour under and around the device, but not extensively under the SNS lines.

5.4 ESD protection

In normal environmental conditions, only one series resistor is required for ESD suppression. A 10 kOhm R_S resistor in series with the sense trace is sufficient in most cases. The dielectric panel (glass or plastic) usually provides a high degree of isolation to prevent ESD discharge from reaching the circuit. R_S should be placed close to the chip. If the C_X load is high, R_S can prevent total charge and transfer and as a result gain can deteriorate. If a reduction in R_S increases gain noticeably, the lower value should be used. Conversely, increasing the R_S can result in added ESD and EMC benefits, provided that the increase does not decrease sensitivity.

5.5 Crosstalk precautions

Adjacent sense traces might require intervening ground traces in order to reduce capacitive cross bleed if high sensitivity is required or high values of delta-C_X are anticipated (for example, from direct human touch to an electrode connection). In normal touch applications behind plastic panels, this is rarely a problem regardless of how the electrodes are wired.

Higher values of R_S will make crosstalk problems worse; try to keep R_S to 22 kOhm or less if possible. In general try to keep the QST device close to the electrodes and reduce the adjacency of the sense wiring to ground planes and other signal traces; this will reduce the C_x load, reduce interference effects, and increase signal gain. The one and only valid reason to run ground near SNS traces is to provide crosstalk isolation between traces, and then only on an as-needed basis.

5.6 PCB layout and construction

The PCB traces, wiring, and any components associated with or in contact with either SNS pin will become touch sensitive and should be treated with caution to limit the touch area to the desired location.

Multiple touch electrodes connected to any sensing channel can be used, for example, to create control surfaces on both sides of an object.

It is important to limit the amount of stray capacitance on the SNS terminals, for example by minimizing trace lengths and widths to allow for higher gain without requiring higher values of C_S. Under heavy delta-C_X loading of one key, cross coupling to another key's trace can cause the other key to trigger. Therefore, electrode traces from adjacent keys should not be run close to each other over long runs in order to minimize cross-coupling if large values of delta-C_X are expected, for example when an electrode is directly touched. This is not a problem when the electrodes are working through a plastic panel with normal touch sensitivity.

For additional information on PCB layout and construction, please contact your local ST Sales Office for a list of available application notes.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5 V (for the 4.5V ≤ V_{DD} ≤ 5.5 V voltage range) and V_{DD} = 3.3 V (for the 3.0 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

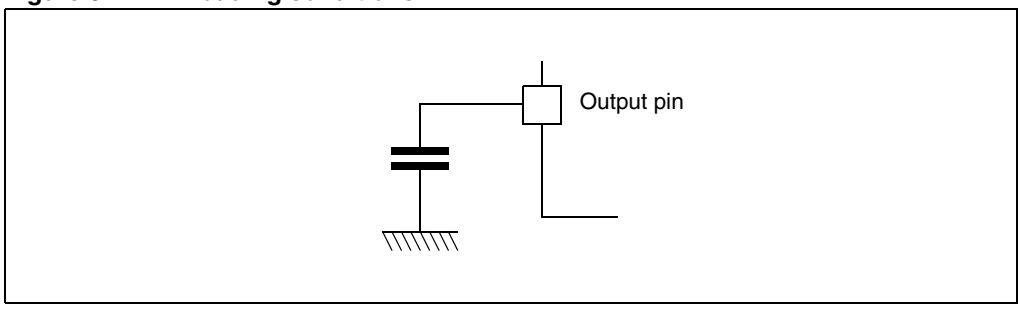
6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

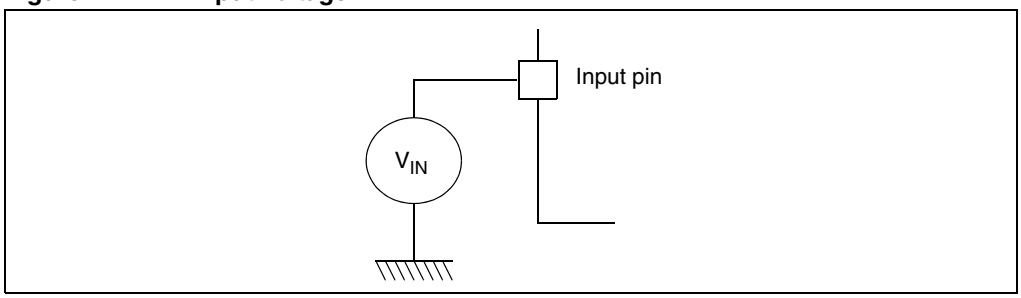
Figure 6. Pin loading conditions



6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage



6.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

6.2.1 Thermal characteristics

Table 4. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature (1)	150	

1. The maximum chip-junction temperature is based on technology characteristics.

6.2.2 Voltage characteristics

Table 5. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
$V_{DD} - V_{SS}$	Supply voltage	7.0	V
V_{IN}	Input voltage on any pin (1)(2)	V_{SS}–0.3 to V_{DD}+0.3	

1. Directly connecting KOUT pins to V_{DD} or V_{SS} could damage the device if an unintentional internal reset is generated.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

6.2.3 Current characteristics

Table 6. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	75	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by KOUT pins	20	
	Output current source by KOUT pins	– 25	
$I_{INJ(PIN)}$(2)(3)	Injected current on KOUT pins	± 5	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)	± 20	

1. All power (V_{DD}) and ground (V_{SS}) lines must always be connected to the external supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly ensured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

6.3 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

6.3.1 Functional EMS (electro magnetic susceptibility)

The product is stressed by two electro magnetic events until a failure occurs:

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Table 7. Functional EMS

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, complies with IEC 1000-4-2	3B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	V_{DD}=5V, T_A=+25°C complies with IEC 1000-4-4	4A

6.3.2 Electro magnetic interference (EMI)

The product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 8. EM emissions

Symbol	Parameter	Conditions	Monitored Frequency Band	f_{DEVICE} = 4 MHz (1)	Unit
S_{EMI}	Peak level	V_{DD}=5V, T_A=+25°C, complies with SAE J 1752/3	0.1 MHz to 30 MHz	20	dBµV
			30 MHz to 130 MHz	20	
			130 MHz to 1 GHz	13	
			SAE EMI Level	2.5	-

1. Data based on characterization results, not tested in production.

6.3.3 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electro-static discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Charge Device Model. These tests comply with JESD22-A114A/A115A specifications.

Table 9. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	4000	V
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)	T_A=+25°C	500	V

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards.

For more details, refer to the application note AN1181.

Table 10. Electrical sensitivities

Symbol	Parameter	Conditions	Class (1)
LU	Static latch-up class	T_A=+125°C	A
DLU	Dynamic latch-up class	V_{DD}=5.5V, f_{DEVICE} = 4MHz, T_A=+25°C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

6.4 Operating conditions

Table 11. Operating conditions

Symbol	Paremeter	Conditions	Min.	Max.	Unit
V_{DD}	Operating supply voltage	f_{DEVICE} = 4 MHz	2.4	5.5	V
T_A	Operating temperature		–40	+85	°C

6.5 Supply current characteristics

Table 12. Supply current characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Average suppy current when one key is “touched”	V_{DD} = 2.4 V		1.50		mA
		V_{DD} = 3.3 V		1.95		
		V_{DD} = 5 V		2.95		
	Average suppy current when no key is “touched”	V_{DD} = 2.4 V		135		µA
		V_{DD} = 3.3 V		200		
		V_{DD} = 5 V		300		

1. The results are performed at T = 25°C and based on C_S = 2.7nF.

6.6 Capacitive sensing characteristics

Table 13. External sensing components

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_S	Sense capacitor			100	nF
C_X	Equivalent electrode capacitor			100	pF
C_T	Equivalent touch capacitor		5		pF
R_S	Serial resistance		10	22	kOhm

Table 14. Capacitive sensing parameters

Symbol	Parameter	Min.	Default	Max.	Unit
t_{CAL}	Calibration duration				ms
t_{Setup}	Setup duration		100		ms
DI	Detection integrator		2		Counts
DeTh	Detection threshold		-10		Counts
EDI	End of detection integrator		2		Counts
EofDeTh	End of detection threshold		-8		Counts
PosRecalI	Positive recalibration integrator		2		Counts
PosRecalTh	Positive recalibration threshold		6		Counts
MaxOnDuration	Max on-duration delay		30		s
PosDiffDrift	Positive differential drift compensation rate		0.5		s/level
NegDiffDrift	Negative differential drift compensation rate		1		s/level
PosDriftI	Positive drift integrator		5		
NegDriftI	Negative drift integrator		10		
DiffFact	Differential time step factor		2		
BurstCount	Burst length	20		2000	Counts

6.7 KOUT pin characteristics

6.7.1 General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 15. General characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_L	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA
C_{KOUT}	KOUT pin capacitance			5		pF
$t_{f(KOUT)out}$	Output high to low level fall time	C_L = 50 pF Between 10% and 90%		25		ns
$t_{r(KOUT)out}$	Output low to high level rise time			25		

6.7.2 Output pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 16. Output pin current (V_{DD} = 2.4V)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL} (1)	Output low level voltage for pin KOUT1	I_{IO} = +8mA		0.6	V
	Output low level voltage for pin KOUT2	I_{IO} = +2mA		0.6	
V_{OH} (1)	Output high level voltage for pins KOUTn	I_{IO} = -2mA	V_{DD}–0.9		

1. Not tested in production, based on characterization results.

Table 17. Output pin current (V_{DD} = 3.3V)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL} (1)	Output low level voltage for pin KOUT1	I_{IO} = +8mA		0.5	V
	Output low level voltage for pin KOUT2	I_{IO} = +2mA		0.5	
V_{OH} (1)	Output high level voltage for pins KOUTn	I_{IO} = -2mA	V_{DD}–0.8		

1. Not tested in production, based on characterization results.

Table 18. Output pin current (V_{DD} = 5V)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL} (1)	Output low level voltage for pin KOUT1	I_{IO} = +20mA		1.3	V
		I_{IO} = +8mA		0.75	
	Output low level voltage for pin KOUT2	I_{IO} = +5mA		1.0	
		I_{IO} = +2mA		0.4	
V_{OH} (2)	Output high level voltage for pins KOUTn	I_{IO} = -5mA	V_{DD}–1.5		
		I_{IO} = -2mA	V_{DD}–0.8		

1. The KOUT current sunk must always respect the absolute maximum rating specified in *Table 6* and the sum of KOUT must not exceed I_{VSS}.
2. The KOUT current sourced must always respect the absolute maximum rating specified in *Table 6* and the sum of KOUT must not exceed I_{VDD}.

Figure 8. Typical V_{OL} at v_{DD} = 2.4V (KOUT2 pin)

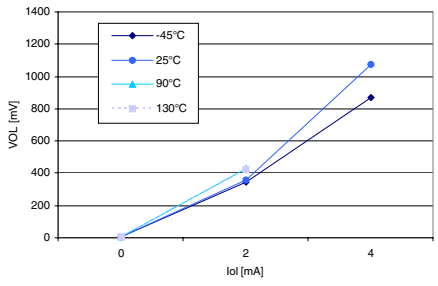


Figure 9. Typical V_{OL} at V_{DD} = 2.4V (KOUT1 pin)

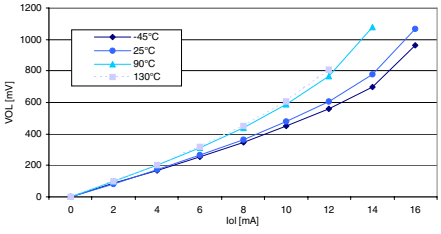


Figure 10. Typical v_{OL} at v_{DD} = 3V (KOUT2 pin)

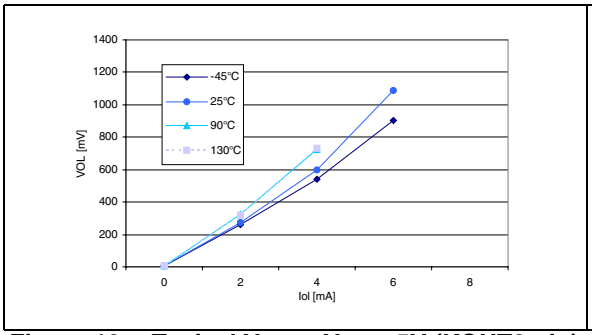


Figure 11. Typical V_{OL} at V_{DD} = 3V (KOUT1 pin)

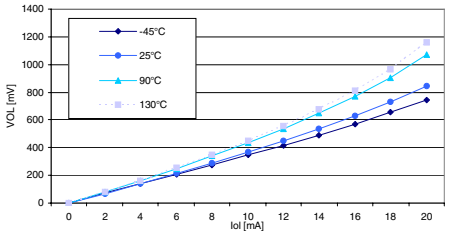


Figure 12. Typical V_{OL} at V_{DD} = 5V (KOUT2 pin)

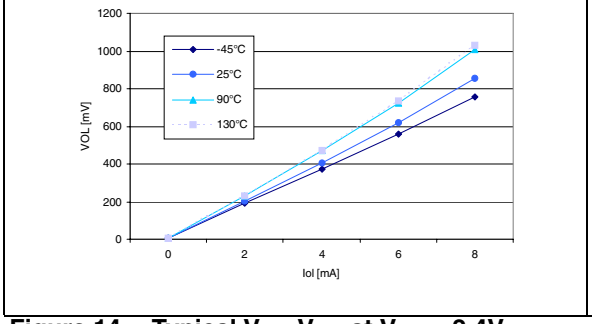


Figure 13. Typical V_{OL} at V_{DD} = 5V (KOUT1 pin)

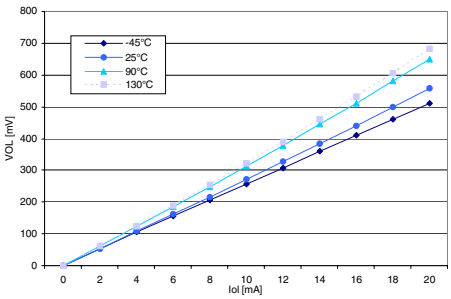


Figure 14. Typical V_{DD}-V_{OH} at V_{DD} = 2.4V (KOUT1 pin)

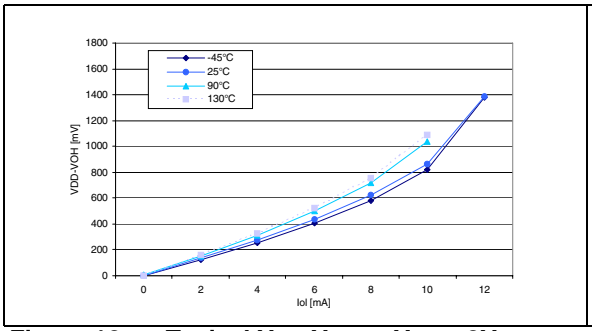


Figure 15. Typical V_{DD}-V_{OH} at V_{DD} = 5V (KOUT1 pin)

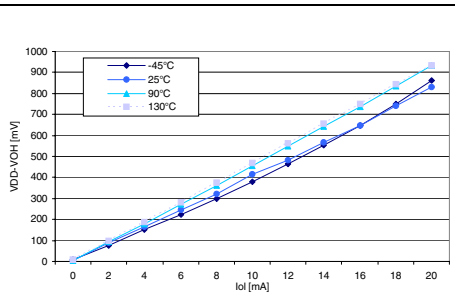


Figure 16. Typical V_{DD}-V_{OH} at V_{DD} = 3V (KOUT1 pin)

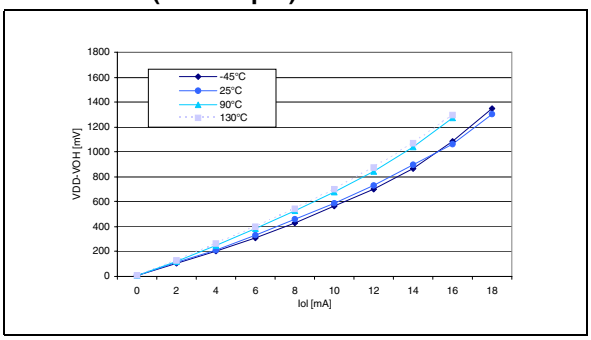


Figure 17. Typical V_{OL} vs. V_{DD} (KOUT1 pin)

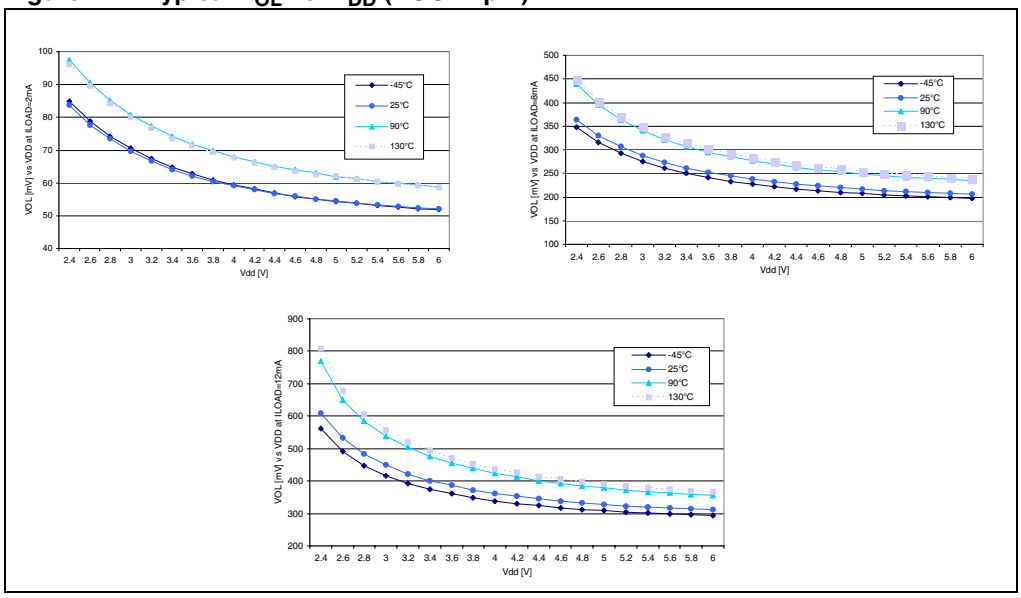
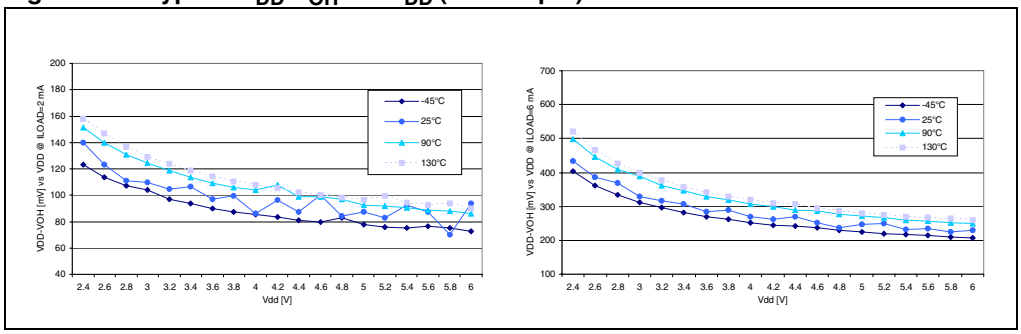


Figure 18. Typical V_{DD}-V_{OH} vs. V_{DD} (KOUT1 pin)



7 Package mechanical data

Figure 19. 8-pin, very thin, fine pitch, quad flat package (DFN) outline

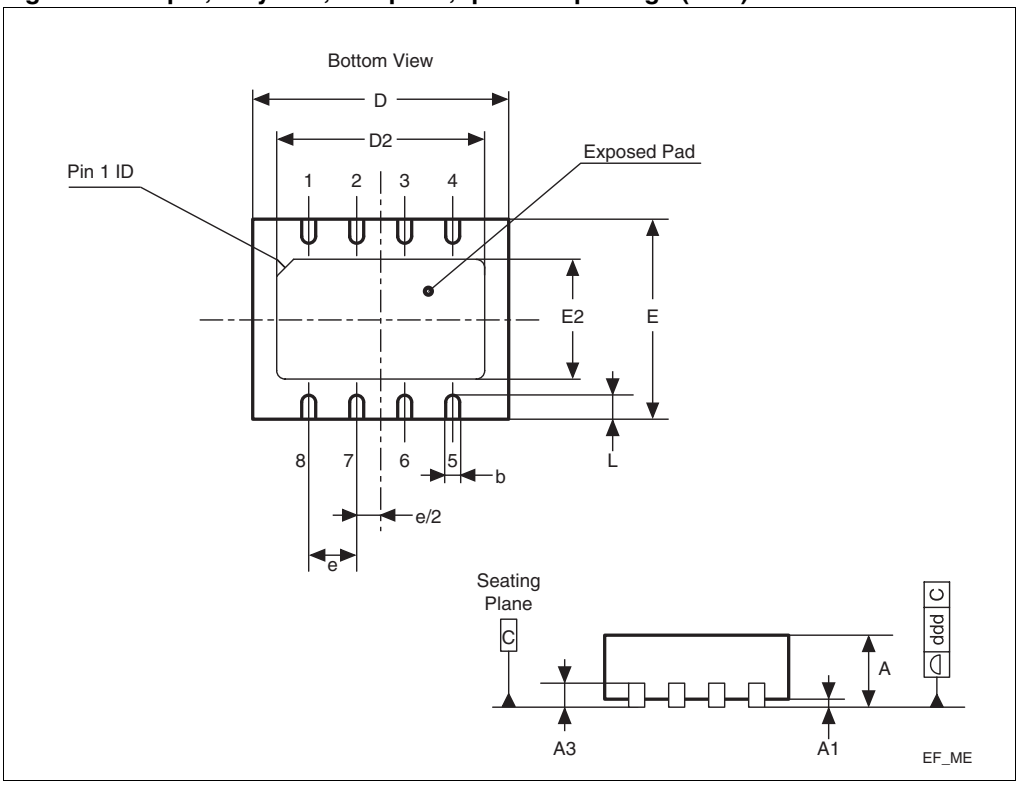


Table 19. 8-pin, very thin, fine pitch, quad flat package (DFN) mechanical data

Dim.	mm			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	0.02	0.05	0.0000	0.0008	0.0020
A3		0.20			0.0079	
b	0.25	0.30	0.35	0.0098	0.01181	0.0138
D	4.35	4.50	4.65	0.1713	0.1771	0.1831
D2	3.50	3.65	3.75	0.1378	0.1437	0.1476
E	3.35	3.50	3.65	0.1319	0.1378	0.1437
E2	1.96	2.11	2.21	0.0772	0.0831	0.0870
e		0.80			0.0315	
L	0.30	0.40	0.50	0.01181	0.0157	0.0197
ddd			0.08			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.1 Soldering information

In accordance with the RoHS European directive, all STMicroelectronics packages have been converted to lead-free technology, named ECOPACK™.

- ECOPACK™ packages are qualified according to the JEDEC STD-020C compliant soldering profile.
- Detailed information on the STMicroelectronics ECOPACK™ transition program is available on www.st.com/stonline/leadfree/, with specific technical Application notes covering the main technical aspects related to lead-free conversion (AN2033, AN2034, AN2035, and AN2036).

Backward and forward compatibility

The main difference between Pb and Pb-free soldering process is the temperature range.

- ECOPACK™ DFN8 packages are fully compatible with Lead (Pb) containing soldering process (see application note AN2034).

Table 20. Soldering compatibility (wave and reflow soldering process)

Plating material devices	Pb solder paste	Pb-free solder paste (1)
Sn (pure Tin)	Yes	Yes

1. Assemblers must verify that the Pb-package maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering process.

8 Part numbering

Table 21. Ordering information scheme

Example: QST 1 02 A U 6

Device type

QST = Capacitive touch sensor

Device sub-family

1: QTouch (3 to 5 V)

Channel count

Number of channels

Pin count

A: 8 pins

Package

U: QFN (dual quad flat no lead)

Temperature range

6: –40°C to +85°C

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

9 Device revision information

9.1 Device identification

Figure 20. Device revision identification

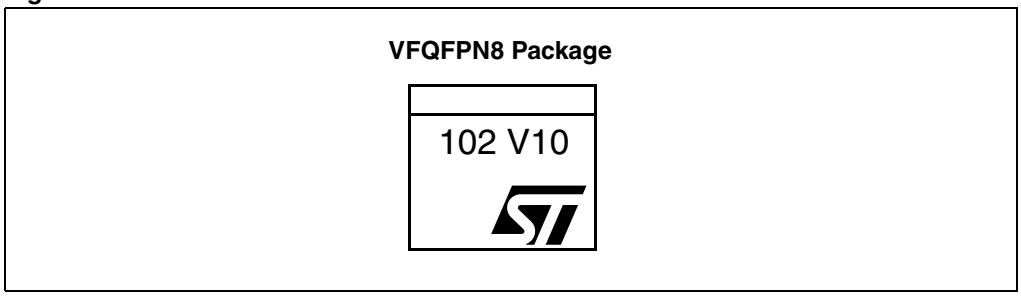


Table 22. Device revision identification

Marking	Device revision
V10	First revision

9.2 Device revision identification

The marking on the first line of the package top face identifies the device revision.

9.2.1 Revision 1.0

First device revision.

10 Revision history

Table 23. Document revision history

Date	Revision	Changes
20-Feb-2008	1	First release.

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