

# EMY1441HI

11.3 Gb/s Direct Modulation Driver IC for +3.3V Supplied Voltage



## 1. Abstract

- 1) Operation speed over 11.3Gb/s
- 2) Output Modulation Current:60mA (typ.,25ohm Load)
- 3) Power Supply Voltage : +3.3V
- 4) Duty Ratio Adjustable
- 5) Output Shutdown Control
- 6) Internal Input 50 ohm Termination
- 7) Modulation Current monitor / Bias Current Monitor
- 8) 4.0mm x 4.0mm 24-pin Hermetically Sealed Ceramic Package


## 2. Absolute Maximum Ratings

The semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings. The normal logic operation is not assured even within the ratings.

Table 2-1. Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	VDD	-0.5 to 7.0	V
Output Termination Voltage	VTT	-0.5 to 7.0	V
Input Voltage(Din,DinB)	VIN	-1.0 to 3.0	V
Power Supply Current	Iss	250	mA
Modulation Current Control Voltage	VIP	-1.0 to 5.0	V
Bias Current Control Voltage	VIB	-1.0 to 5.0	V
Duty Control Voltage	VDUTY	-1.0 to 5.0	V
Output Shut Down Control Voltage	VSD	-1.0 to 5.0	V
Output Voltage(Dout,DoutB,IBout)	Vout	-0.5 to 6.0	V
Storage Temperature	Tstg	-55 to 125	degC

Eudyna Device Inc. assumes customer's agreement on the notes in the last page for use of the information in this document.

	<p>This device contains Gallium Arsenide(GaAs).                  For safety, please observe the following:</p> <p>(1) Do not put devices in your mouth. Gallium Arsenide is dangerous if ingested.</p> <p>(2) Do not burn, crush, or process chemically. It is dangerous to inhale or ingest the gas, powder, or liquid which results from burning, crushing or chemical processing of the devices.</p> <p>(3) Discard devices separately from industrial and domestic wastes in accordance with the method specified by law.</p>
<p><b>GaAs</b></p> <p><b>CAUTION</b></p>	

**3. Recommended Operating Conditions**

The recommended operating conditions are the recommended values assuring normal operation and long term reliability.

Table 3-1. Recommended Operating Conditions

Parameter	Symbol	Condition	Limit			Unit
			Min.	Typ.	Max.	
Supply Voltage	VDD		3.07	3.3	3.47	V
Output Termination Voltage	VTT		4.65	5.0	5.25	V
Input Data Swing	VIND	Differential Input (AC coupled)	0.15	---	1.0	Vpp
Input Data Swing	VINS	Single-ended Input (AC coupled)	0.3	---	1.0	Vpp
Modulation Current Control Voltage	VIP		0	---	1.0	V
Bias Current Control Voltage	VIB		0	-	0.8	V
Output Shut down Control Voltage	VSDH		1.6	1.8	2.0	V
	VSDL		0	0.6	0.8	V
Duty Control Voltage	VDUTY		0.6	1.2	1.8	V
Case Temperature	TC		-10	---	85	degC

- Note a) Power on sequence: 1) VDD, 2) VTT, 3) VDUTY, VSD, 4) VIB, VIP  
 b) For operation with single-ended data input, a capacitor should be connected between Complimentary input and GND  
 c) External capacitors are necessary at data input terminals(Din,DinB) for DC blocking.

Table4-1. Electrical Characteristics (R<sub>L</sub>=25ohm)

Parameter	Symbol	Condition	Limit			Unit
			Min.	Typ.	Max.	
Maximum Data Rate	fb	NRZ	11.3	---	---	Gb/s
Power Supply Current	I <sub>DD</sub>	V <sub>IP</sub> =0.0V V <sub>IB</sub> =0.0V	60	100	120	mA
Maximum Modulation Current	I <sub>P</sub> MAX	V <sub>IP</sub> =1.0V, V <sub>IB</sub> =V <sub>SS</sub> V <sub>SD</sub> = 'L'	40	60	---	mA
Maximum Modulation Current @ T <sub>c</sub> =85degC	I <sub>P</sub> MAX85	V <sub>IP</sub> =1.0V, V <sub>IB</sub> =V <sub>SS</sub> V <sub>SD</sub> = 'L', T <sub>c</sub> =85degC	55	75	---	mA
Minimum Modulation Current	I <sub>P</sub> MIN	V <sub>IP</sub> =0.0V, V <sub>IB</sub> =0.0V V <sub>SD</sub> = 'L'	---	2.0	8.0	mA
Maximum Bias Current	I <sub>B</sub> MAX	V <sub>IB</sub> =0.8V V <sub>IP</sub> =0.0V V <sub>SD</sub> = 'L'	40	60	---	mA
Minimum Bias Current	I <sub>B</sub> MIN	V <sub>IB</sub> =0.0V V <sub>IP</sub> =0.0V V <sub>SD</sub> = 'L'	---	4.0	12.5	mA
Modulation Current Leakage (Shutdown)	I <sub>P</sub> sd	V <sub>IP</sub> =1.0V V <sub>SD</sub> = 'H'	---	4.0	7.0	mA
Bias Current Leakage (Shutdown)	I <sub>B</sub> sd	V <sub>IB</sub> =0.8V V <sub>SD</sub> = 'H'	---	2.0	3.0	mA
Rise Time	T <sub>r</sub>	fb=2.5Gb/s 1,0,1,0...Alternative Pattern 20 to 80 %	---	25	35	ps
Fall Time	T <sub>f</sub>	V <sub>IP</sub> =1.0V V <sub>SD</sub> = 'L'	---	25	35	ps
Crossing Adjustment Range	CRSmin	fb=11.3Gb/s, NRZ PRBS 2 <sup>31</sup> -1 V <sub>IND</sub> =0.5V <sub>pp</sub>	---	---	40	%
	CRSmax	Input Crossing Point:50% V <sub>IP</sub> =1.0V V <sub>SD</sub> = 'L'	60	---	---	%
Jitter RMS	Jitter	fb=11.3Gb/s, NRZ PRBS 2 <sup>31</sup> -1 V <sub>IND</sub> =0.5V <sub>pp</sub> Input Crossing Point:50% Output Crossing Point:50% V <sub>IP</sub> =1.0V V <sub>SD</sub> = 'L'	---	2.5	3.5	ps

### 5. Block Diagram

Figure 5-1. Block Diagram

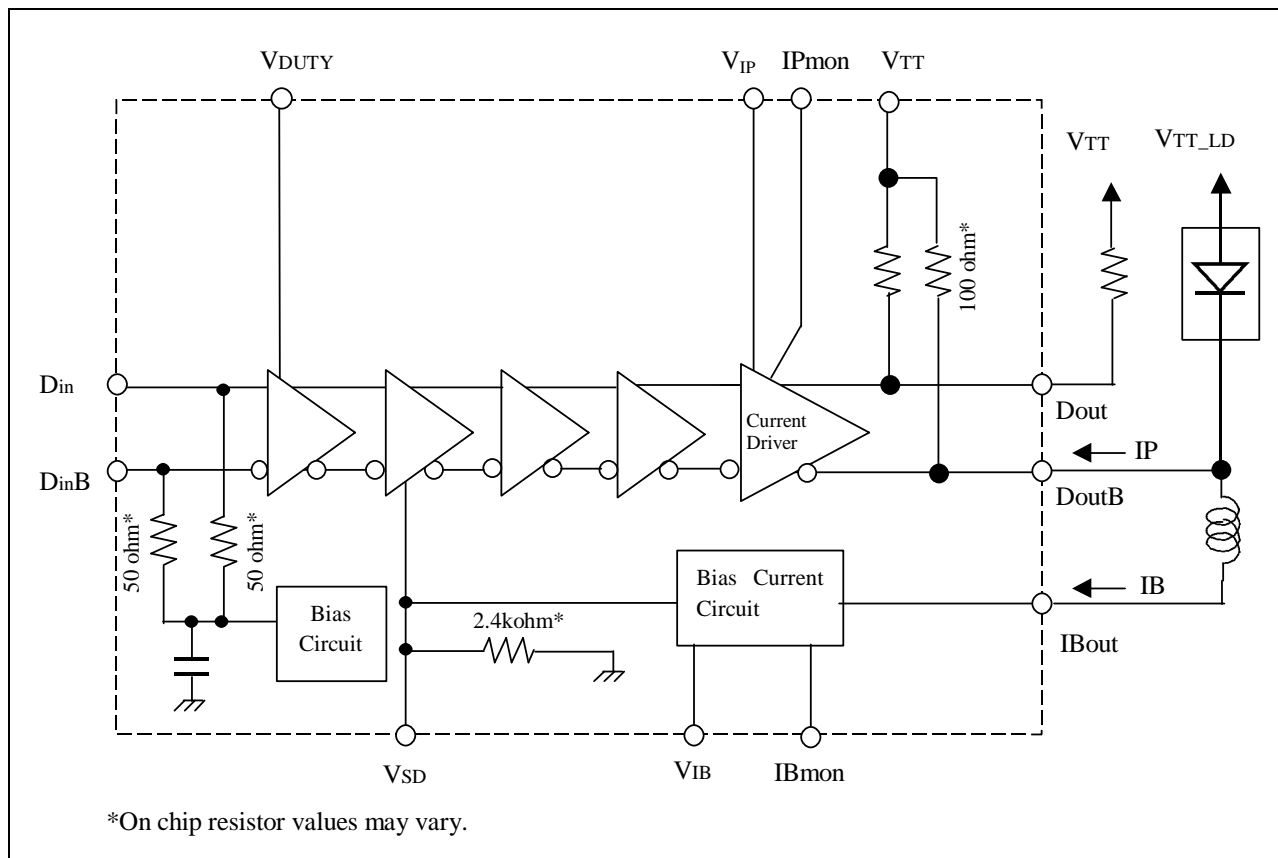


Table 5-1 Truth Table of Data I/O \*Note 1)

Din	DinB	Dout	DoutB	Optical output from DM-LD at Dout	Optical output from DM-LD at DoutB
L	H	L	H	ON	OFF
H	L	H	L	OFF	ON

Note 1) DM-LD connection at cathode with the IC.

Table 5-2 Truth Table of Shutdown Function

VSD	Modulation Current	Bias Current
L or Open	Enabled	Enabled
H	Disabled *Note 2)	Disabled

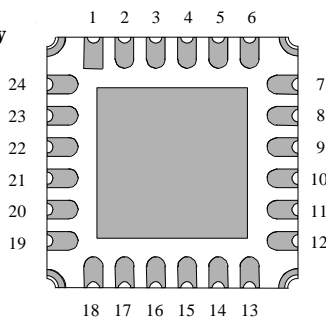
Note 2) DoutB is fixed at H (Optical output OFF) and Dout is fixed at L (Optical output ON).

### 6. Pin Description

Table 7-1 Pin Description

Pin Number	Symbol	I/O	Function	Remarks
1	GND		GND	
2	Din	I	Data Input	
3	GND		GND	
4	GND		GND	
5	DinB	I	Complementary Data Input	
6	GND		GND	
7	VSD	I	Shut Down Control Voltage	
8	VDD	---	Supply Voltage	
9	VTT	---	Termination Voltage	
10	GND		GND	
11	GND		GND	
12	IBmon	O	Bias Current Monitor Output Voltage	
13	IBout	O	Bias Current Output	
14	DoutB	O	Complementary Data Output	
15	GND		GND	
16	GND		GND	
17	Dout	O	Data Output	
18	VTT	---	Termination Voltage	
19	IPmon	O	Modulation Current Monitor Output Voltage	
20	VIB	I	Bias Current Control Voltage	
21	GND		GND	
22	VIP	I	Modulation Current Control Voltage	
23	VDD	---	Supply Voltage	
24	VDUTY	I	Duty Control(Cross Point Control)	

Bottom View



### 7. Package

Fig.7-1 Package Outline

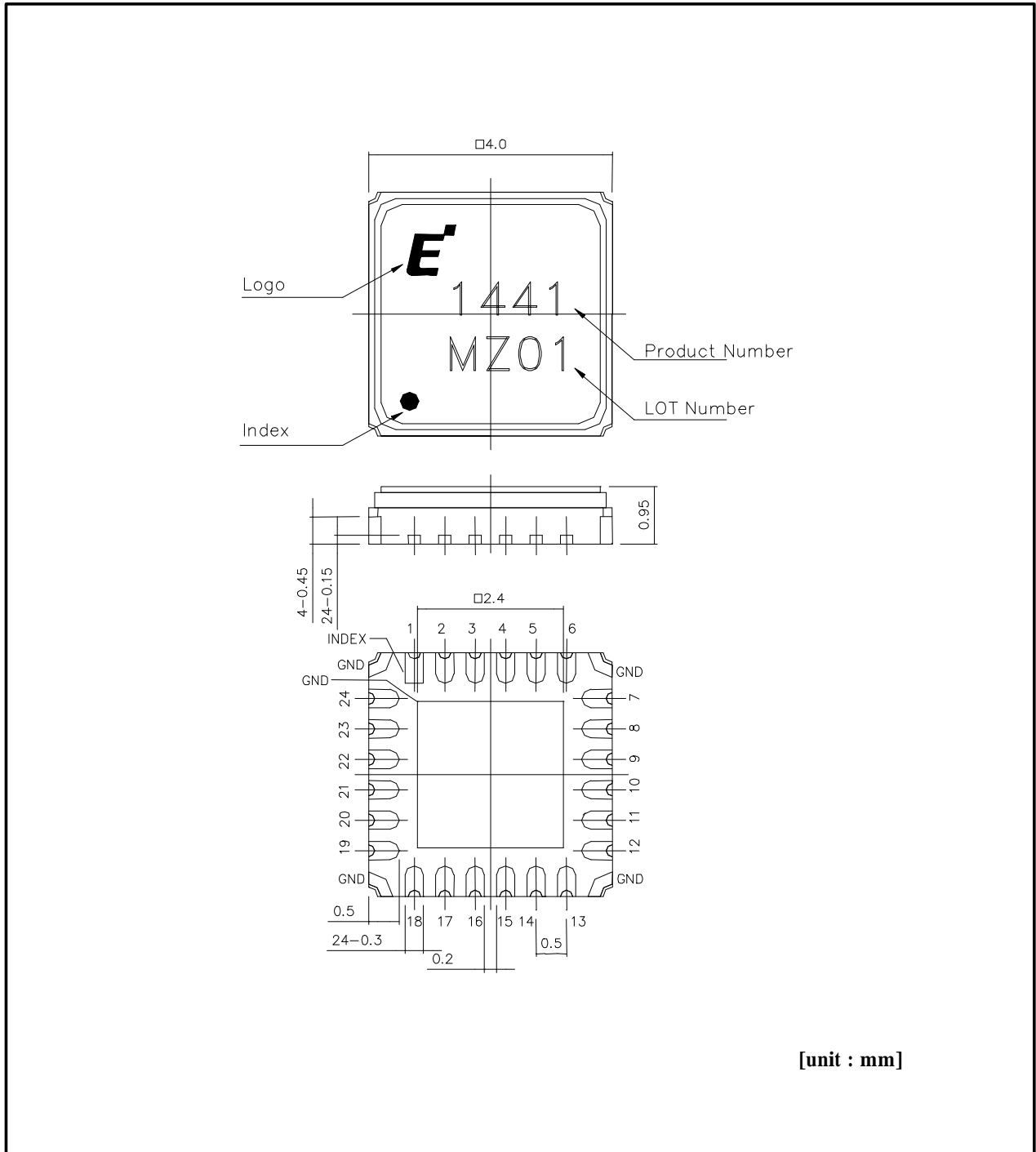
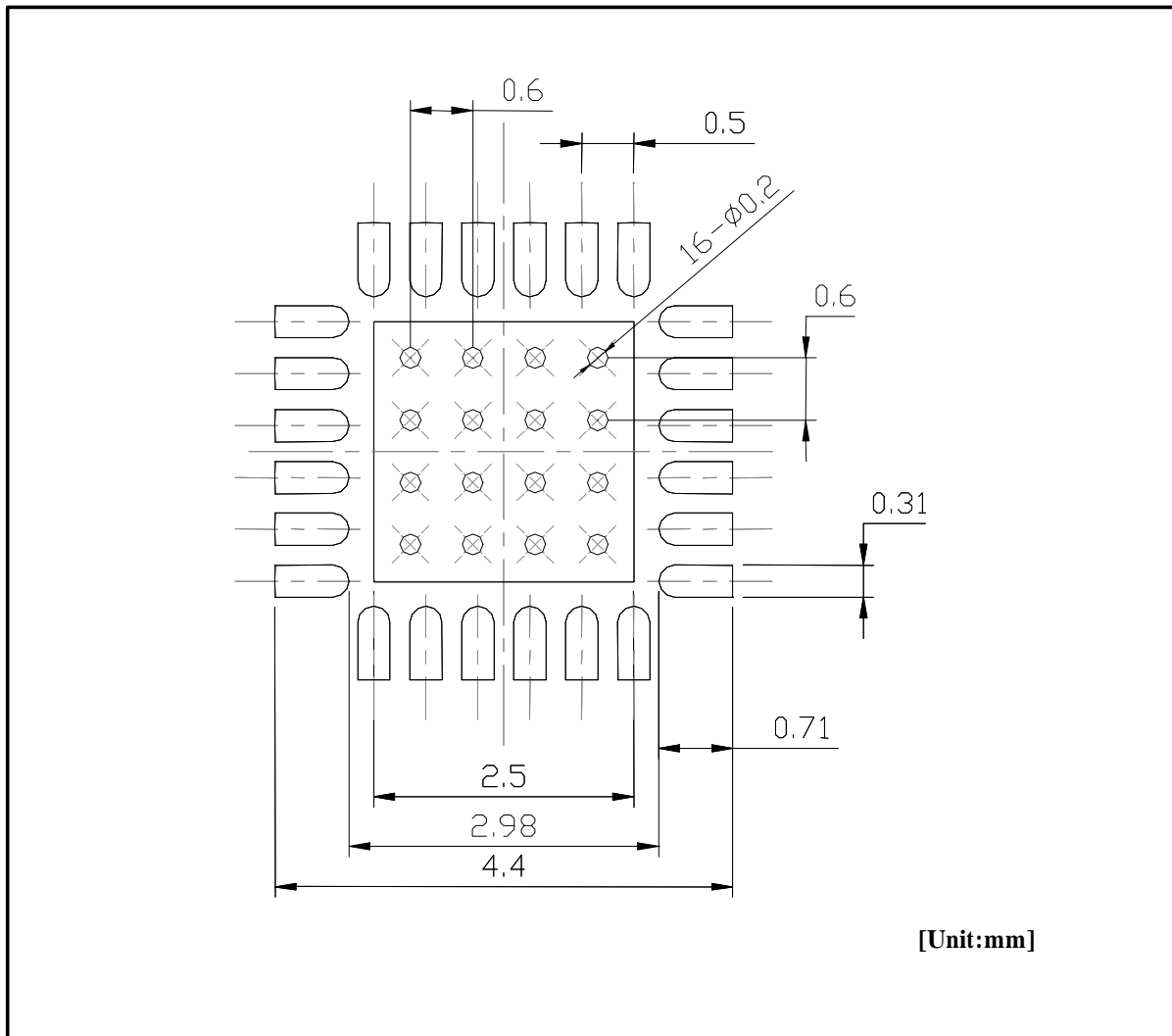
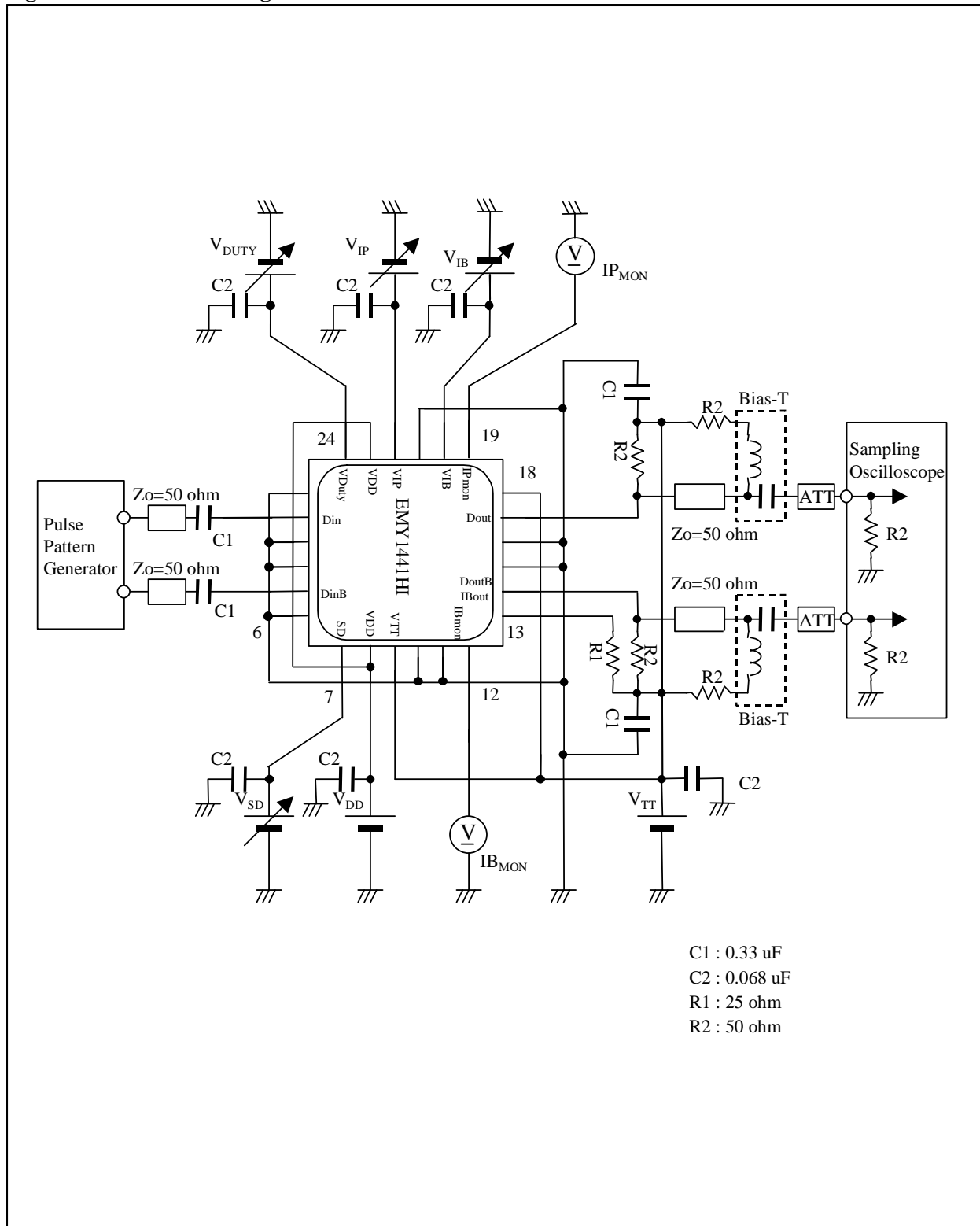


Figure 7-2 Recommended Footprint for HI Package



8. Test Circuit

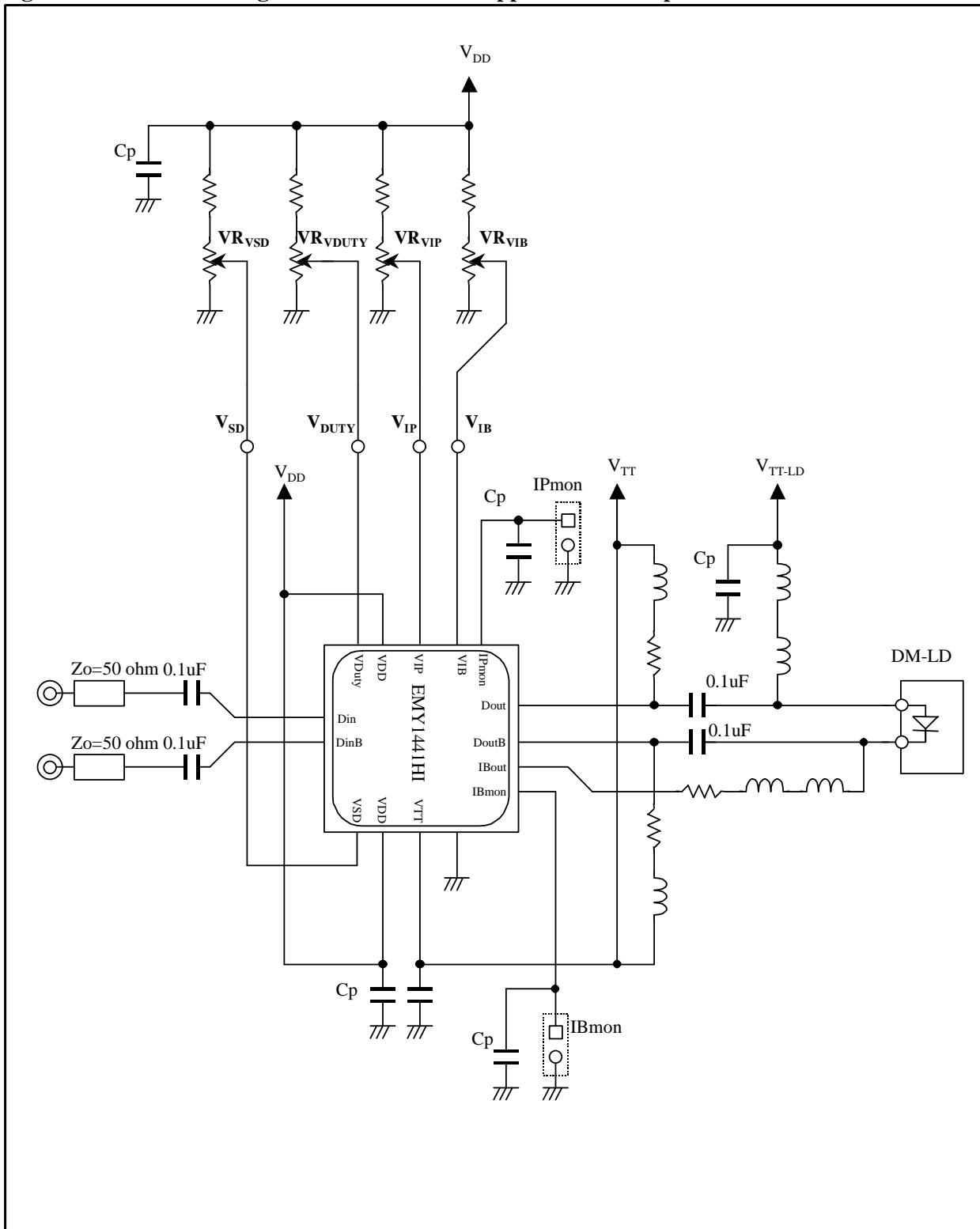
Figure 8-1 Schematic Diagram of Test Circuit for EMY1441HI





9. Application Reference

Figure 9-1 Schematic Diagram of EMY1441HI Application Example

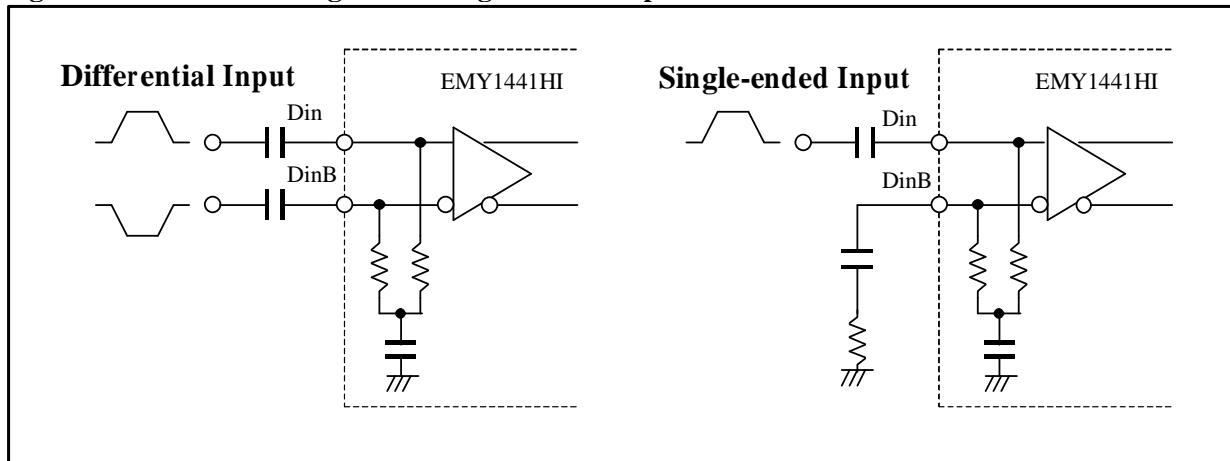


### 9.1. Input RF Signal

There are 50ohm termination resistors to ground on EMY1441HI die. The input RF signal must be fed into the IC through 50ohm lines with DC block capacitors. The IC operates with either differential or single-ended input signal. For operation with single-ended input, the unused input pin should be connected to ground with a capacitor for better stability in internally generated reference voltage.

Schematic diagram of the differential and single-ended input circuit is shown in Figure 9-2.

Figure 9-2 Schematic Diagram of Single-Ended Input Circuit



### 9.2. DM-LD Drive and Output Circuit

It is recommended to connect DoutB from EMY1441HI to cathode pin of a DM-LD, when shutdown function of the IC should be used in the system. Anode pin of the DM-LD should be connected to  $V_{TT}$ , together with Dout load resistor and back-termination resistors in the IC. The RF signal line should be impedance-controlled. Design for complementary signal termination is important for good optical performance, as well as the signal line design for DM-LD.

When IBout terminal is not used, IBout should be connected to  $V_{TT}$  through load resistor.

### 9.3. RF Signal Line Design

Low loss material for PCB must be used for good signal quality. Careful designs must be taken for the layout, such as bends, land patterns, via-holes, etc., in order to minimize impedance discontinuity that may degrade the waveforms. It is recommended to make physically and electrically symmetric design for differential RF signal line at both input and output, as much as possible.

### 9.4. Bias De-coupling

It is recommended to have bypass capacitors for power supply and DC control voltage pins. Having two or more different capacitors (for example, ranging from some  $10^{-11}$  to  $10^{-6}$  farads) at each node will be effective to obtain a good de-coupling over wide frequency range.

## 9.5. Power Supply Sequence

It is recommended to follow the power supply sequence to avoid damaging the IC.

1. Set  $V_{DUTY}$ ,  $V_{IP}$ ,  $V_{IB}$  and  $V_{SD}$  to ground, increase or turn on  $V_{DD}$ , then  $V_{TT}$ .
2. Adjust  $V_{IP}$ ,  $V_{IB}$  and  $V_{DUTY}$  for desired output waveforms.
3. Return  $V_{DUTY}$ ,  $V_{IP}$ ,  $V_{IB}$  and  $V_{SD}$  to ground, then decrease or turn off  $V_{TT}$ , then  $V_{DD}$ .

Such care may not be necessary when the control circuit for  $V_{DUTY}$ ,  $V_{IP}$ ,  $V_{IB}$ , and  $V_{SD}$  are designed properly to generate the voltage within the absolute maximum ratings for each pin.

## 9.6. Modulation Current Monitoring

There is a resistor,  $R_{IP}$  (1ohm Typ.) between  $IP_{MON}$  pin and ground of in EMY1441HI for monitoring total modulation current,  $IP$ , as a voltage drop across  $R_{IP}$ .

$$IP = IP_{BT} + IP_{LD} = V_{IPMON} / R_{IP} = V_{IPMON} \quad (9-1a)$$

$$IP_{LD} = IP \cdot R_{BT} / (R_{LD} + R_{BT}) \quad (9-1b)$$

$$IP_{BT} = IP \cdot R_{LD} / (R_{LD} + R_{BT}) \quad (9-1c)$$

The modulation current includes the current through back termination resistor and LD. The relationship between  $V_{IMOD}$  and  $I_{IP}$  is shown in Figure 10-13.

## 9.7. Bias Current Monitoring

There is a resistor,  $R_{IB}$  (1ohm Typ.) between  $IB_{MON}$  pin and ground of in EMY1441HI for monitoring modulation current,  $IB$ , as a voltage drop across  $R_{IB}$ . The relationship between  $I_B$  and  $V_{IB}$  is shown in Figure 10-14.

$$IB = V_{IBMON} / R_{IB} = V_{IBMON} \quad (9-2)$$

## 9.8. Power Dissipation

Power dissipation of EMY1441HI can be estimated with the equations from 9-4a to 9-4f, with current flow shown in Figure 9-2 and voltage swing at input,  $V_{IN}$ , and output,  $V_{OUT}$ .

$$P_D = P_{IN} + P_{DD} + P_{IP} + P_{IB} - P_{OUT} \quad (9-4a)$$

$$P_{IN} = 0.5 V_{IN}^2 / R_I = V_{IN}^2 / 100 \quad (9-4b)$$

$$P_{DD} = V_{DD} \cdot I_{DD} \quad (9-4c)$$

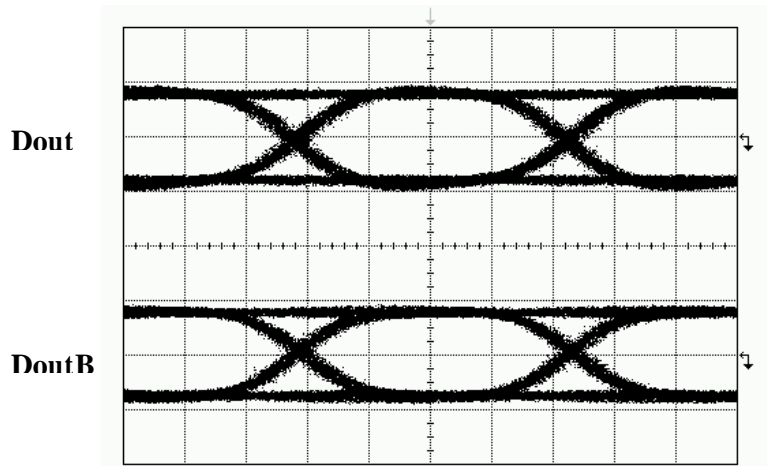
$$P_{IP} = V_{TT} \cdot IP \quad (9-4d)$$

$$P_{IB} = V_{TT} \cdot IB \quad (9-4e)$$

$$P_{OUT} = IP_{LD}^2 \cdot R_{LD} + IB^2 \cdot R_{LD} \quad (9-4f)$$

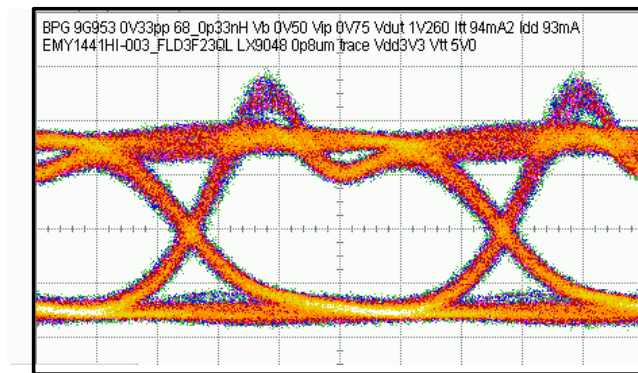
## 9.9. Thermal Design

The EMY1441HI die is attached to the heat sink at the bottom of the package (face up). Proper design of heat transfer path (Ex. thermal VIA) from the heat sink to module base plate or outside of the system should be taken to keep the IC case temperature,  $T_C$ , within the recommended operating conditions for normal operation and long term reliability.



$T_c=25\text{degC}$ ,  $V_{DD} = 3.3\text{V}$ ,  $V_{TT} = 5.0\text{V}$ ,  $V_{IP}=1.0\text{V}$ ,  $V_{IB}=0.0\text{V}$   
 $V_{DUTY}=1.2\text{V}$ ,  $V_{SD} = 0.6\text{V}$ ,  $D_{IN}/D_{INB}=0.5\text{Vpp}$   
 11.3Gb/s, PRBS  $2^{31} - 1$ ,  $R_L=25\ \text{ohm}$

Figure 10-1 Electrical Waveforms (H:20ps/div.,V:1.0V/div.)



$T_c=25\text{degC}$ ,  $V_{DD} = 3.3\text{V}$ ,  $V_{TT} = 5.0\text{V}$ ,  $V_{DUTY}=1.26\text{V}$ ,  $V_{SD} = 0.6\text{V}$ ,  $D_{IN}/D_{INB}=0.5\text{Vpp}$   
 10.0Gb/s, PRBS  $2^{31} - 1$ , Extinction Ratio=7.7dB, Average Power=0.25dBm  
 LD:FLD5F23QL(Eudyna)

Figure 10-2 Optical Waveforms without filter at back to back (H:20ps/div.)

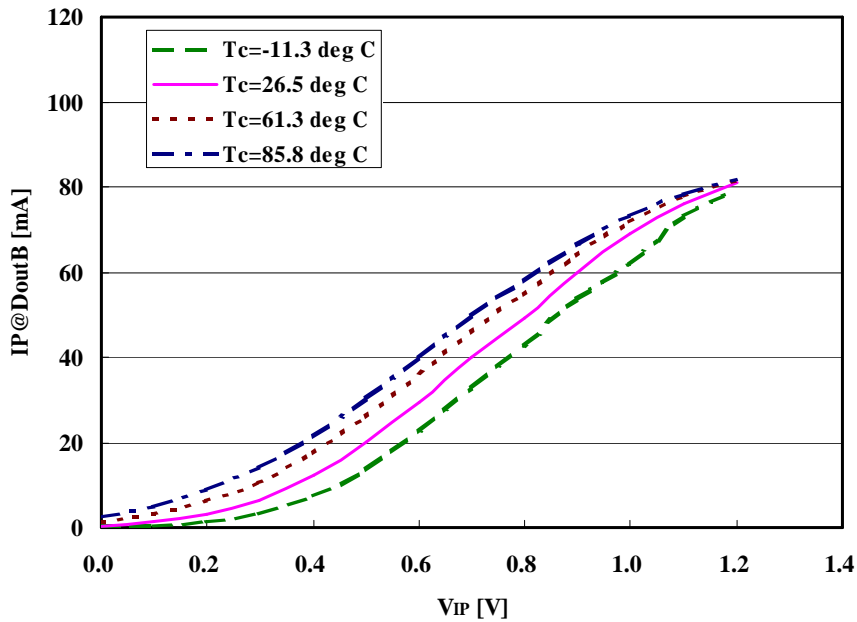


Figure 10-3 Modulation Current ( $I_P$ ) vs. Control Voltage ( $V_{IP}$ ) Relationship  
( $V_{DD}=3.3V$ ,  $V_{TT}=5.0V$ ,  $T_c$  dependency)

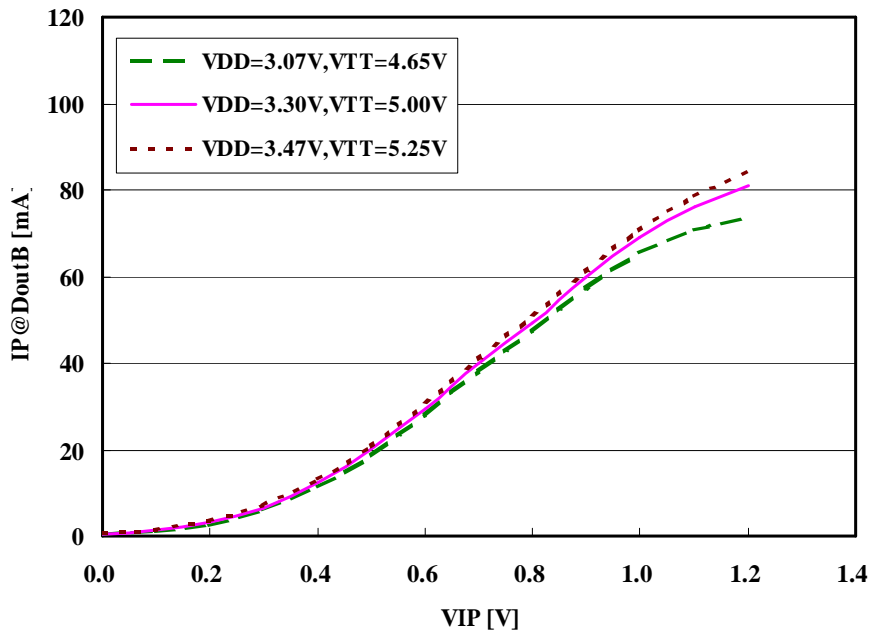


Figure 10-4 Modulation Current ( $I_P$ ) vs. Control Voltage ( $V_{IP}$ ) Relationship  
( $T_c=25degC$ ,  $V_{DD}/V_{TT}$  dependency)

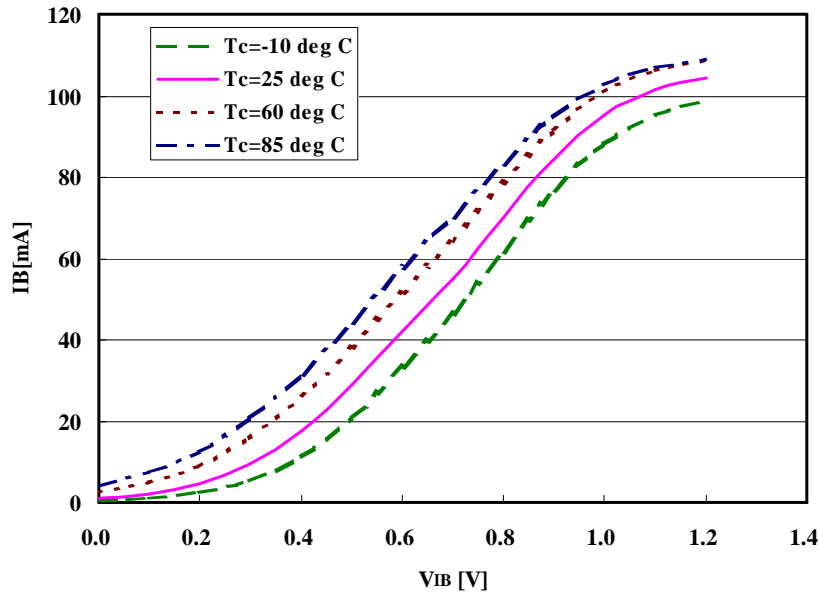


Figure 10-5 Bias Current ( $I_B$ ) vs. Control Voltage(  $V_{IB}$  ) Relationship  
( $V_{DD}=3.3V$ ,  $V_{TT}=5.0V$  Tc dependency)

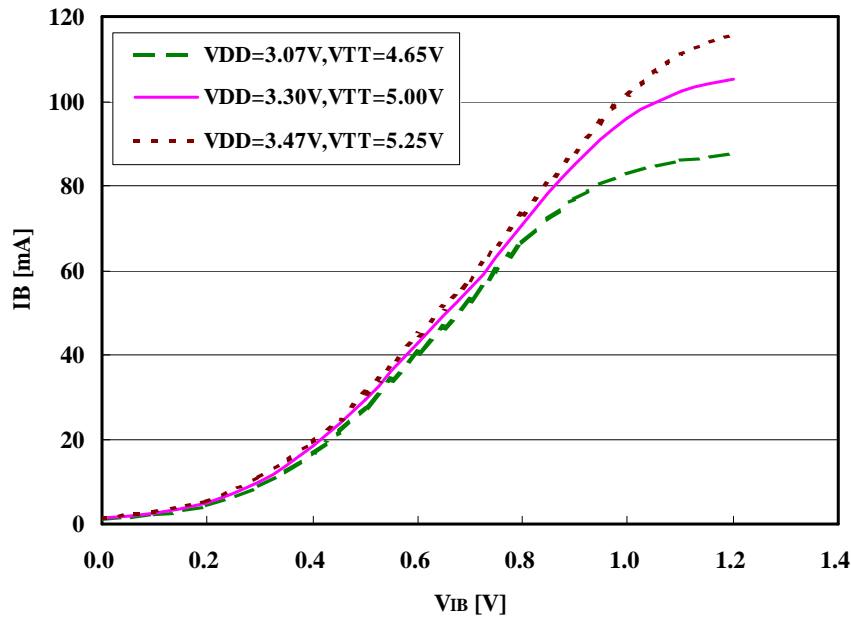
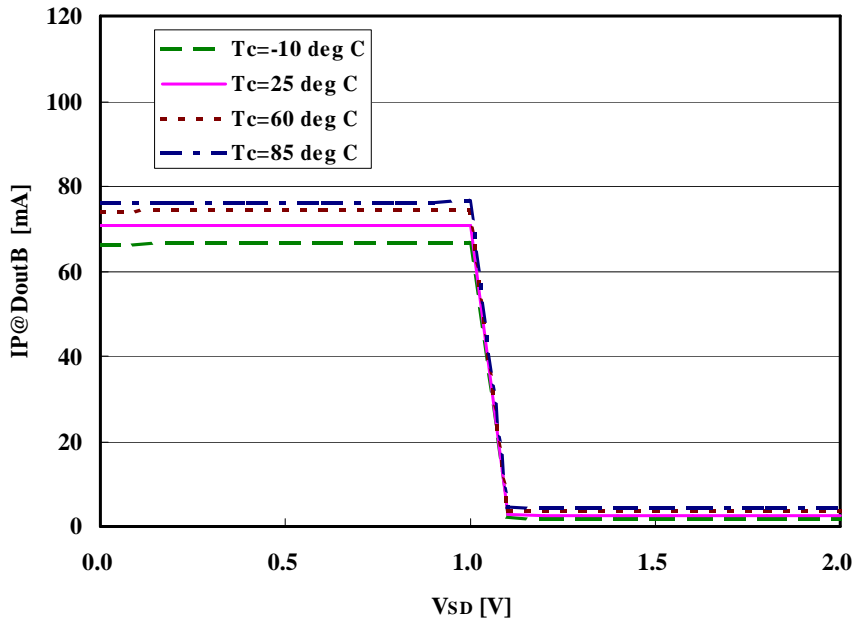
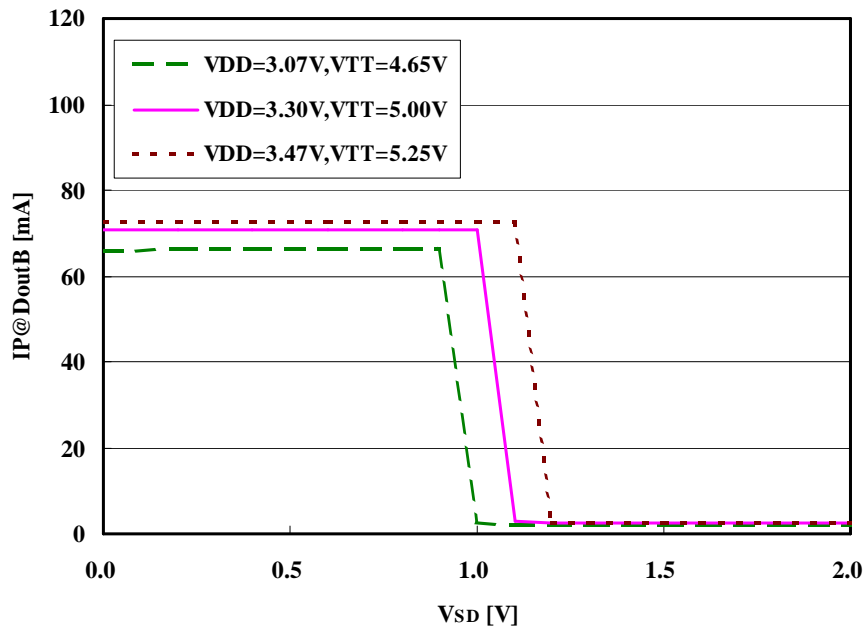


Figure 10-6 Bias Current ( $I_B$ ) vs. Control Voltage(  $V_{IB}$  ) Relationship  
( $T_c=25\text{degC}$ ,  $V_{DD}/V_{TT}$  dependency)



**Figure 10-7 Modulation Current(IP) vs. Shutdown Control Voltage( $V_{SD}$ ) Relationship**  
 ( $V_{DD}=3.3V$ ,  $V_{TT}=5.0V$ ,  $V_{IP}=1.0V$ ,  $T_c$  dependency)



**Figure 10-8 Modulation Current(IP) vs. Shutdown Control Voltage( $V_{SD}$ ) Relationship**  
 ( $T_c = 25deg$ ,  $V_{IP}=1.0V$ ,  $V_{DD}/V_{TT}$  dependency)

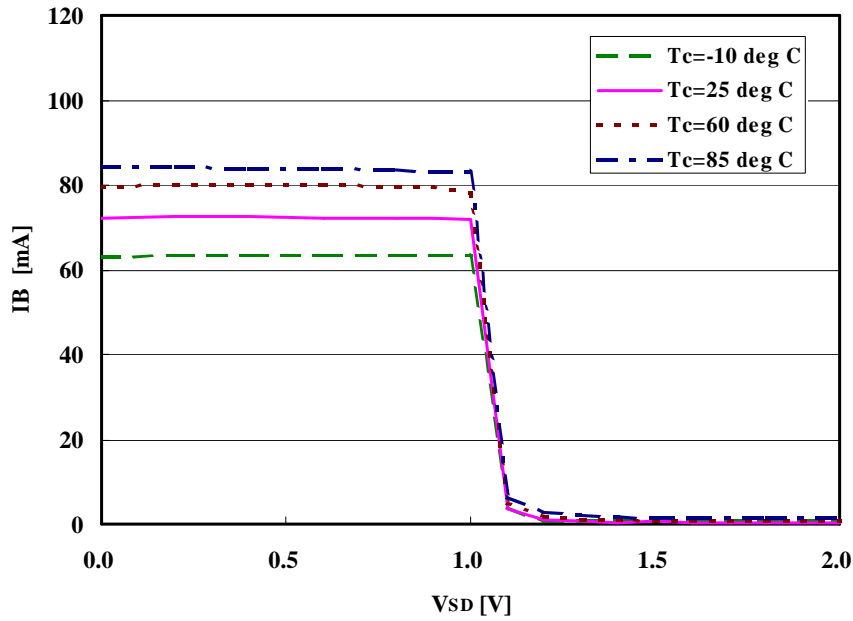


Figure 10-9 Bias Current(IB) vs. Shutdown Control Voltage( $V_{SD}$ ) Relationship ( $V_{DD}=3.3V$ ,  $V_{TT}=5.0V$ ,  $V_{IP}=1.0V$ ,  $T_c$  dependency)

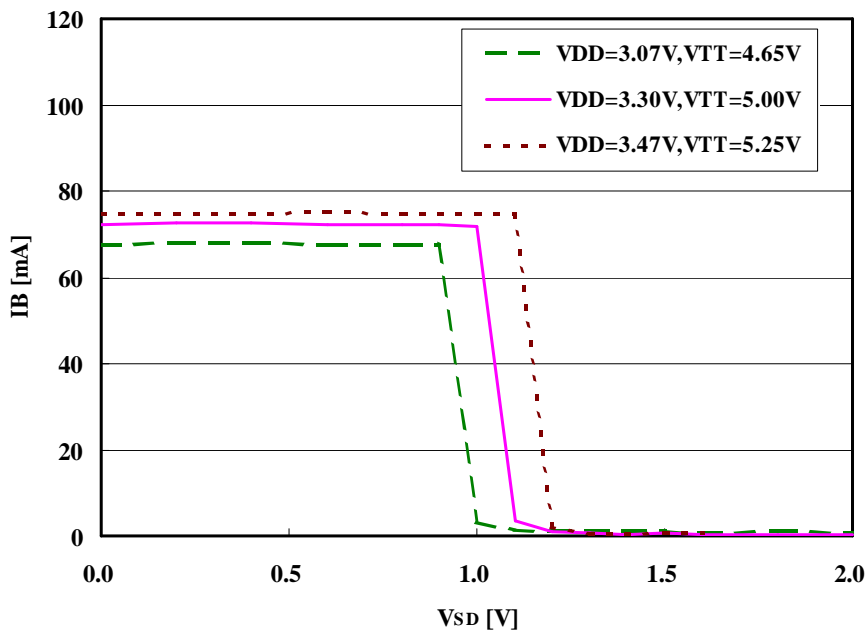
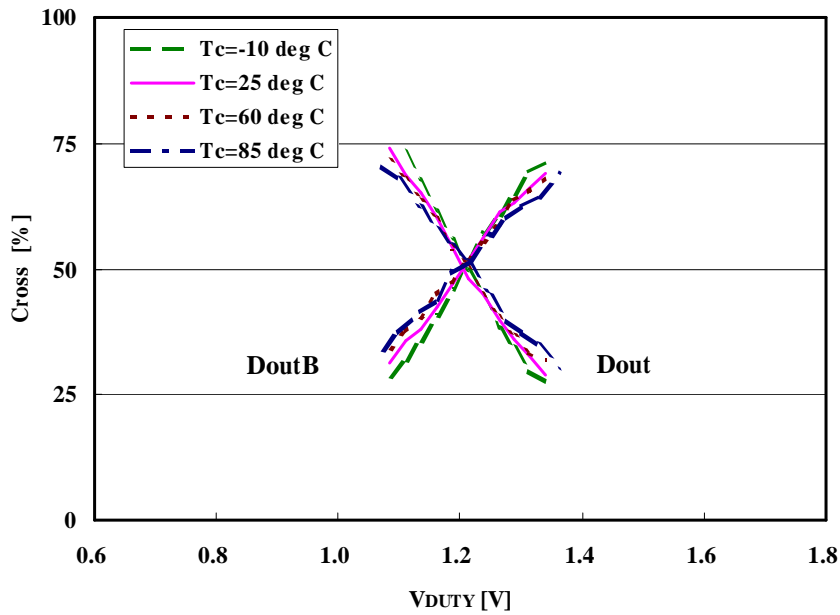
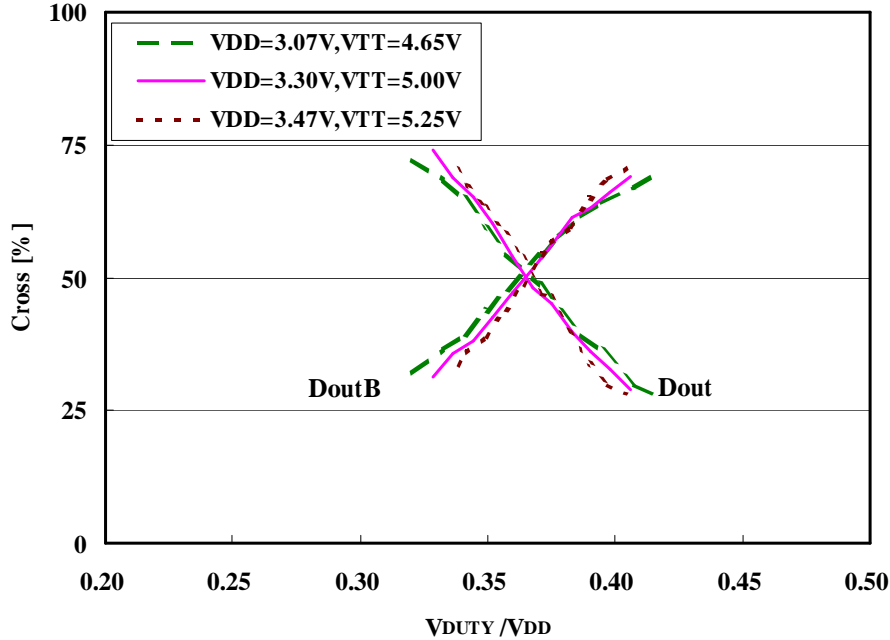


Figure 10-10 Bias Current(IB) vs. Shutdown Control Voltage( $V_{SD}$ ) Relationship ( $T_c = 25\text{deg}$ ,  $V_{IP}=1.0V$ ,  $V_{DD}/V_{TT}$  dependency)

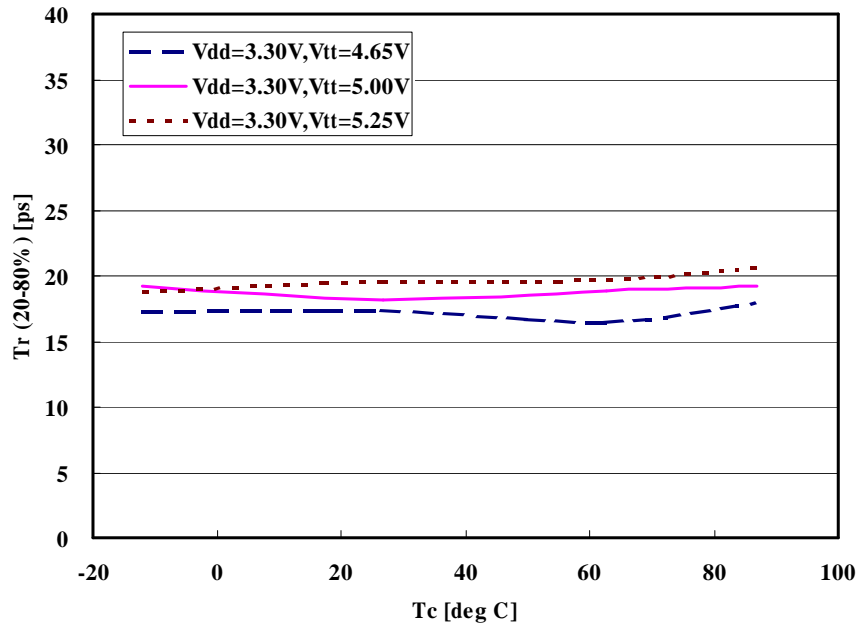




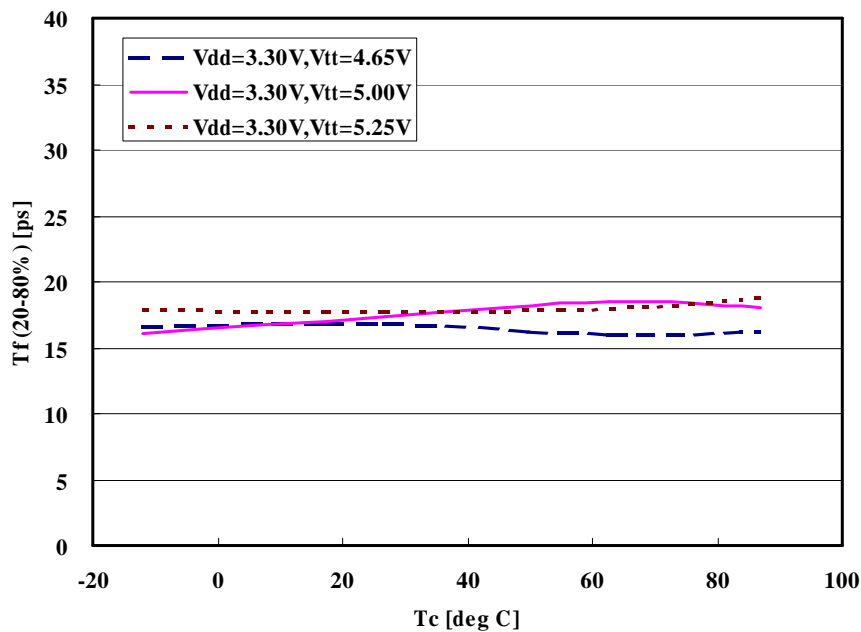
**Figure 10-11 Cross Point vs. Duty Control Voltage (VDUTY) Relationship**  
 (Tc =25deg, VIP=1.0V, VDD/VTT dependency)



**Figure 10-12 Cross Point vs. Duty Control Voltage (VDUTY / VDD) Relationship**  
 (Tc =25deg, VIP=1.0V, VDD/VTT dependency)



**Figure 10-13 Rise Time( $T_r$ ) vs. Case Temperature ( $T_C$ ) Relationship**  
 ( $T_c = 25\text{deg}$ ,  $V_{IP} = 1.0\text{V}$ ,  $V_{DD}/V_{TT}$  dependency)



**Figure 10-14 Fall Time ( $T_f$ ) vs. Case Temperature ( $T_C$ ) Relationship**  
 ( $T_c = 25\text{deg}$ ,  $V_{IP} = 1.0\text{V}$ ,  $V_{DD}/V_{TT}$  dependency)

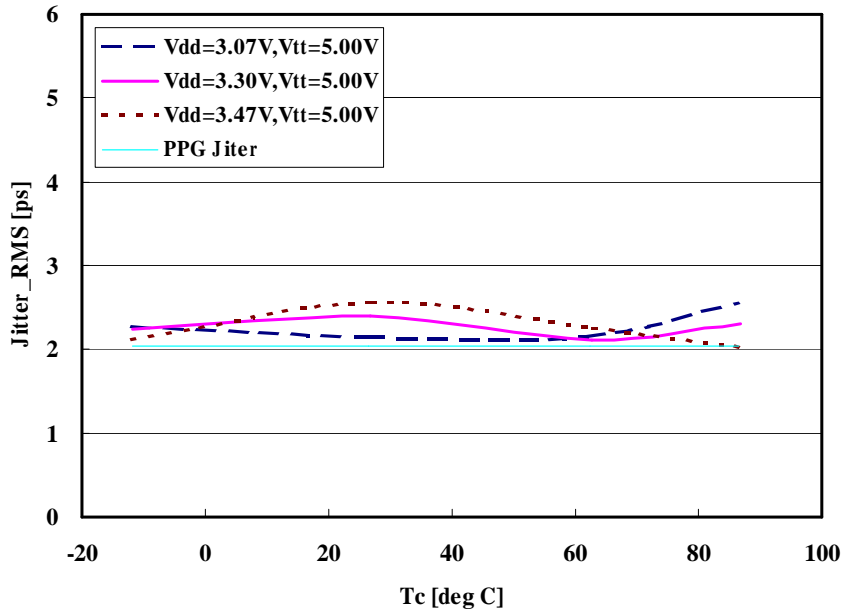


Figure 10-15 Jitter\_RMS vs. Case Temperature (T<sub>C</sub>) Relationship  
(T<sub>C</sub> =25deg, V<sub>IP</sub>=1.0V, V<sub>DD</sub>/V<sub>TT</sub> dependency)

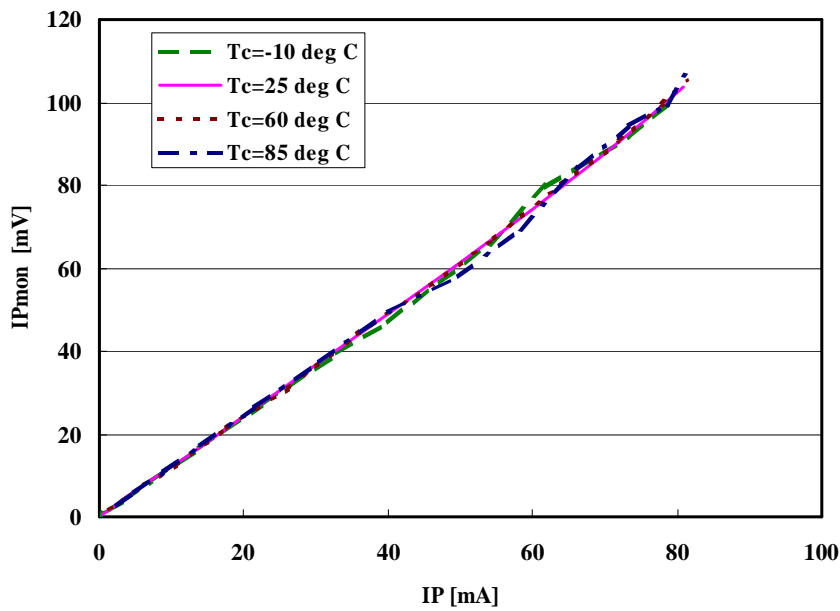


Figure 10-16 Modulation Current monitor Voltage(IPmon) vs. Modulation Current(IP)Relationship  
(V<sub>DD</sub>=3.3V, V<sub>TT</sub>=5.0V, T<sub>C</sub> dependency)

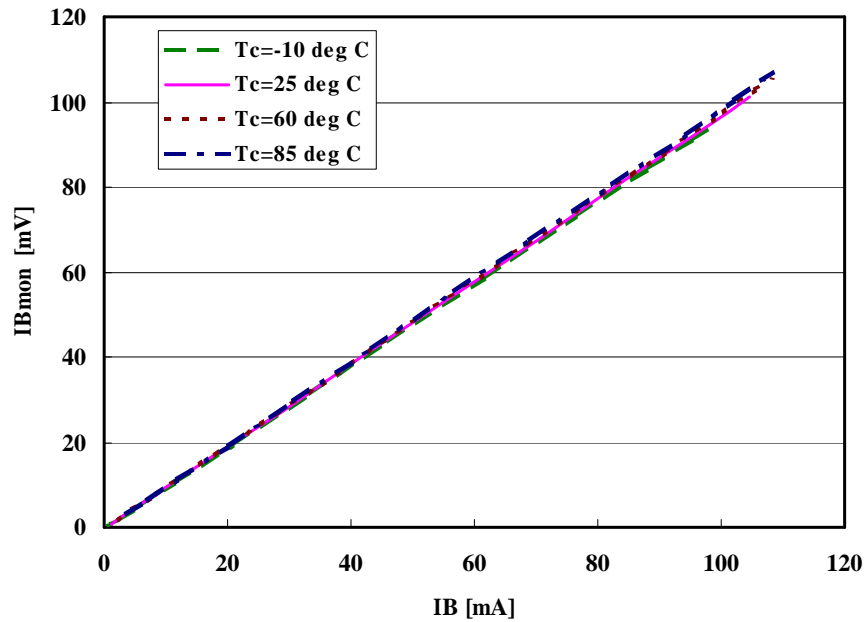


Figure 10-17 Bias Current Monitor Voltage (IBmon) vs. Bias Current (IBout) Relationship (V<sub>DD</sub>=3.3V, V<sub>TT</sub>=5.0V, Tc dependency)

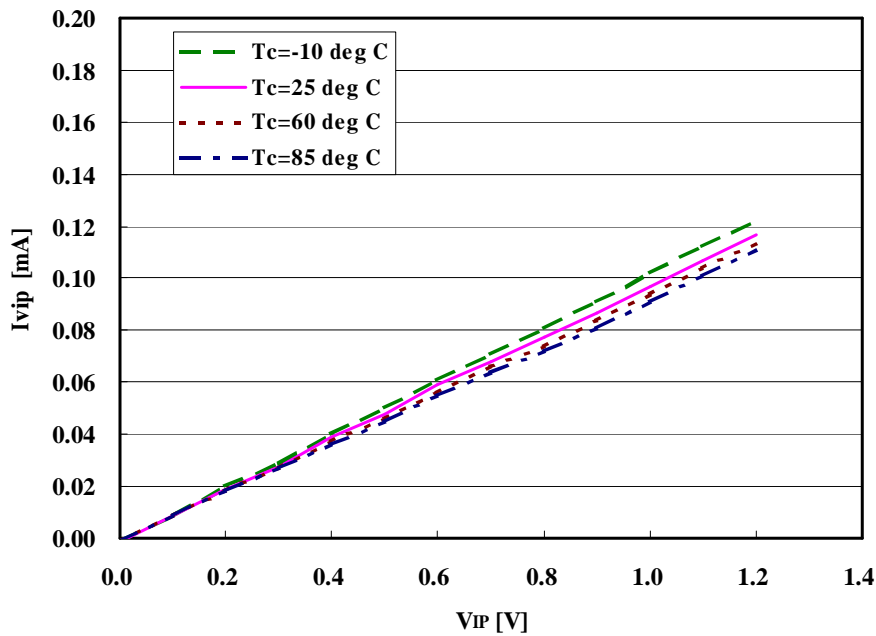


Figure 10-18 V<sub>IP</sub> Terminal Current (I<sub>VIP</sub>) vs. Control Voltage (V<sub>IP</sub>) Relationship (V<sub>DD</sub>=3.3V, V<sub>TT</sub>=5.0V, V<sub>IP</sub>=1.0V, Tc dependency)

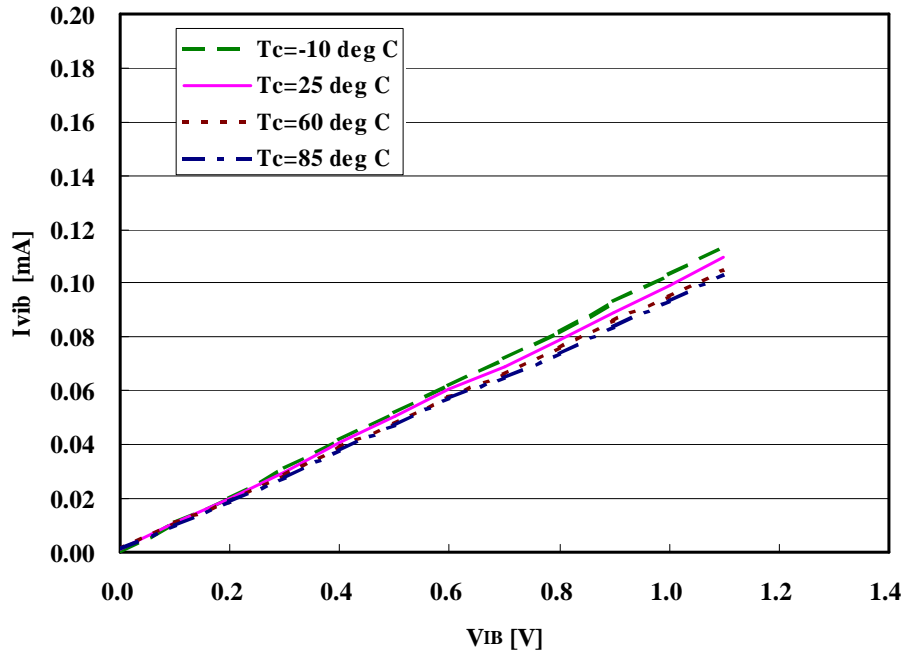


Figure 10-19  $V_{IB}$  Terminal Voltage ( $I_{VIB}$ ) vs. Control Voltage( $V_{IB}$ ) Relationship (Tc dependency)

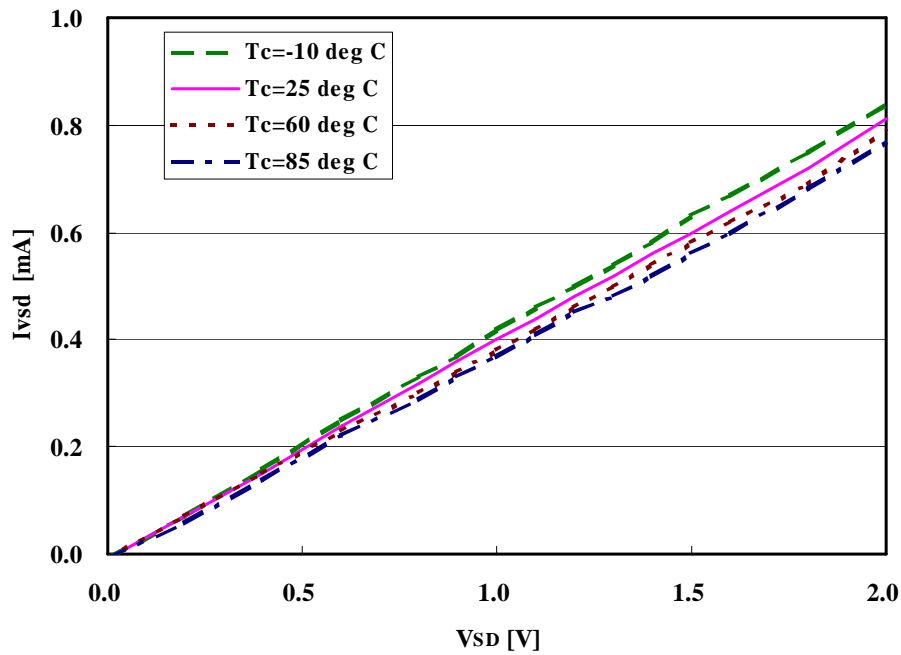


Figure 10-20  $V_{SD}$  Terminal Current ( $I_{SD}$ ) vs. Control Voltage( $V_{SD}$ ) Relationship (Tc dependency)

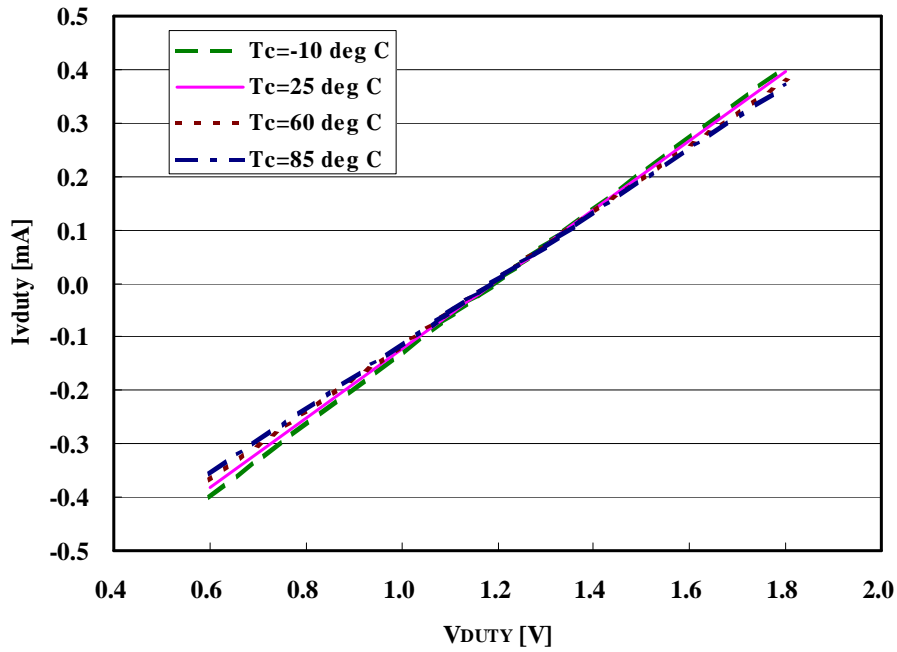


Figure 10-21 V<sub>VDUTY</sub> Terminal Current (I<sub>VDUTY</sub>) vs. Control Voltage (V<sub>VDUTY</sub>) Relationship (T<sub>c</sub> dependency)

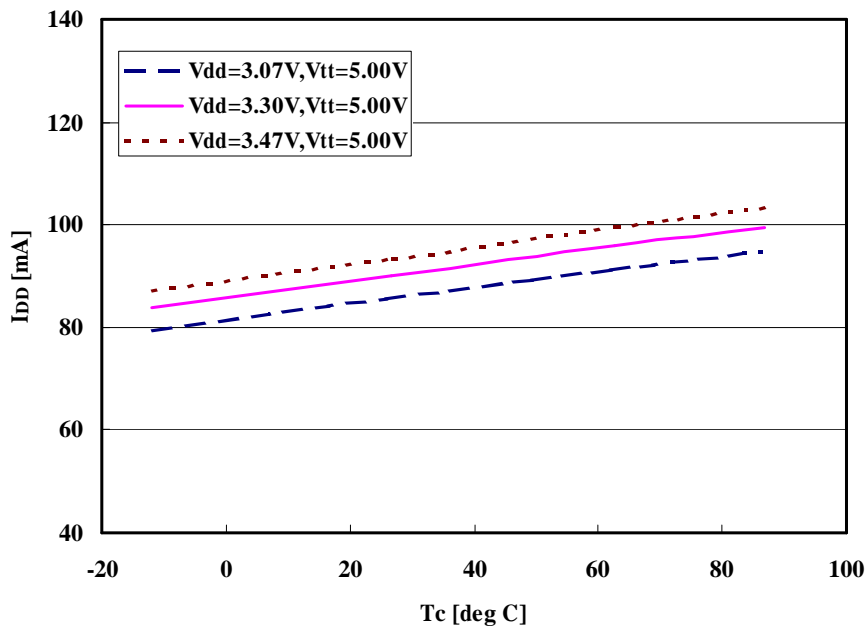


Figure 10-22 Power Supply Current (I<sub>DD</sub>) vs. Case Temperature (T<sub>c</sub>) Relationship (V<sub>IP</sub>=0.0V, V<sub>IB</sub>=0.0V)

Notice:

1) This document contains preliminary information on new products. The specification is subject to change without notice.

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