

Data Sheet

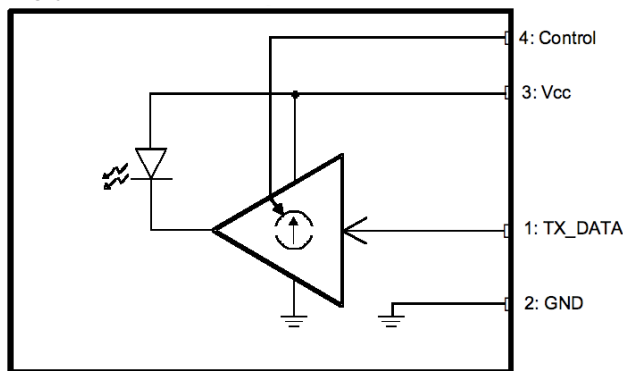
Description

The MOST Tx Plastic Fiber Optic Transmitter is a highly integrated CMOS IC combined with a High speed LED designed to transmit up to 25Mbit/sec optical data which is biphase coded at up to 50Mbaud.

The internal peaking circuit minimizes PWD.

The current through the LED will be setup by an external resistor connected to VCC. This makes it possible to control the optical output power of the LED.

MIT3 02



Actual design status:

IC Revision	package type	device marking
J	CAI	date code, MIT3 02

Features

Excellent solution for converting high speed data from TTL to Plastic Optical Fiber (POF)

- High speed transmitter up to 50 Mbaud
- TTL Data Input (Logic to Light Function)
- 650 nm for working in a low attenuation range of PMMA Fiber
- High coupled power in 1000 micron plastic fiber
- Low cost

Applications

- Optical Transmitter for MOST Systems

Safety Hints

Applications of new chip technologies leads to increasing optical efficiency and growing and higher levels of optical performance. We therefore recommend that the current versions of the IEC 825-1 and EN 60825-1 standards are taken into account right from the outset, i.e. at the equipment development stage, and that suitable protection facilities are provided.

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	T_{STG}	-40	100	°C
Junction Temperature	T_J	-40	100	°C
Soldering Temperature (>2.5 mm from case bottom $t \leq 5s$)	T_S	-	235	°C
Power Dissipation	P_{TOT}	-	300	mW
Power Supply Voltage	V_{CCMax}	-0.5	6.0	V

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.75	5.25	V
Operating Temperature Range ($R_{ext} = 13.5 \text{ k}\Omega$)	T_A	-40	85	°C

All the data in this specification refers to the operating conditions above unless otherwise stated.

Optical Signal Characteristics

(22.5 Mbit/s MOST Data, $V_{CC} = 4.75 \dots 5.25 \text{ V}$)

Parameter	Symbol	Min	Typ	Max	Unit
Peak wavelength at $T_A = 25^\circ\text{C}$	λ_{Peak25}	640	650	660	nm
Temperature coefficient λ_{Peak}	TC_{λ}	-	0.16	-	nm/K
Peak wavelength at $T_A = -40 \dots 85^\circ\text{C}$	λ_{Peak}	630	650	670	nm
Spectral bandwidth (FWHM)	Delta λ	-	20	30	nm
Average Output Power coupled into plastic fiber at $T_A = 25^\circ\text{C}$, $R_{ext} = 15 \text{ k}\Omega$ [1]	$P_{opt25,0}$	-7.4 (185)	-5.2 (300)	-3.6 (435)	dBm (μW)
Temperature coefficient P_{opt}	TC_{Popt}	-	-0.4	-	%/K
Average Output Power coupled into plastic fiber at $T_A = -40 \dots 85^\circ\text{C}$, $R_{ext} = 15 \text{ k}\Omega$ [1]	P_{opt}	-8.6 (140)	-5.2 (300)	-3.1 (490)	dBm (μW)
Average Output Power coupled into plastic fiber at $T_A = -40 \dots 85^\circ\text{C}$, $R_{ext} = 15 \text{ k}\Omega$, over lifetime [1]	$P_{opt, lifetime}$	-9.6 (110)	-5.2 (300)	-2.1 (615)	dBm (μW)
Gain in P_{opt} when using 13.5 k Ω instead of 15 k Ω		0.35	0.4	0.45	dB
Optical Rise Time (20% - 80%)	t_r	-	4	6	ns
Optical Fall Time (20% - 80%)	t_f	-	4	6	ns
Extinction Ratio	r_e	10	11	-	dB
Pulse Width Variation [2]	t_{PWV}	20.9	-	24.4	ns
Average Pulse Width Distortion [2]	t_{APWD}	-0.5	-	1.5	ns

Notes:

- The output power coupled into plastic fiber P_{opt} is measured with a large area detector at the end of a short length of a fiber (about 30 cm), which is ideally coupled to the Sidelooker. This value must not be used for calculating the power budget for a fiber optic system with a long fiber because the numerical aperture of plastic fibers decreases on the first meters. Therefore the fiber seems to have a higher attenuation over the first few meters compared with the specified value. Due to the direct coupling of the fiber to the LED at the end of the short fiber UMD (uniform mode distribution) will be observed. Therefore the following section of the cable has higher losses compared with EMD (equilibrium mode distribution)
- The electrical input signal fulfills $t_{PWV(\min)} = 22.9 \text{ ns}$ and $t_{PWV(\max)} = 24.1 \text{ ns}$.

Pulse Width Variation (t_{PWV}) and Average Pulse Width Distortion (t_{APWD})

The SPF MIT3 O2 generates negative Puls Width Distortion. This means the optical output signal is shortened compared to the electrical input signal. Therefore the parameters t_{PWV} and t_{APWD} do not meet the MOST Specification of Physical Layer Rev 1.0 (MOST SPL Rev. 1.0) either at the electrical input signal (SP1 in the MOST SPL Rev. 1.0) or at the optical output signal (SP2 in the MOST SPL Rev. 1.0). This characteristic is shown in the following table.

Parameter	Symbol	Electrical Input Signal		Optical Output Signal		Unit	Remarks	
		Min	Max	Min	Max			
a	Pulse Width Variation	t_{PWV}	22.9	24.1	20.9	24.4	ns	Optical Output Signal according to MOST Specification of Physical Layer Rev. 1.0
	Average Pulse Width Distortion	t_{APWD}	1.0	1.5	-0.5	1.5	ns	
b	Pulse Width Variation	t_{PWV}	21.1	23.1	19.1	23.4	ns	Electrical Input Signal according to MOST Specification of Physical Layer Rev. 1.0
	Average Pulse Width Distortion	t_{APWD}	-0.5	0.5	-2.0	0.5	ns	

Based on this table, the MOST System may be considered by two aspects:

- In order to meet the MOST SPL Rev 1.0 at SP2 the t_{PWV} and t_{apwd} at SP1 have to be longer than described in the MOST SPL Rev. 1.0. This can be achieved e.g. by using OS8104 as MOST transceiver chip.
- If the MOST SPL Rev. 1.0 is met regarding t_{PWV} and t_{apwd} at SP1, then the output signal SP2 is systematically shortened. Within a MOST System, this characteristic can be compensated by the optical receiver which detects the signal at SP3. For this compensation, the optical receiver has to be specified in a range which is smaller than the range described in the MOST SPL Rev. 1.0. For a detailed evaluation of system behavior, see paper "OS8300 Revision J behavior on SP2 (optical output signal)" from Oasis SiliconSystems.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Low Level Input Voltage	V_{IL}	-0.3	-	0.8	V
High Level Input Voltage	V_{IH}	2.0	-	$V_{CC} + 0.3$	V
Input Leakage Current ($V_{CC}=5.0V$, $V_I=0.0V$ or $V_I=5.0V$)	I_L	-	-	+/- 20	μA
Input Capacitance	C_I	-	-	7	pF
Input Resistance	R_I	100	-	-	kOhm
Supply Current ($R_{ext} = 15\text{ kOhm}$) ON state, biphas coded data ^[1]	I_{CC}	-	25	35	mA
Supply Current ($R_{ext} = 15\text{ kOhm}$) OFF state ^[2]	I_{LP2}	-	-	1	mA

Notes:

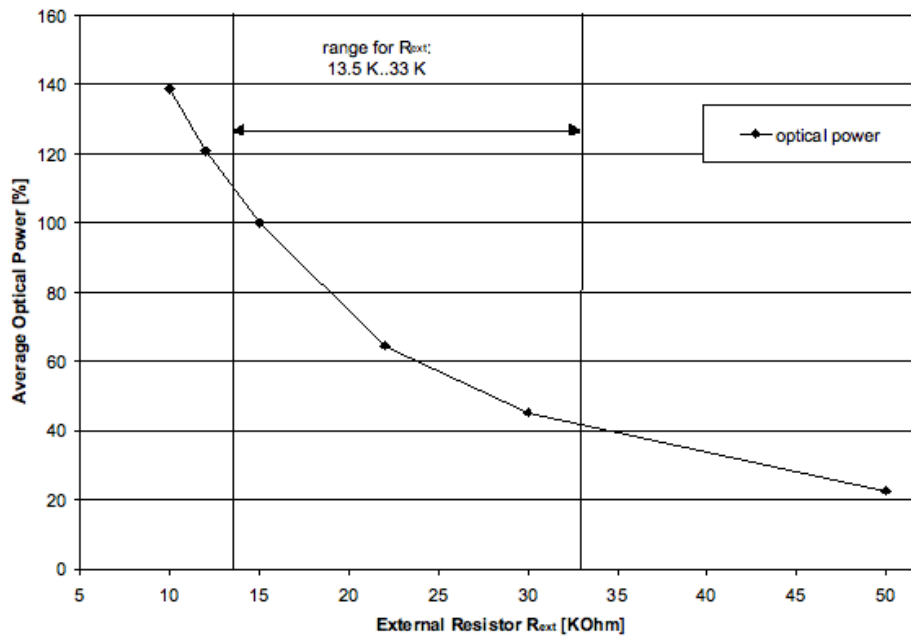
- The current through the LED and therefore the optical output power and overall power consumption depends on the settings of R_{ext} . The nominal value for R_{ext} is 15K. With $R_{ext}=30K$ the optical output power is about -3dB of the nominal value. Typical behaviour see Fiure below.
Important: The external resistor of R_{ext} must be within the range of 13.5K to 33K. For values of R_{ext} out of this range functionality may not be given over the whole temperature range and the device lifetime. Using values below 13K for R_{ext} can damage the transmitter.
- The transmitter jumps to low power mode after TX DATA is low for max. 18 μs If the transmitter is in low power mode it is switched ON 5 μs (max.) after TX DATA starts toggling.

AC Electrical Characteristics

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Power Supply Rejection Ratio	25 MHz Power Supply Noise	PSRR	-	30	-	dB
Power Up Time	Zero - MOST Data	TPU	1.0	2.5	5.0	μ s
Power Down Time	MOST Data - Zero	TPD	-	-	18.0	μ s
Input Rise Time		t_{TLH}	-	-	5	ns
Input Fall Time		t_{THL}	-	-	5	ns

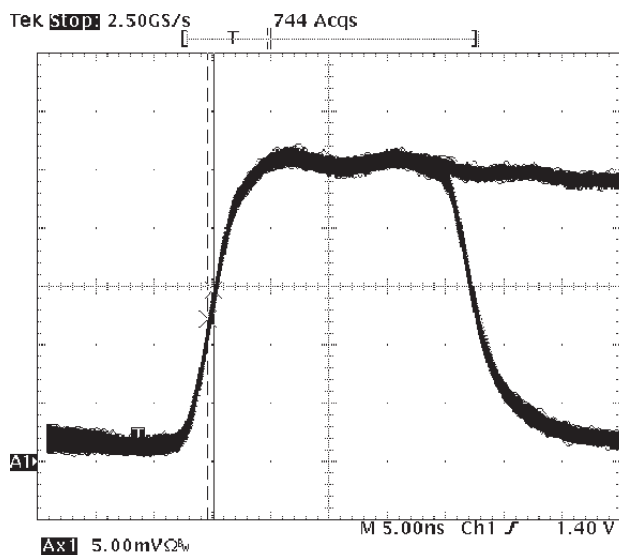
Typical Dependency of Average Output Power P_{opt} on external Resistor R_{ext}

(22.5 MBit MOST Data / $V_{CC}=5V$ / $T_A=25^\circ C$)

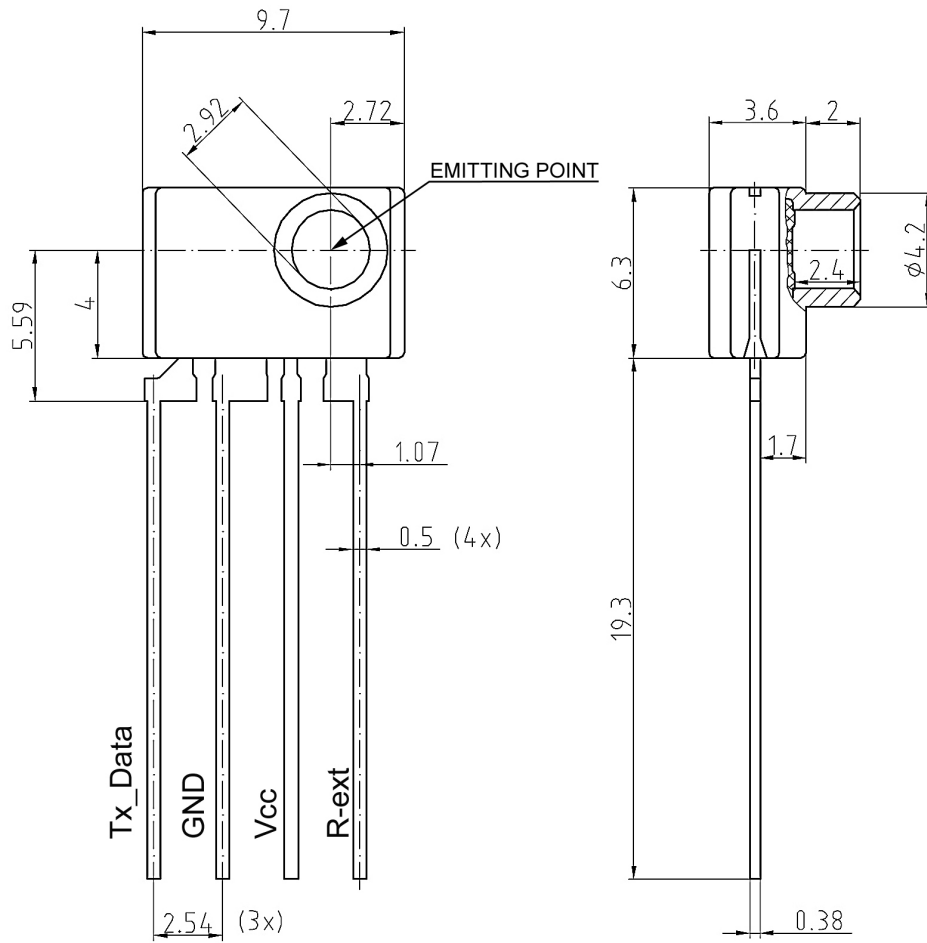


Typical Output Signal

Measured with fast optical receiver (Graviton SPD-1) with 15 kOhm external resistor and 22.579 Mbit/s MOST Data at $T_A=25^\circ C$.

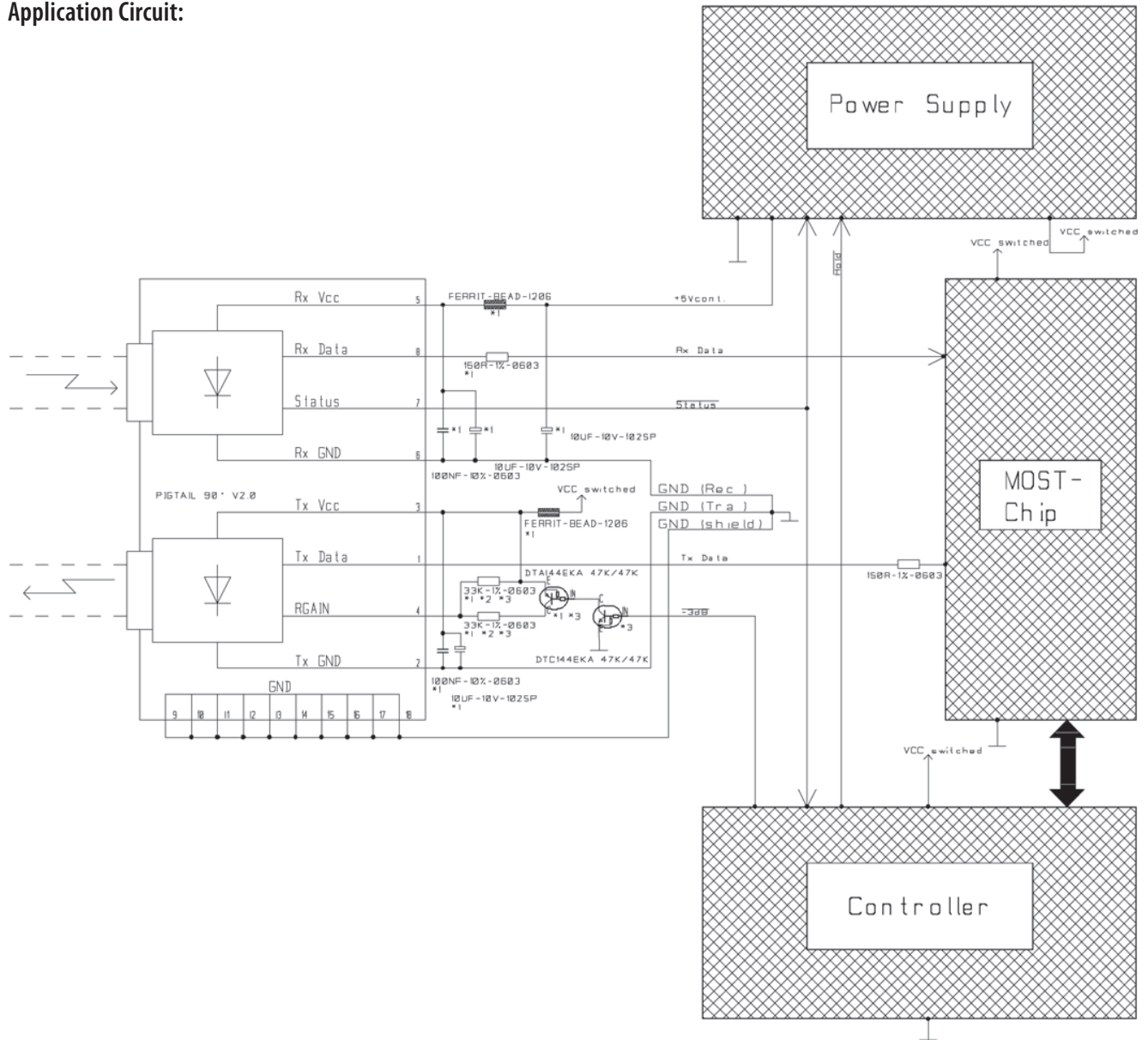


Mechanical Design MIT3 02: CAI package (cavity as interface)



Device information (Lot number etc.) is given on CAI backside by laser marking (for details see drawing marking specification).

Application Circuit:



Notes:

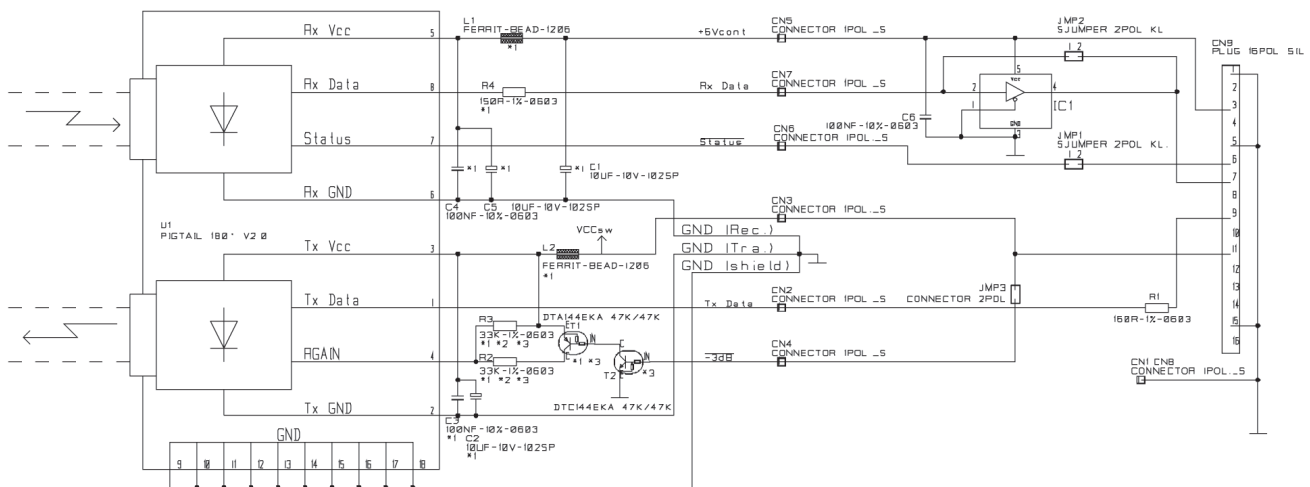
1. Place these components as close as possible to their corresponding pins of the FOT.
2. Values can change due to different light output power of the LED.
3. This is just a proposal for the Rext application. There can be used also other circuits to switch Rext from 15K to 30K

Design & Layout rules

- The 100nF bypass capacitors of the FOTs must be located as close as possible between the pins Vcc and GND of the FOTs. Use ceramic caps and tantalum caps with low ESR.
- Also the inductor/ferrite bead (receiver) and the -3dB - control circuit (transmitter) must be placed as close as possible to the FOTs. We prefer ferrite beads (e.g. type 74279214 Würth Elektronik) since the d.c. resistance is very low. If other inductors are used the d.c. resistor should be less than 30Ω.
- For EMC a ferrite bead should be connected to the power supply close to the transmitter and the receiver. Do not use only one ferrite bead together for receiver and transmitter!
- For the ground connection a ground plane is recommended (Y-structure). That means the ground planes of the transmitter, the receiver and the shielding must be separated. The three ground planes should be connected together behind the bypass capacitors (refer to the PCB design below). This ground signal should be connected directly to the ground plane of the MOST controller (e.g. OS8104) and the power supply on the top layer and/or bottom layer and ground layer as it is indicated in the example below.
- If a multi layer design is used the ground layer must have the same ground separation like shown for the top layer!
- A serial resistor in the Rx/Tx data line will also reduce EMC - problems. For Rx the resistor must be placed near the receiver - for Tx the resistor must be placed near the MOST controller chip. The value depends from the distance between the FOTs and the MOST chip (< 5cm) and can be in the range of up to 150Ω. Higher values for the resistors will increase jitter and can therefore cause locking problems of the MOST PLL!
- The Rx/Tx signals should not be routed parallel over a long distance but may be embedded with ground copper, if possible.
- The GND pin and the pin of Rext (15K - resistor) of the transmitter are used for heat dissipation. Therefore there should be a good connection to the PCB - no isolation gaps! Both pins should dip into a copper area (see layout example below).

Layout example

The reference board from OASIS Silicon Systems follows the requirements above. The schematic is very similar to the example above, but does not include the connection to the power supply, the OS8104 or the microcontroller.



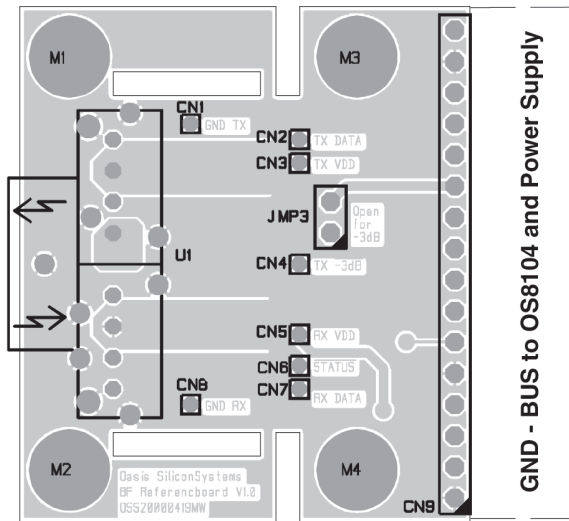
The examples below for top- and bottom layer is the layout of the reference design board and shows how the layout around the optical receiver and transmitter should look like.

It is strongly recommended to follow this examples in your design to get best performance!

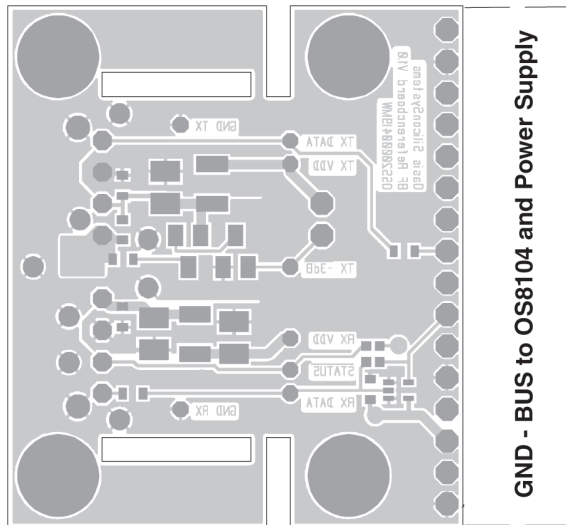
Note:

1. The buffer circuit (IC1), the connectors and jumpers in the middle to the right section of the schematic are only for use of the reference board and will not be necessary for your HW - design.

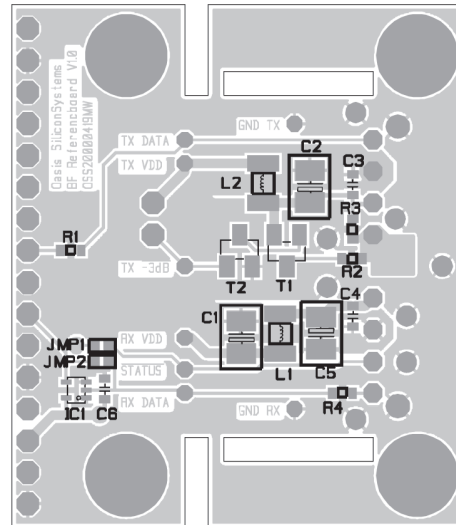
Top Layer with 180° version of the pigtail:



Bottom Layer (seen from the top side of the PCB):



Bottom Layer: Bottom side / positions



Other items

- The shown circuit for the -3dB attenuation is just a proposal. Also any other circuit which can double the value of Rext is permitted.
- Due to the fact that the optical average level jumps if the power control signal (/ -3dB) is toggled there can occur LOCK/coding – errors at the following device for a short time. This is not very critical, since it does occur only in diagnosis mode. After a time of 10ms the device should lock again if the optical attenuation between the devices is not too high.
- The Rx and Tx signals can be measured by using standard probes (>1M/<10pF). However, if the signal quality is very bad and the LOCK signal of the MOST chip is flaky connecting a passive probe to the Rx signal can cause the MOST chip to lock better or worse to the signal. This is due to the capacitance of the analog probe which is usually in the range of 8..12pF and shifts the phase and PWD of the signal. In this case an active probe with a capacitance of less than 1pF is recommended.
- The reference test board which corresponds to the layout examples above is available at the Oasis Silicon System AG.

Disclaimer

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

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