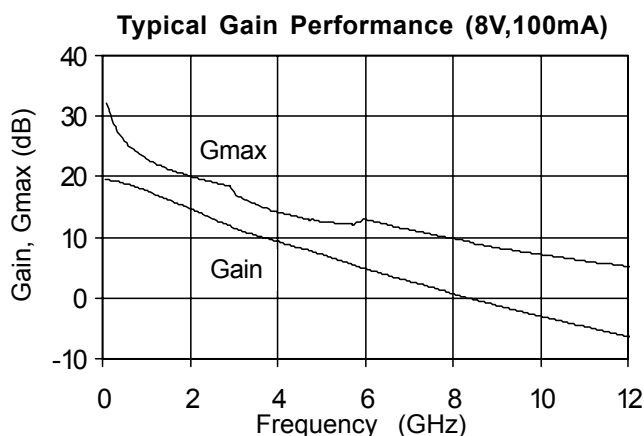


Product Description

Sirenza Microdevices' SHF-0186 is a high performance AlGaAs/GaAs Heterostructure FET (HFET) housed in a low-cost surface-mount plastic package. The HFET technology improves breakdown voltage while minimizing Schottky leakage current resulting in higher PAE and improved linearity.

Output power at 1dB compression for the SHF-0186 is +28 dBm when biased for Class AB operation at 8V,100mA. The +40 dBm third order intercept makes it ideal for high dynamic range, high intercept point requirements. It is well suited for use in both analog and digital wireless communication infrastructure and subscriber equipment including 3G, cellular, PCS, fixed wireless, and pager systems



SHF-0186

0.05-12 GHz, 0.5 Watt GaAs HFET



Pending Obsolescence
Last Time Buy Date: March 15, 2004

Product Features

- +28 dBm Output Power at 1dB Compression
- +40 dBm Output IP3
- High Drain Efficiency
- 18 dB Gain at 900 MHz (Application circuit)
- 15 dB Gain at 1960 MHz (Application circuit)
- See App Note AN-020 for circuit details

Applications

- Analog and Digital Wireless Systems
- 3G, Cellular, PCS
- Fixed Wireless, Pager Systems

Symbol	Device Characteristics, T = 25°C V _{DS} =8V, I _{DD} =100mA (unless otherwise noted)	Test Frequency [1] = 100% Tested [2] = Sample Tested	Units	Min.	Typ.	Max.
G _{max}	Maximum Available Gain Z _S =Z _S [*] , Z _L =Z _L [*]	f = 900 MHz f = 1960 MHz f = 12000 MHz [1]	dB	- - 4.0	23.4 20.1 5.0	- - -
S ₂₁	Insertion Gain Z _S =Z _L = 50 Ohms	f = 900 MHz f = 1900 MHz [1]	dB	- 14.0	18.0 15.0	- 16.0
G	Power Gain Z _S =Z _{SOPT} , Z _L =Z _{LOPT}	f = 900 MHz f = 1960 MHz [2]	dBm	- -	17.9 14.5	- -
OIP3	Output Third Order Intercept Point Z _S =Z _{SOPT} , Z _L =Z _{LOPT} , P _{OUT} = +15 dBm per tone	f = 900 MHz f = 1960 MHz [2]	dBm	- -	41 40	- -
P1dB	Output 1dB Compression Point Z _S =Z _{SOPT} , Z _L =Z _{LOPT}	f = 900 MHz f = 1960 MHz [2]	dBm	- -	28 28	- -
I _{DSS}	Saturated Drain Current V _{DS} = V _{DSP} , V _{GS} = 0V		mA	204	294	384
g _m	Transconductance V _{DS} = V _{DSP} , V _{GS} = -0.25V		mS	144	198	252
V _P	Pinch-Off Voltage V _{DS} = 2V, I _{DS} = 0.6mA	[1]	V	-3.0	-1.9	-1.0
BV _{GS}	Gate-to-Source Breakdown Voltage I _{GS} = 1.2mA, drain open	[1]	V	-	-17	-15
BV _{GD}	Gate-to-Drain Breakdown Voltage I _{GD} = 1.2mA, V _{GS} = -5V	[1]	V	-	-22	-17
R _{th}	Thermal Resistance (junction-to-lead)		°C/W	-	66	-
V _{DS}	Operating Voltage (drain-to-source)		V	-	-	9.0
I _{DS}	Operating Current (drain-to-source, quiescent)		mA	-	-	200
T _J	Recommended Operating Junction Temperature		C	-	-	150

The information provided herein is believed to be reliable at press time. Sirenza Microdevices assumes no responsibility for inaccuracies or omissions.

Sirenza Microdevices assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. Sirenza Microdevices does not authorize or warrant any Sirenza Microdevices product for use in life-support devices and/or systems.

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Absolute Maximum Ratings

Operation of this device beyond any one of these parameters may cause permanent damage.

MTTF is inversely proportional to the device junction temperature. For junction temperature and MTTF considerations the device operating conditions should also satisfy the following expressions:

$$P_{DC} - P_{OUT} < (T_J - T_L) / R_{TH}$$

where:

- $P_{DC} = I_{DS} * V_{DS}$ (W)
- P_{OUT} = RF Output Power (W)
- T_J = Junction Temperature (°C)
- T_L = Lead Temperature (pin 2,4) (°C)
- R_{TH} = Thermal Resistance (°C/W)

Parameter	Symbol	Value	Unit
Drain Current	I_{DS}	294	mA
Forward Gate Current	I_{GSF}	1.2	mA
Reverse Gate Current	I_{GSR}	1.2	mA
Drain-to-Source Voltage	V_{DS}	+12	V
Gate-to-Source Voltage	V_{GS}	<-5 or >0	V
RF Input Power	P_{IN}	200	mW
Operating Temperature	T_{OP}	-40 to +85	°C
Storage Temperature Range	T_{stor}	-40 to +175	°C
Power Dissipation	P_{DISS}	3.5	W
Channel Temperature	T_J	+175	°C

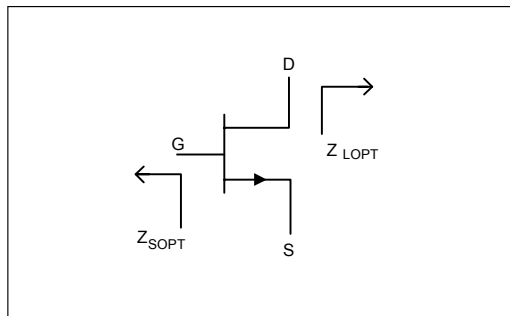
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page 1.

Typical Performance - Engineering Application Circuits (See App Note AN-020)

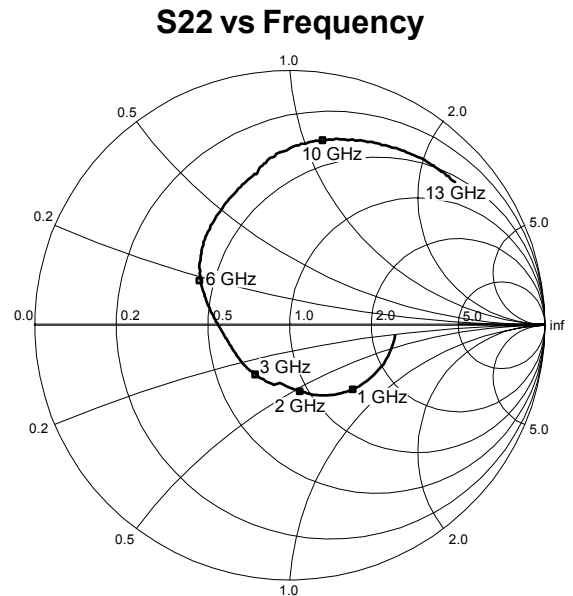
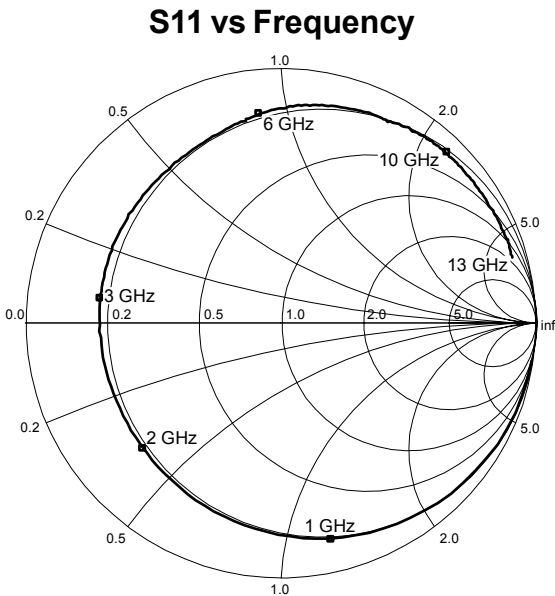
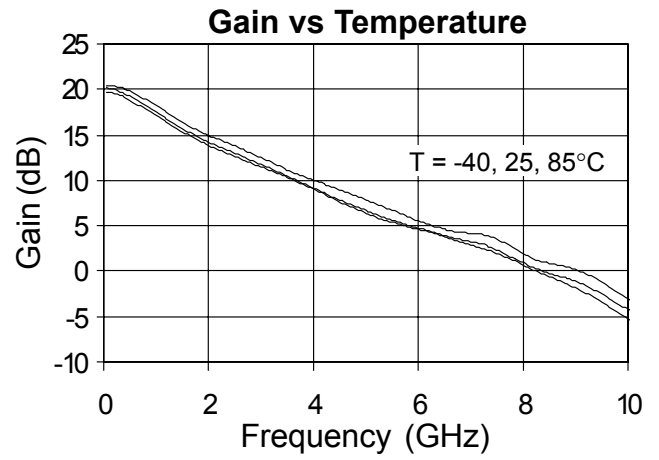
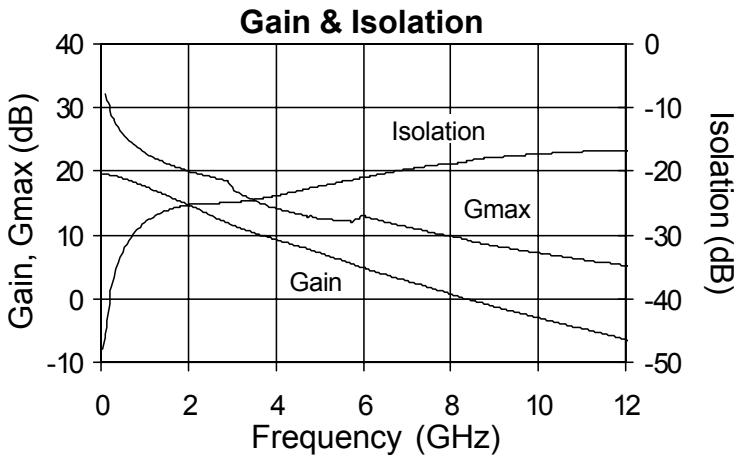
Freq (MHz)	V_{DS} (V)	I_{DQ} (mA)	P1dB (dBm)	OIP3* (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)	Z_{SOPT} (Ω)	Z_{LOPT} (Ω)
900	8	100	28.1	40.5	18.4	-16	-9	3.1	73 + j51.5	50.3 + j2.6
1960	8	100	28.8	40	14.7	-16	-5	2.5	24.9 + j32.0	36.4 - j2.5
2140	8	100	28.7	38.5	14.4	-12	-7	3.0	21.4 + j24.7	34.9 + j2.3
2450	8	100	28.6	39.5	13.9	-15	-5	2.9	15.0 + j21.6	44.8 - j5.5

* P_{OUT} = +15dBm per tone, 1MHz tone spacing

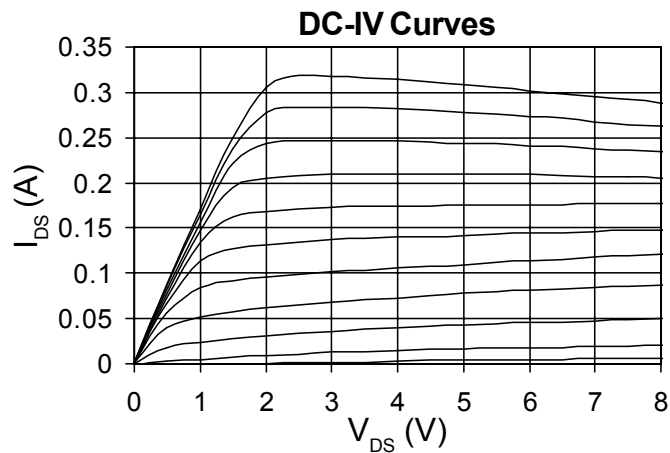
Data above represents typical performance of the application circuits noted in Application Note AN-020. Refer to the application note for additional RF data, PCB layouts, and BOMs for each application circuit. The application note also includes biasing instructions and other key issues to be considered. For the latest application notes please visit our site at www.sirenza.com or call your local sales representative.



De-embedded S-Parameters ($Z_S=Z_L=50\ \text{Ohms}$, $V_{DS}=8\text{V}$, $I_{DS}=100\text{mA}$, 25°C)



Note: S-parameters are de-embedded to the device leads with $Z_S=Z_L=50\ \Omega$. The data represents typical performance of the device. De-embedded s-parameters can be downloaded from our website (www.sirenza.com).



$V_{GS} = -2.0\ \text{to}\ 0\text{V}$, 0.2V steps
 $T=25^\circ\text{C}$



Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Part Number Ordering Information

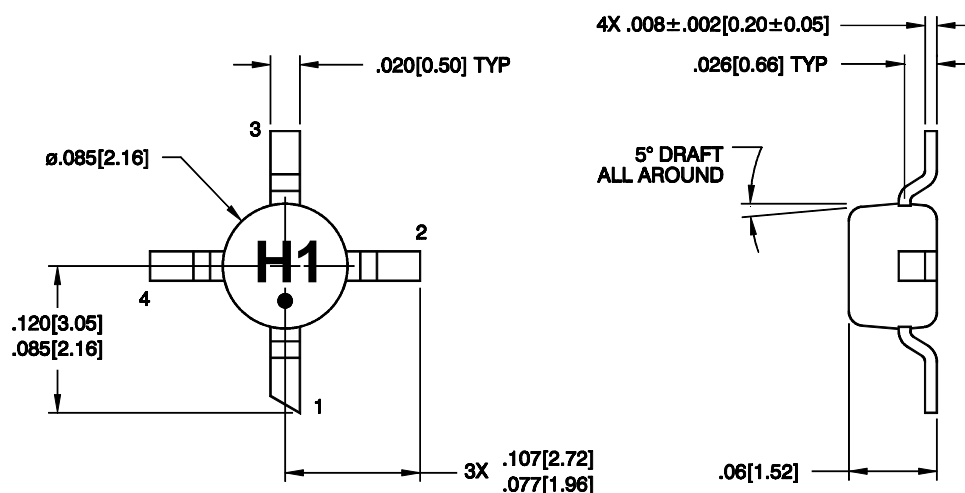
Part Number	Reel Size	Devices/Reel
SHF-0186	7"	1000

Part Symbolization

The part will be symbolized with the "H1" designator and a dot signifying pin 1 on the top surface of the package.

Pin #	Function	Description
1	Gate	RF Input
2	Source	Connection to ground. Use via holes to reduce lead inductance. Place vias as close to ground leads as possible.
3	Drain	RF Output
4	Source	Same as Pin 2

Package Dimensions



PCB Pad Layout

