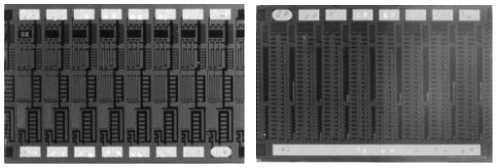
Thin Film Eight Resistor Array



Product may not be to scale

The CLA and CLB resistor arrays are the hybrid equivalent to the eight resistor common connection and isolated networks available in sips or dips. The resistors are spaced on 0.010 inches centers resulting in minimal space requirements.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CLA and CLBs are 100 % electrically tested and visually inspected to MIL-STD-883.

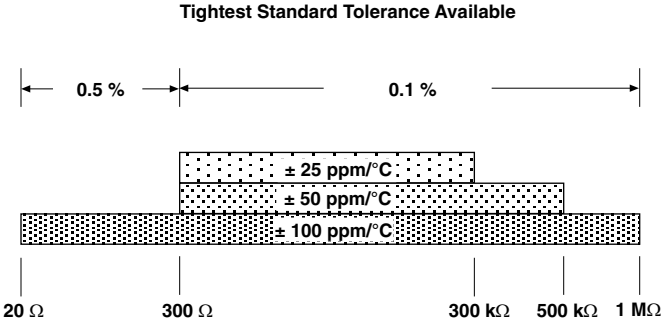
FEATURES

- Wire bondable
- Eight equal value resistors on a 0.060 x 0.090 inch chip
- Resistance range: 20 Ω to 1 MΩ
- Excellent TCR tracking
- Resistor material: Tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Custom values available
- Moisture resistant

APPLICATIONS

The CLA and CLB thin film resistor arrays are designed for hybrid packages requiring up to eight resistors of the same resistance value and tolerance, as well as excellent TCR tracking. For such hybrids, they afford great savings in cost and space.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
026	054
017	049
008	045

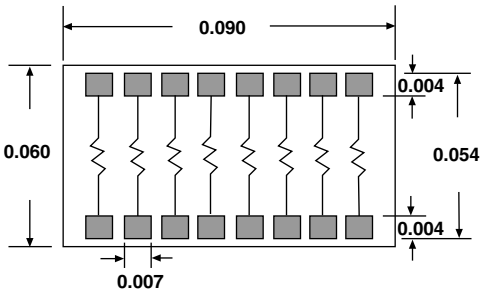
*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

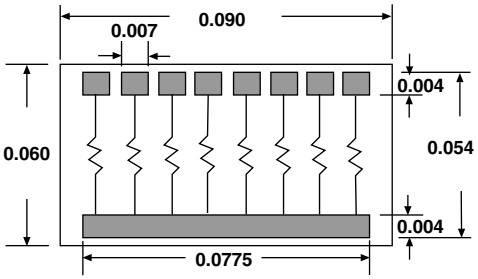
PARAMETER	
TCR Tracking Spread	± 5 ppm/°C
Noise, MIL-STD-202, Method 308 **100 Ω - 250 kΩ** **< 100 Ω or > 251 kΩ**	- 35 dB typ. - 20 dB typ.
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 % max. Δ*R*/*R*
Stability, 1000 h, + 125 °C, 25 mW **Absolute** **Ratio**	± 0.25 % max. Δ*R*/*R* ± 0.05 % max. Δ*R*/*R*
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock, MIL-STD-202 **Method 107, Test Condition F**	± 0.1 % max. Δ*R*/*R*
High Temperature Exposure, ± 150 °C, 100 h	± 0.2 % max. Δ*R*/*R*
Dielectric Voltage Breakdown	200 V
Insulation Resistance	10^{12} min.
Operating Voltage	100 V
DC Power Rating at + 70 °C (Derated to Zero at 175 °C)	50 mW per resistor
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.1 % max. Δ*R*/*R*

DIMENSIONS in inches

CLA



CLB



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.060 x 0.090 ± 0.002 (1.50 x 2.26 ± 0.05 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO_2
Resistor Material	Tantalum nitride, self-passivating
Bonding Pads	0.004 x 0.007 (0.10 x 0.178 mm)
Number of Top Pads	CLA - 16 CLB - 9
Pad Material	10 kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

Options: Gold backing for eutectic die attach
For custom configurations, consult Applications Engineer

ORDERING INFORMATION

Example: 100 % visualled, 10 kΩ, ± 1 %, ± 100 ppm/°C TCR, CLA format, aluminum pads, class H visual inspection

P/N:	**W**	**CLA**	**008**	**1000**	**1**	**F**
	INSPECTION /PACKAGING **W** = 100 % visually inspected parts per MIL-STD-883 in matrix trays **X** = Sample, visually inspected loaded in matrix trays (4 % AQL)	PRODUCT FAMILY	PROCESS CODE See Process Code table	RESISTANCE VALUE Use first 4 significant digits of the resistance	MULTIPLIER CODE **D** = 0.0001 **C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	TOLERANCE CODE **B** = 0.1 % **C** = 0.2 % **D** = 0.5 % **F** = 1.0 % **G** = 2.0 % **H** = 2.5 % **J** = 5.0 % **K** = 10 %

Disclaimer

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