



# STH165N10F4-2 STP165N10F4

N-channel 100 V, 4.1 mΩ, 160 A TO-220, H<sup>2</sup>PAK  
STripFET™ DeepGATE™ Power MOSFET

Preliminary data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STH165N10F4-2	100 V	< 5.1 mΩ	160 A
STP165N10F4	100 V	< 5.5 mΩ	120 A

- N-channel enhancement mode
- 100% avalanche rated
- Low gate charge
- Very low on-resistance

## Application

- Switching applications

## Description

This STripFET™ DeepGATE™ Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance, with a new gate structure, providing superior switching performances.

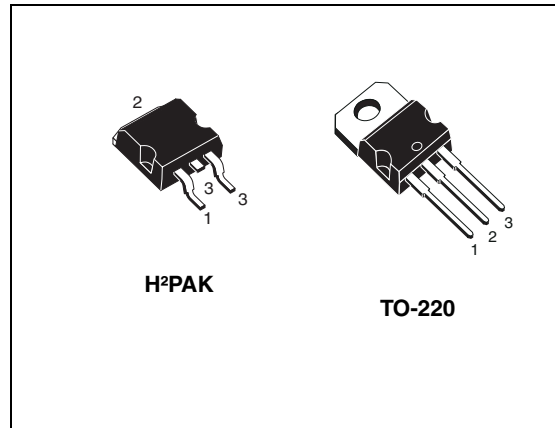


Figure 1. Internal schematic diagram

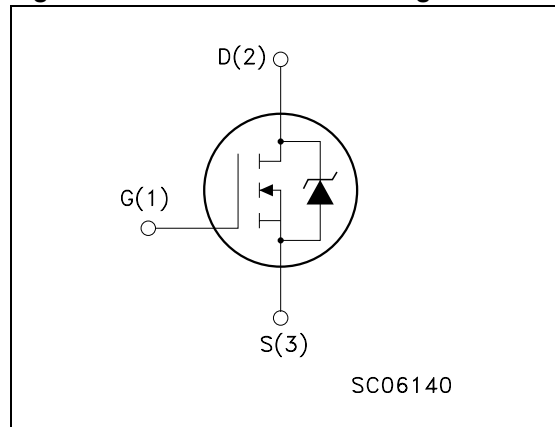


Table 1. Device summary

Order codes	Marking	Package	Packaging
STH165N10F4-2	165N10F4	H <sup>2</sup> PAK	Tape and reel
STP165N10F4	165N10F4	TO-220	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220	H <sup>2</sup> PAK	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	100		V
V <sub>GS</sub>	Gate- source voltage	± 20		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	120	160	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	110	115	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	480	640	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	315		W
	Derating factor	2.1		W/°C
E <sub>AS</sub> <sup>(2)</sup>	Single pulse avalanche energy	TBD		J
T <sub>stg</sub>	Storage temperature	– 55 to 175		°C
T <sub>j</sub>	Max. operating junction temperature	175		

1. Pulse width limited by safe operating area
2. Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = 45 A, V<sub>DD</sub> = 60 V

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220,	H <sup>2</sup> PAK	
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.48		°C/W
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb max		35 <sup>(1)</sup>	
R <sub>thj-a</sub>	Thermal resistance junction-ambient max	62.5		°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purpose	315		°C

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage	$V_{DS} = \text{max rating}$			1	$\mu A$
	Drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}, T_C = 125^{\circ}C$			100	$\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 60 A^{(1)}$		4.4	5.5	m $\Omega$
		$V_{GS} = 10 V, I_D = 80 A^{(2)}$		4.1	5.1	m $\Omega$

1. For TO-220

2. For H<sup>2</sup>PAK

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25 V, f = 1 \text{ MHz}, V_{GS} = 0$		10500		pF
$C_{oss}$	Output capacitance		-	1170	-	pF
$C_{rss}$	Reverse transfer capacitance				630	
$Q_g$	Total gate charge	$V_{DD} = 50 V, I_D = 120 A, V_{GS} = 10 V$ (see Figure 3)		180		nC
$Q_{gs}$	Gate-source charge		-	TBD	-	nC
$Q_{gd}$	Gate-drain charge				TBD	

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time	$V_{DD} = 50 V, I_D = 60 A, R_G = 4.7 \Omega, V_{GS} = 10 V$ (see Figure 2)		TBD		ns
	Rise time		-	TBD	-	ns
$t_{d(off)}$ $t_f$	Turn-off-delay time	$V_{DD} = 50 V, I_D = 60 A, R_G = 4.7 \Omega, V_{GS} = 10 V$ (see Figure 2)		TBD		ns
	Fall time		-	TBD	-	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		120 <sup>(1)</sup> 160 <sup>(2)</sup>	A
$I_{SDM}^{(3)}$	Source-drain current (pulsed)		-		480 <sup>(1)</sup> 640 <sup>(2)</sup>	A
$V_{SD}^{(4)}$	Forward on voltage	$I_{SD} = 120\text{ A}, V_{GS} = 0$	-		TBD	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 120\text{ A},$ $V_{DD} = 25\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s},$ $T_j = 150\text{ }^\circ\text{C}$ <i>(see Figure 4)</i>	-	TBD TBD TBD		ns nC A

1. For TO-220
2. For H<sup>2</sup>PAK
3. Pulse width limited by safe operating area.
4. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

### 3 Test circuits

Figure 2. Switching times test circuit for resistive load

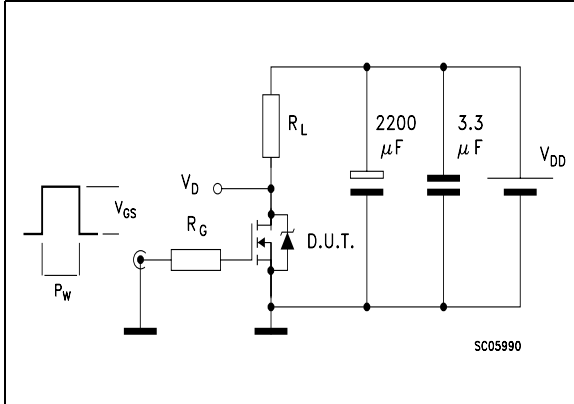


Figure 3. Gate charge test circuit

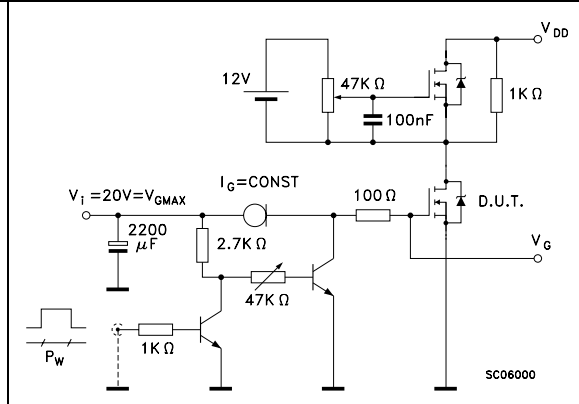


Figure 4. Test circuit for inductive load switching and diode recovery times

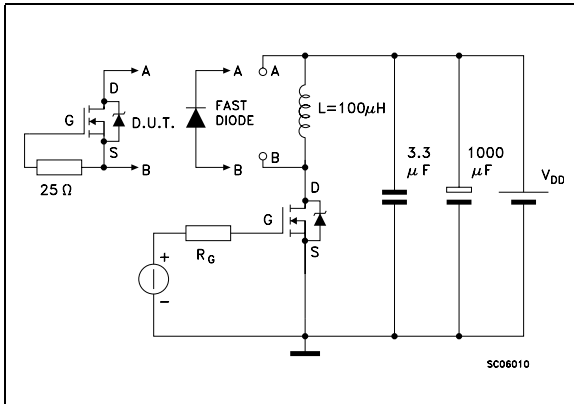


Figure 5. Unclamped inductive load test circuit

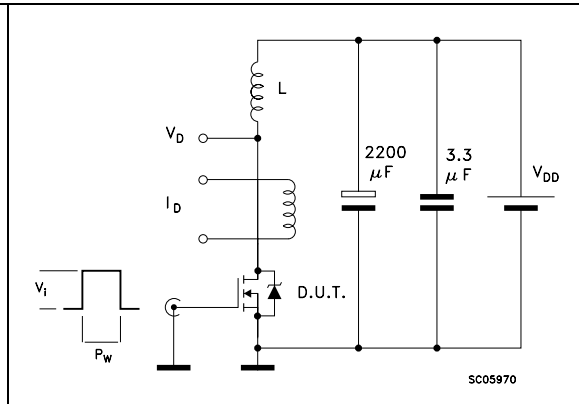


Figure 6. Unclamped inductive waveform

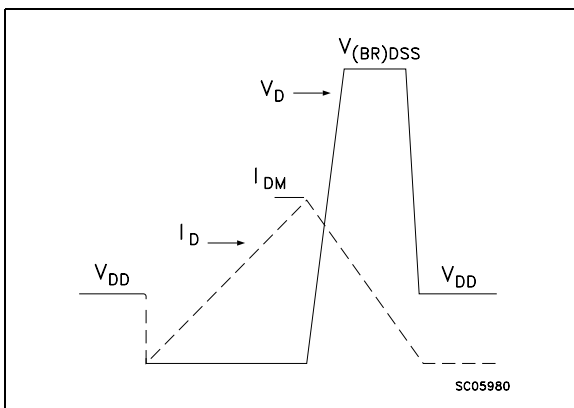
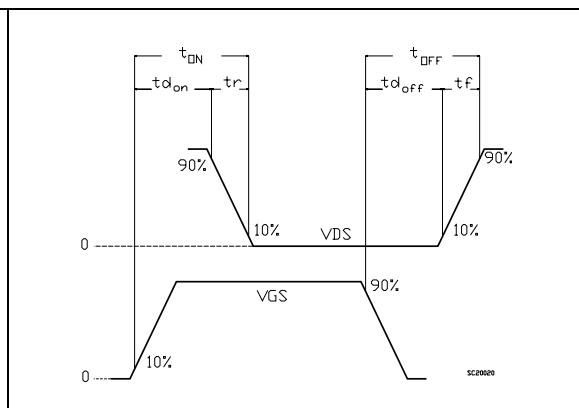


Figure 7. Switching time waveform



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

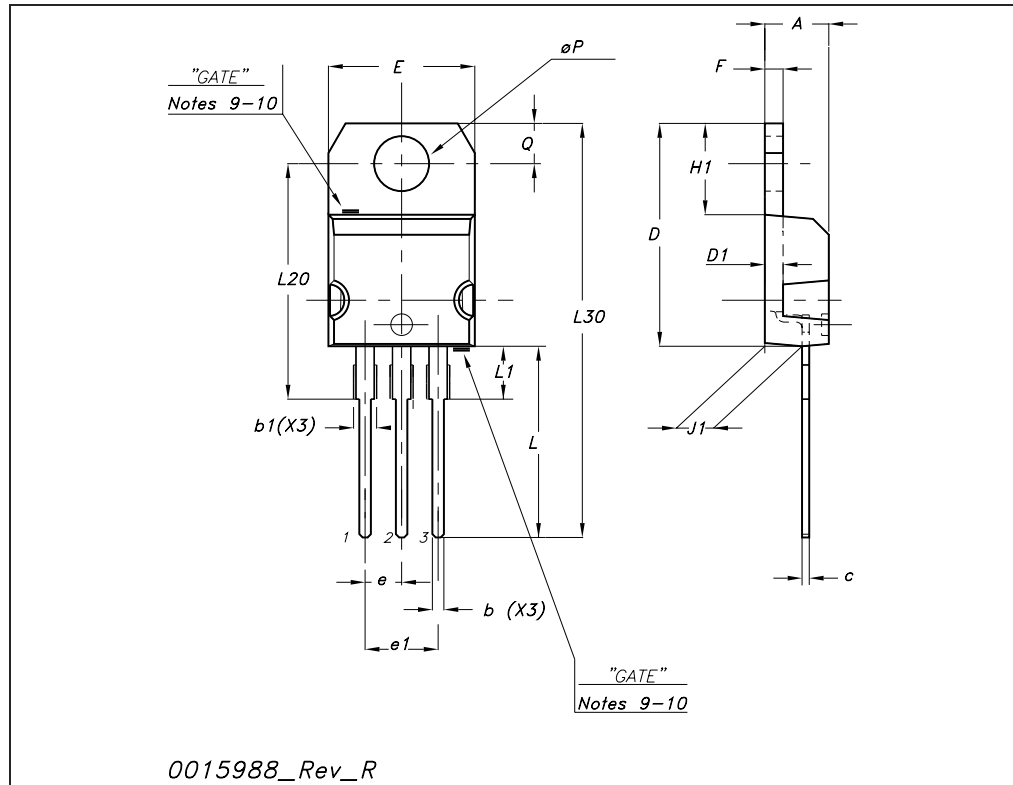




Table 8. H<sup>2</sup>PAK 2 leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.171		7.971
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	7.45		7.85
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 8. H<sup>2</sup>PAK 2 leads drawing

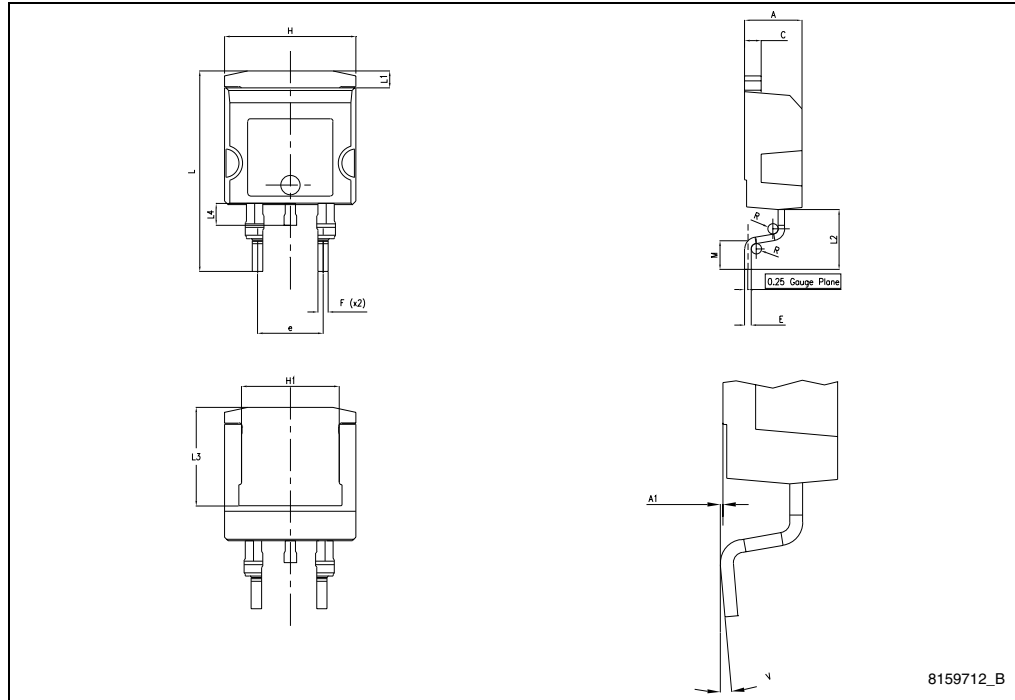
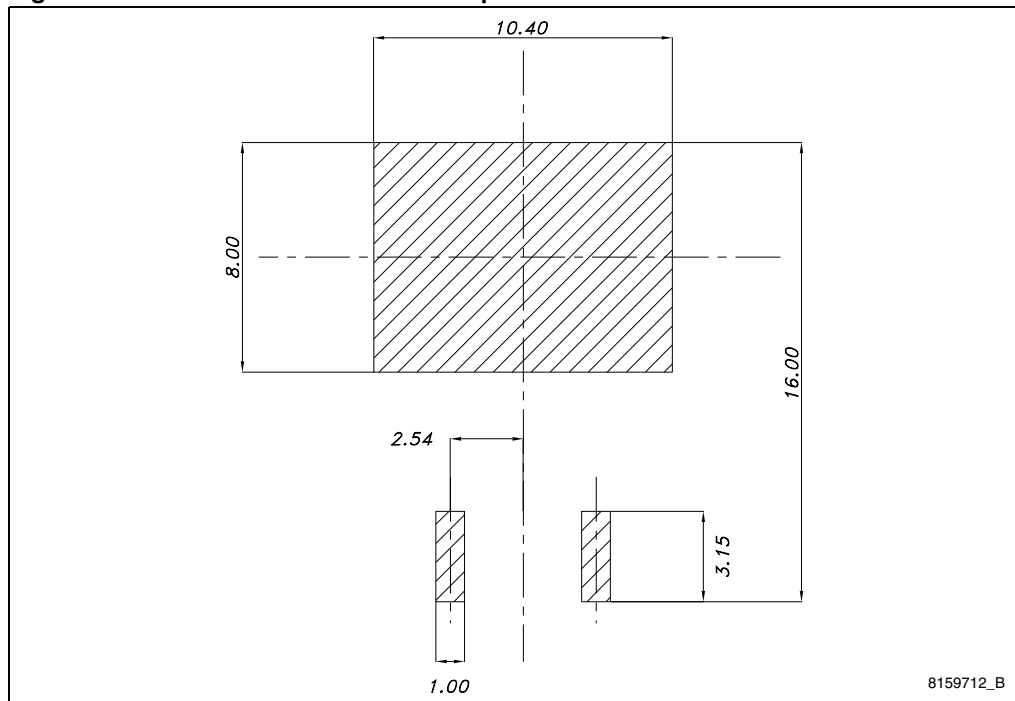


Figure 9. H<sup>2</sup>PAK 2 recommended footprint



## 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-May-2009	1	First release

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