

PHB/PHD66NQ03LT

N-channel TrenchMOS™ logic level FET

Rev. 06 — 2 August 2004

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Low on-state resistance.

1.3 Applications

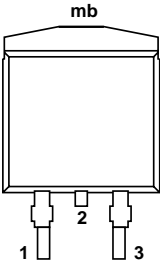
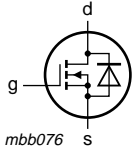
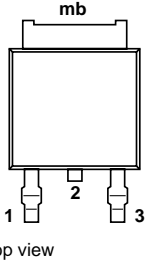
- DC-to-DC converters
- General purpose switching.

1.4 Quick reference data

- $V_{DS} \leq 25$ V
- $I_D \leq 66$ A
- $R_{DSon} \leq 10.5$ m Ω
- $Q_{gd} = 3.6$ nC (typ).

2. Pinning information

Table 1: Discrete pinning

| Pin | Description | Simplified outline | Symbol |
|-----|--|---|---|
| 1 | gate (g) |  |  |
| 2 | drain (d) ^[1] | | |
| 3 | source (s) | | |
| mb | mounting base; connected to drain (d) | | |
| | |  | |
| | | Top view | |
| | | SOT404 (D ² -PAK) | SOT428 (D-PAK) |

[1] It is not possible to make a connection to pin 2 of the SOT404 and SOT428 packages.

PHILIPS

3. Ordering information

Table 2: Ordering information

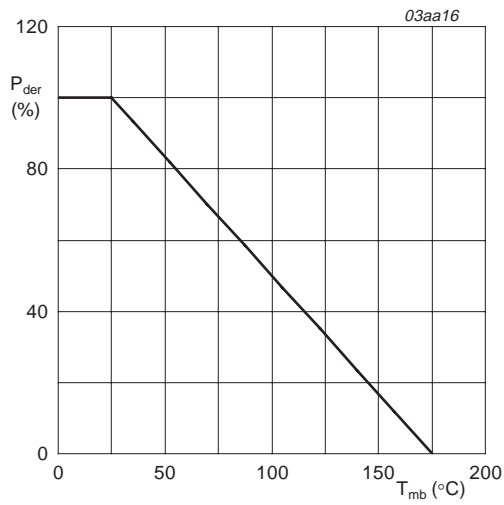
| Type number | Package | | Version |
|-------------|---------------------|---|---------|
| | Name | Description | |
| PHB66NQ03LT | D ² -PAK | Plastic single-ended surface mounted package (Philips version of D ² -PAK); 3 leads (one lead cropped) | SOT404 |
| PHD66NQ03LT | D-PAK | Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped) | SOT428 |

4. Limiting values

Table 3: Limiting values

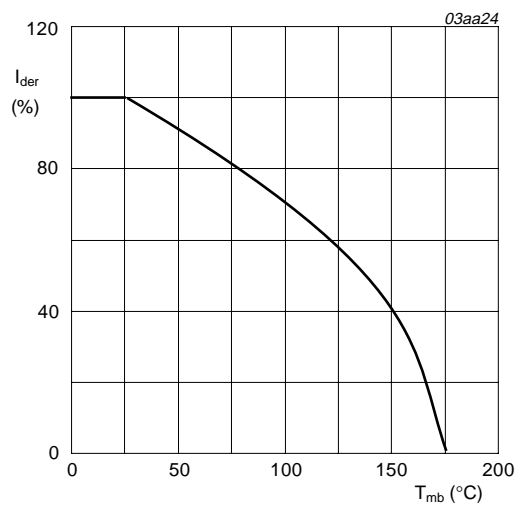
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|---|-----|------|------|
| V _{DS} | drain-source voltage (DC) | 25 °C ≤ T _j ≤ 175 °C | - | 25 | V |
| V _{DGR} | drain-gate voltage (DC) | 25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ | - | 25 | V |
| V _{GS} | gate-source voltage (DC) | | - | ±20 | V |
| I _D | drain current (DC) | T _{mb} = 25 °C; V _{GS} = 5 V; Figure 2 and 3 | - | 57 | A |
| | | T _{mb} = 100 °C; V _{GS} = 5 V; Figure 2 | - | 40 | A |
| | | T _{mb} = 25 °C; V _{GS} = 10 V | - | 66 | A |
| | | T _{mb} = 100 °C; V _{GS} = 10 V | - | 45 | A |
| I _{DM} | peak drain current | T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; Figure 3 | - | 228 | A |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; Figure 1 | - | 93 | W |
| T _{stg} | storage temperature | | -55 | +175 | °C |
| T _j | junction temperature | | -55 | +175 | °C |
| Source-drain diode | | | | | |
| I _S | source (diode forward) current (DC) | T _{mb} = 25 °C | - | 57 | A |
| I _{SM} | peak source (diode forward) current | T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs | - | 228 | A |
| Avalanche ruggedness | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | unclamped inductive load; I _D = 43 A; t _p = 0.15 ms; V _{DD} ≤ 25 V; R _{GS} = 50 Ω; V _{GS} = 10 V; starting at T _j = 25 °C | - | 90 | mJ |



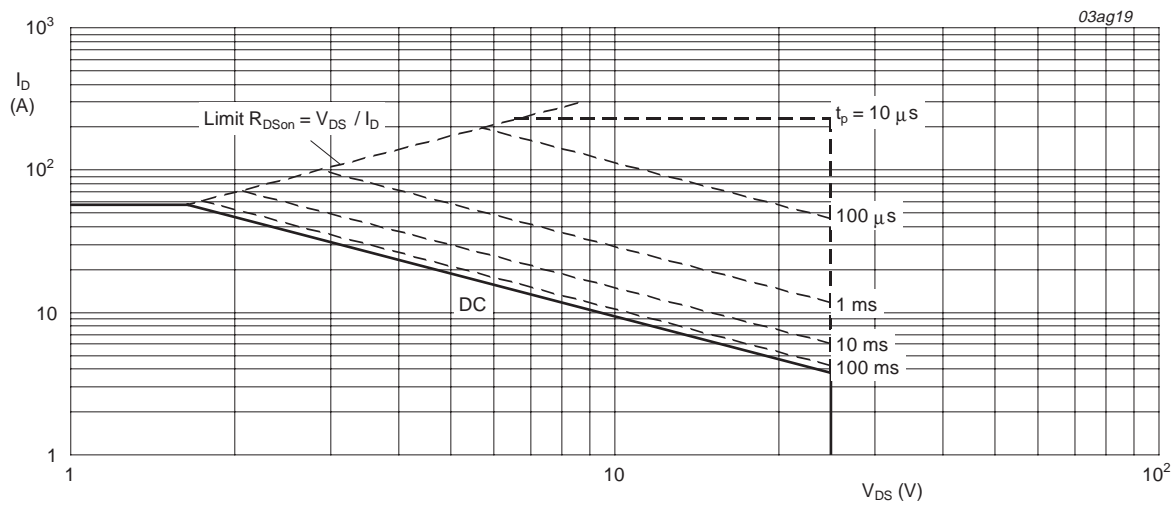
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 5 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|----------------|---|--------------------------|---|-----|-----|------|-----|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Figure 4 | - | - | 1.6 | K/W | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | SOT404 | mounted on a printed-circuit board; minimum footprint; vertical in still air | - | 50 | - | K/W |
| | | SOT428 | mounted on a printed-circuit board; minimum footprint; vertical in still air | - | 75 | - | K/W |
| | | | mounted on a printed-circuit board; SOT404 minimum footprint; vertical in still air | - | 50 | - | K/W |

5.1 Transient thermal impedance

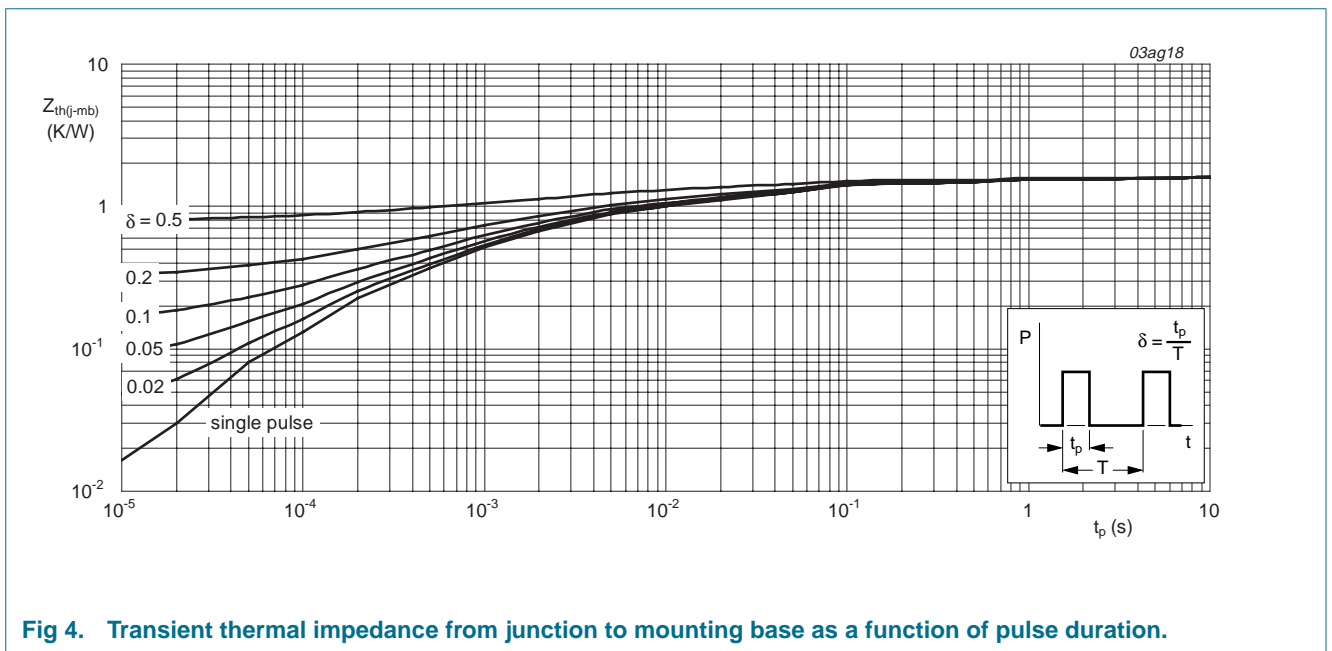
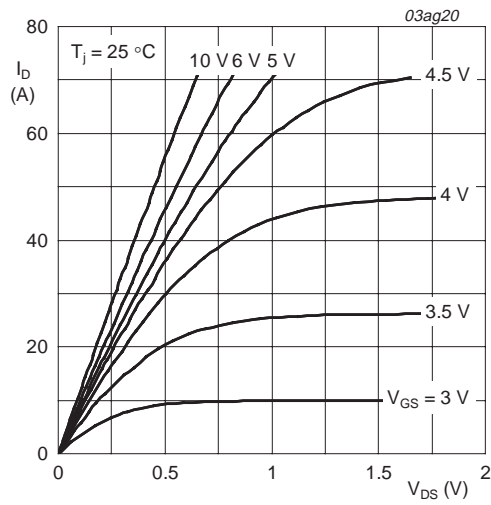


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

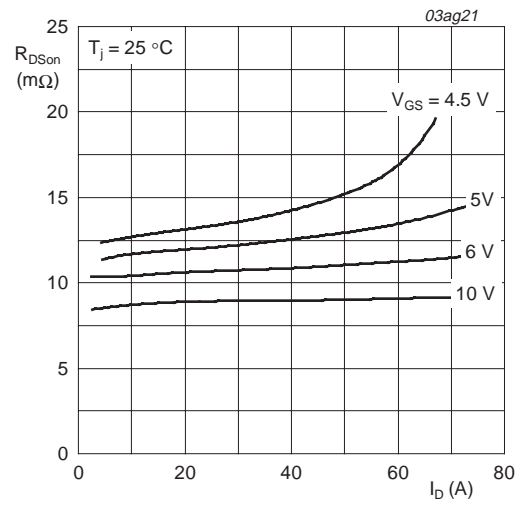
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--------------------------------------|--|---------------|---------------------|----------------------|----------------|
| Static characteristics | | | | | | |
| V _{(BR)DSS} | drain-source breakdown voltage | I _D = 250 μA; V _{GS} = 0 V T _j = 25 °C T _j = -55 °C | 25 22 | - - | - - | V V |
| V _{GS(th)} | gate-source threshold voltage | I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 and 10 T _j = 25 °C T _j = 175 °C T _j = -55 °C | 1 0.5 - | 1.5 - - | 2 - 2.2 | V V V |
| I _{DSS} | drain-source leakage current | V _{DS} = 25 V; V _{GS} = 0 V T _j = 25 °C T _j = 175 °C | - - - | - - - | 10 500 | μA μA |
| I _{GSS} | gate-source leakage current | V _{GS} = ±15 V; V _{DS} = 0 V | - | 10 | 100 | nA |
| R _{DS(on)} | drain-source on-state resistance | V _{GS} = 10 V; I _D = 25 A; Figure 6 and 8 T _j = 25 °C T _j = 175 °C V _{GS} = 5 V; I _D = 25 A; Figure 6 and 8 | - - - | 9.1 16.4 11.2 | 10.5 18.9 13.6 | mΩ mΩ mΩ |
| Dynamic characteristics | | | | | | |
| Q _{g(tot)} | total gate charge | I _D = 50 A; V _{DS} = 15 V; V _{GS} = 5 V; Figure 11 | - | 12 | - | nC |
| Q _{gs} | gate-source charge | | - | 4.5 | - | nC |
| Q _{gd} | gate-drain (Miller) charge | | - | 3.6 | - | nC |
| C _{iss} | input capacitance | V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; Figure 13 | - | 860 | - | pF |
| C _{oss} | output capacitance | | - | 330 | - | pF |
| C _{rss} | reverse transfer capacitance | | - | 145 | - | pF |
| t _{d(on)} | turn-on delay time | V _{DS} = 15 V; R _L = 0.6 Ω; V _{GS} = 5 V; R _G = 5.6 Ω | - | 15 | 25 | ns |
| t _r | rise time | | - | 90 | 135 | ns |
| t _{d(off)} | turn-off delay time | | - | 25 | 40 | ns |
| t _f | fall time | | - | 25 | 40 | ns |
| Source-drain diode | | | | | | |
| V _{SD} | source-drain (diode forward) voltage | I _S = 25 A; V _{GS} = 0 V; Figure 12 | - | 0.95 | 1.2 | V |
| t _{rr} | reverse recovery time | I _S = 10 A; dI _S /dt = -100 A/μs; | - | 32 | - | ns |
| Q _r | recovered charge | V _{GS} = 0 V; V _R = 25 V | - | 20 | - | nC |



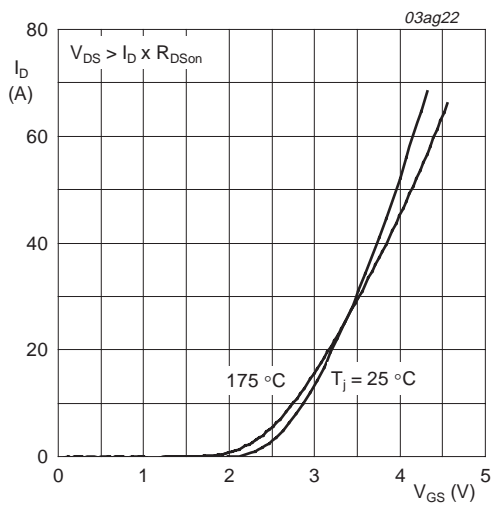
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



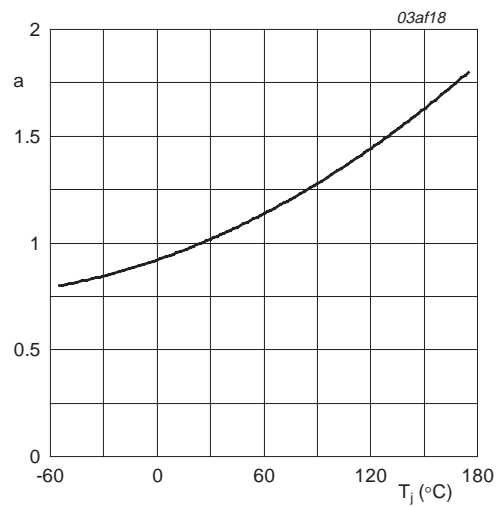
$T_j = 25\text{ °C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values.



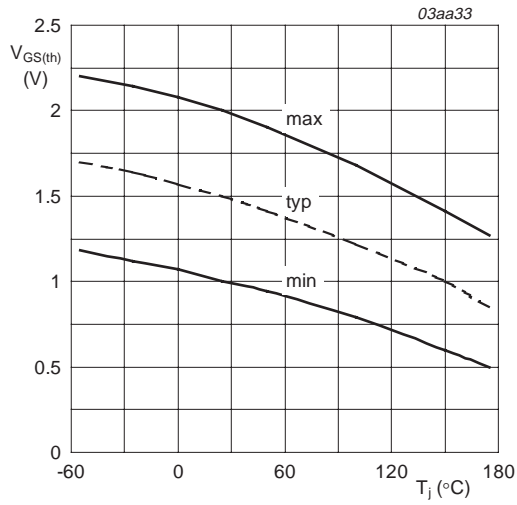
$T_j = 25\text{ °C and } 175\text{ °C}; V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



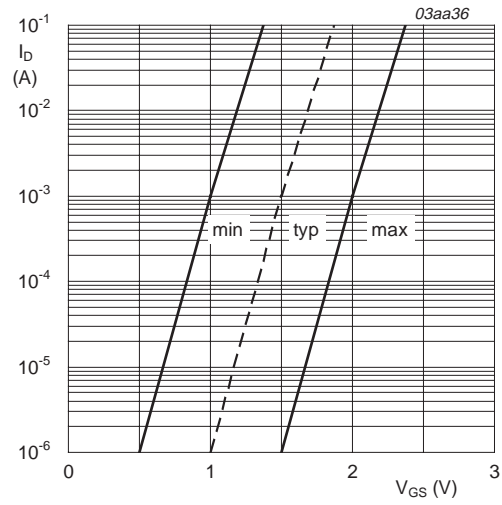
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



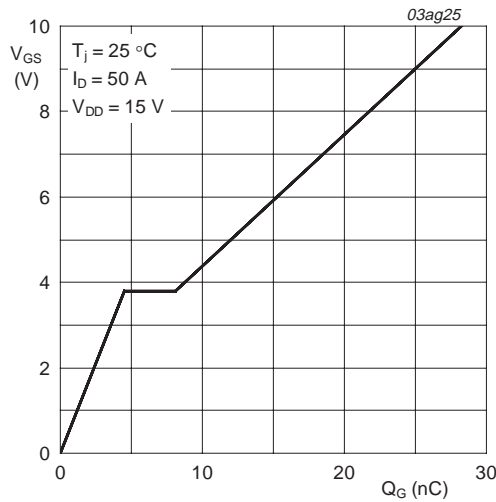
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



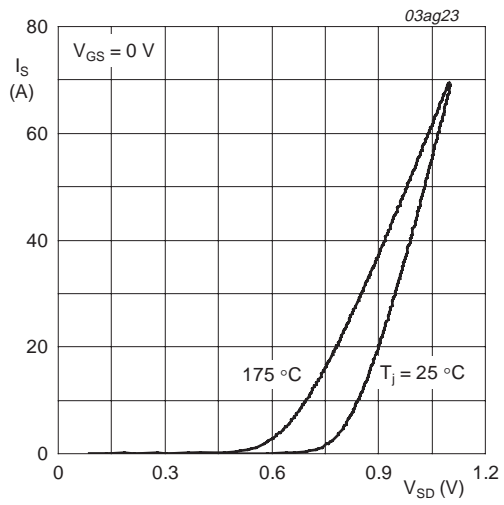
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



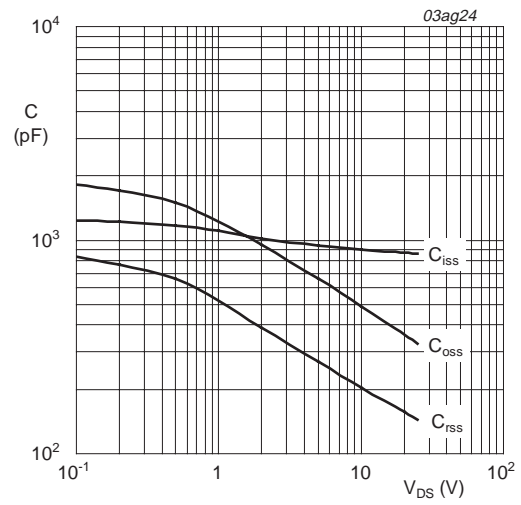
$I_D = 50 \text{ A}; V_{DS} = 15 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values.



$T_J = 25\text{ °C}$ and 175 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



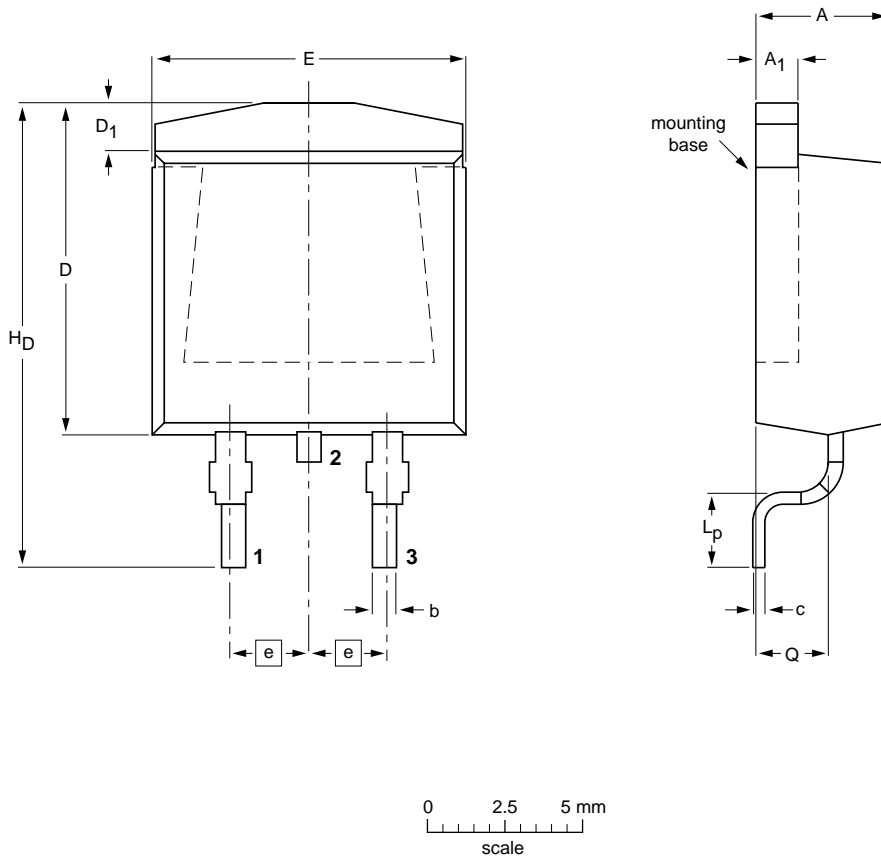
$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

| UNIT | A | A ₁ | b | c | D max. | D ₁ | E | e | L _p | H _D | Q |
|------|------|----------------|------|------|--------|----------------|-------|------|----------------|----------------|------|
| mm | 4.50 | 1.40 | 0.85 | 0.64 | 11 | 1.60 | 10.30 | 2.54 | 2.90 | 15.80 | 2.60 |
| | 4.10 | 1.27 | 0.60 | 0.46 | | 1.20 | 9.70 | | 2.10 | 14.80 | 2.20 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT404 | | | | | | 99-06-25 01-02-12 |

Fig 14. SOT404 (D²-PAK) package outline.

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428

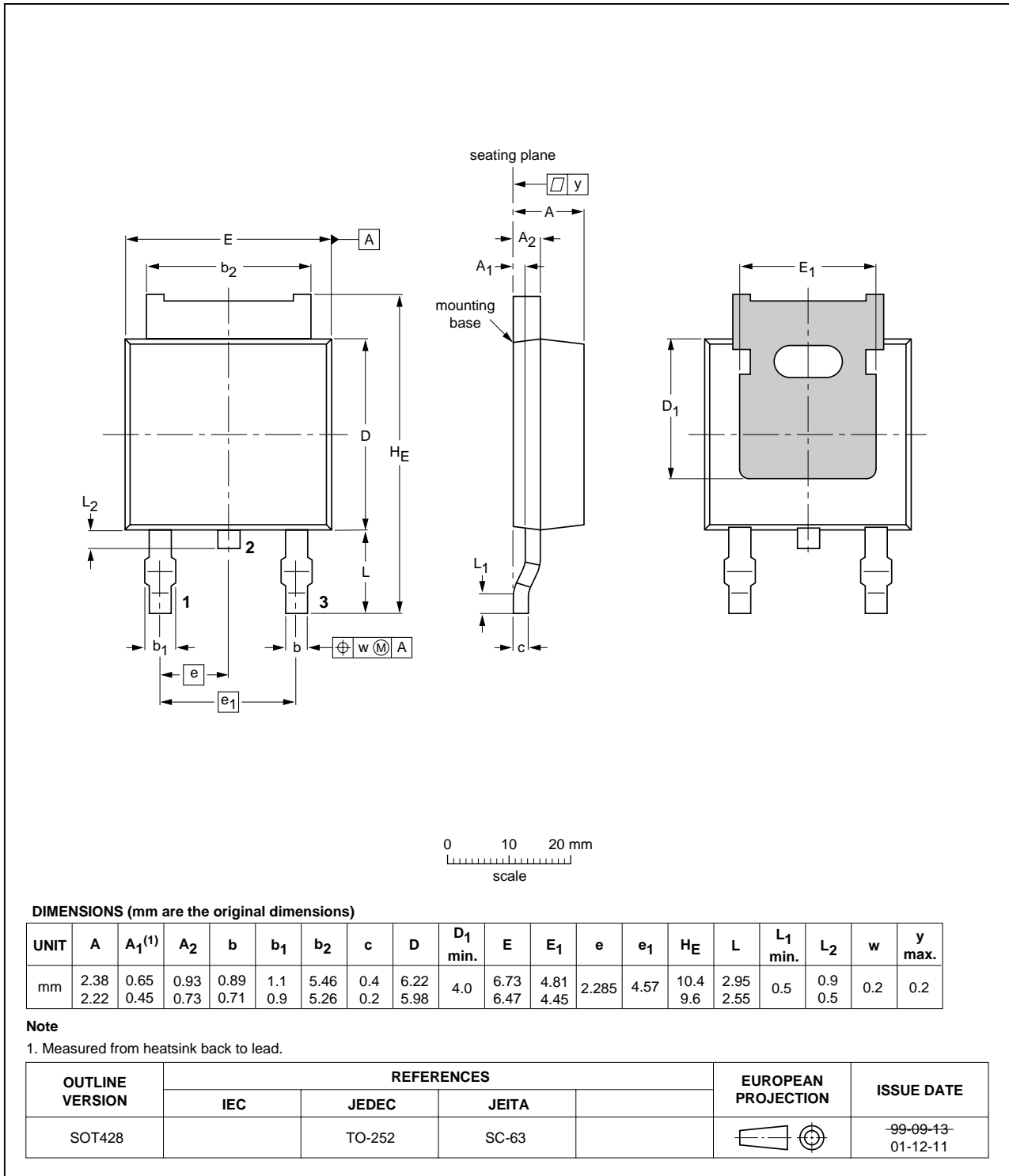


Fig 15. SOT428 (D-PAK) package outline.

8. Revision history

Table 6: Revision history

| Document ID | Release date | Data sheet status | Change notice | Document number | Supersedes |
|-----------------------|--------------|---|---------------|-----------------|-----------------------|
| PHB_PHD66NQ03LT_6 | 20040802 | Product data sheet | - | 9397 750 13429 | PHP_PHB_PHD66NQ03LT_5 |
| Modifications: | | <ul style="list-style-type: none"> • Removal of PHP66NQ03LT (now in separate data sheet) • Data sheet updated to latest standard. | | | |
| PHP_PHB_PHD66NQ03LT_5 | 20040415 | Product data sheet | - | 9397 750 13107 | PHP_PHB_PHD66NQ03LT_4 |
| PHP_PHB_PHD66NQ03LT_4 | 20020909 | Product data sheet | - | 9397 750 10158 | PHP_PHB_PHD66NQ03LT_3 |
| PHP_PHB_PHD66NQ03LT_3 | 20020312 | Product data sheet | - | 9397 750 09284 | PHP_PHB_PHD66NQ03LT_2 |
| PHP_PHB_PHD66NQ03LT_2 | 20011210 | Product data sheet | - | 9397 750 09119 | PHP_PHB_PHD66NQ03LT_1 |
| PHP_PHB_PHD66NQ03LT_1 | 20011012 | Product data sheet | - | 9397 750 08725 | - |

9. Data sheet status

| Level | Data sheet status ^[1] | Product status ^[2] ^[3] | Definition |
|-------|----------------------------------|--|--|
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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14. Contents

| | | |
|-----------|--------------------------------------|-----------|
| 1 | Product profile | 1 |
| 1.1 | General description | 1 |
| 1.2 | Features | 1 |
| 1.3 | Applications | 1 |
| 1.4 | Quick reference data | 1 |
| 2 | Pinning information | 1 |
| 3 | Ordering information | 2 |
| 4 | Limiting values | 2 |
| 5 | Thermal characteristics | 4 |
| 5.1 | Transient thermal impedance | 4 |
| 6 | Characteristics | 5 |
| 7 | Package outline | 9 |
| 8 | Revision history | 11 |
| 9 | Data sheet status | 12 |
| 10 | Definitions | 12 |
| 11 | Disclaimers | 12 |
| 12 | Trademarks | 12 |
| 13 | Contact information | 12 |



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