

### ■ General Description

The ATPA02G is a power sequence controller for AMD K8 processor. This part can mainly control the power supply relationships during power up, power down, entry and exit of any power management state in order to avoid damage to the device and ensure proper operation of the device.

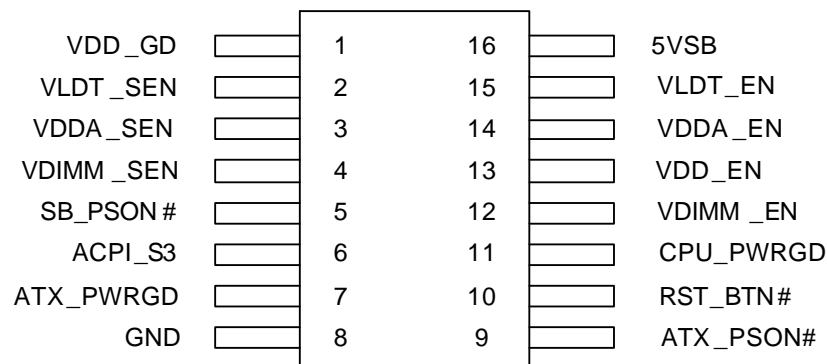
### ■ Features

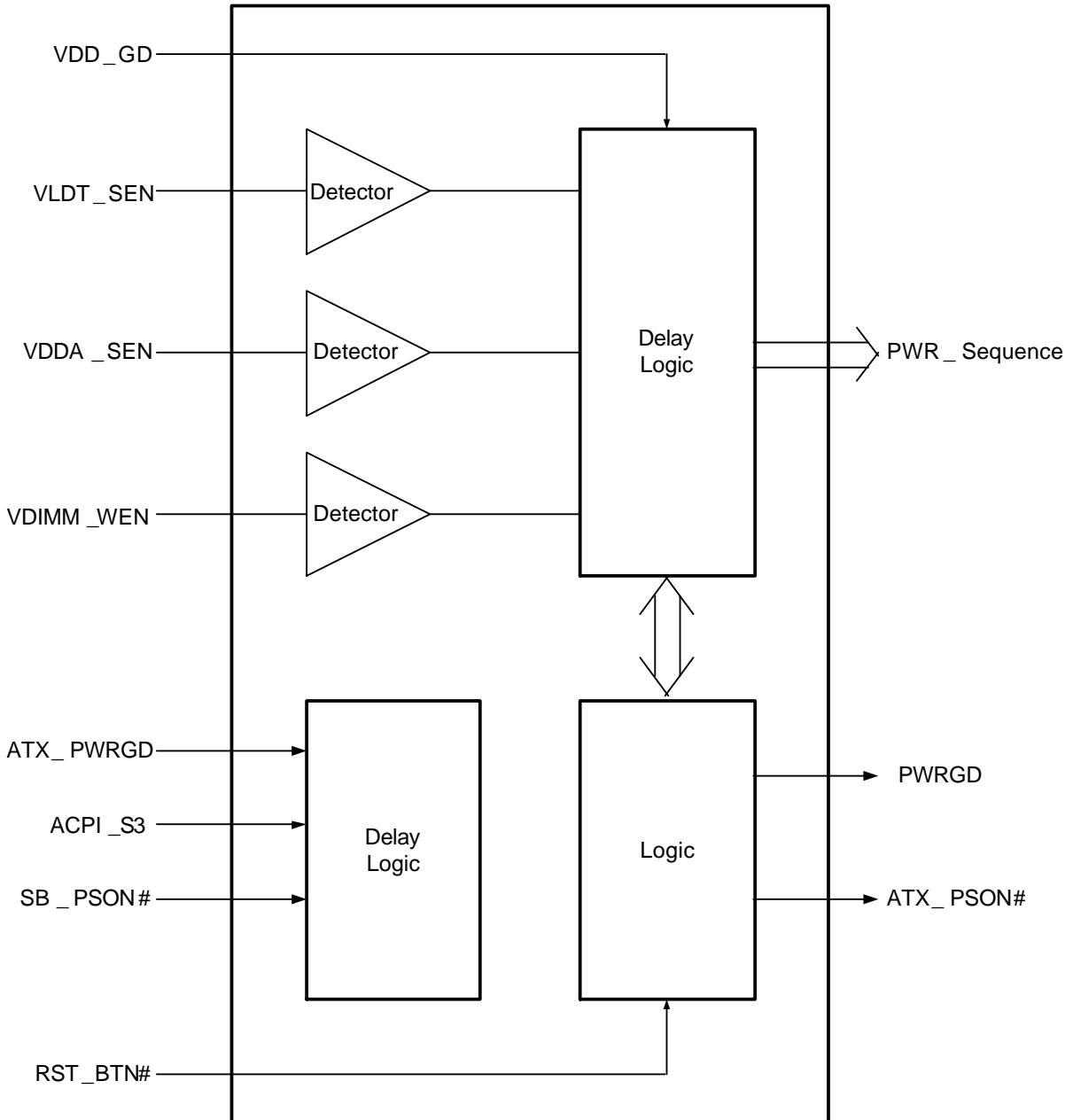
- Provides a Complete Power Sequence Controller
- Supports DDR ACPI-STR Functions
- Under-Voltage Fault Monitor
- Package: SOP-16
- Green Package
- All AME's Lead Free Products Meet RoHS Standards

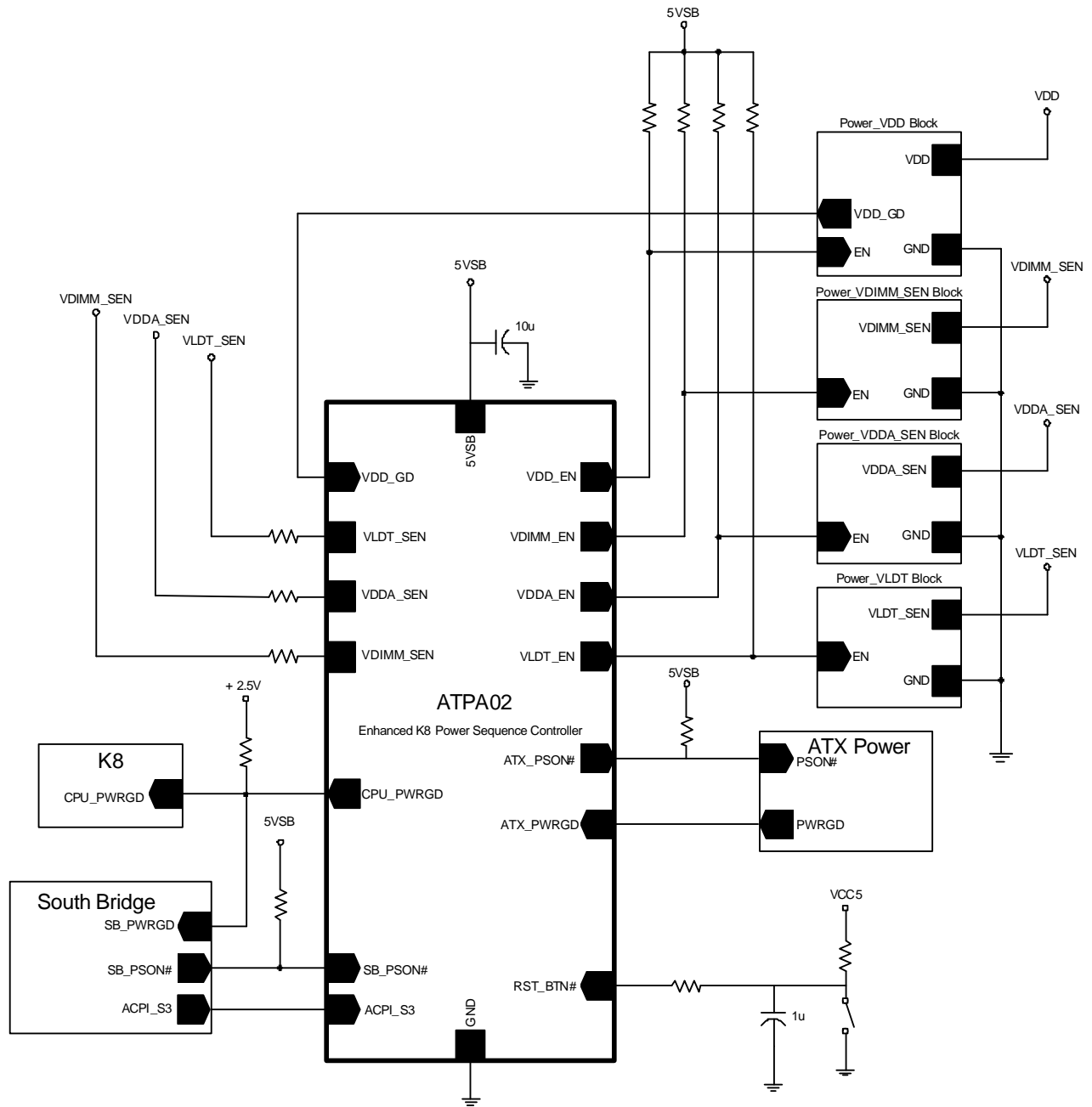
### ■ Application

- Motherboard
- Desktop system

### ■ Pin Configuration



**■ Function Block Diagram**


**■ Application Circuit**


**■ Pin Description**

I/O Type	Function
IN <sub>t</sub>	TTL level input
IN <sub>a</sub>	Analog input
OD <sub>70</sub>	Open-drain with 70mA sink current

Pin No.	Pin Name	I/O Type	Function
1	VDD_GD	IN <sub>t</sub>	Active-High of this signal indicates VDD voltage is valid. This signal is usually connected to the power-good output of the PWM for CPU core voltage
2	VLDT_SEN	IN <sub>a</sub>	This pin is used to detect the ClawHammer VLDT (1.2V) power or power-good signal.
3	VDDA_SEN	IN <sub>a</sub>	This pin is used to detect the ClawHammer VDDA (2.5V) power or power-good signal.
4	VDIMM_SEN	IN <sub>a</sub>	This pin is used to detect the VDIMM (2.5V/1.8V) power or power-good signal.
5	SB_PSON#	IN <sub>t</sub>	Active low. This signal is connected to the PSON# signal from the SB or Super I/O to control the on/off of ATX power supply.
6	ACPI_S3	IN <sub>t</sub>	Active high. This signal indicates that the system is in S3 state.
7	ATX_PWRGD	IN <sub>t</sub>	Active-High of this signal indicates all of the voltage from the ATX power supply is valid.
8	GND		Ground
9	ATX_PSON#	OD <sub>70</sub>	Active low. This pin is used to control the on/off of ATX power supply. Active-Low of this signal will turn on the ATX power supply. This pin is open-drain output and should be pulled-up via a resistor to 5VSB externally.
10	RST_BTN#	IN <sub>t</sub>	Active low. This function is panel reset button input with de-bounce circuit.
11	CPU_PWRGD	OD <sub>70</sub>	Active high. This signal is connected to the Claw Hammer to indicate all system powers are valid. This pin is open-drain output and should be pulled-up externally via a resistor to 2.5V.

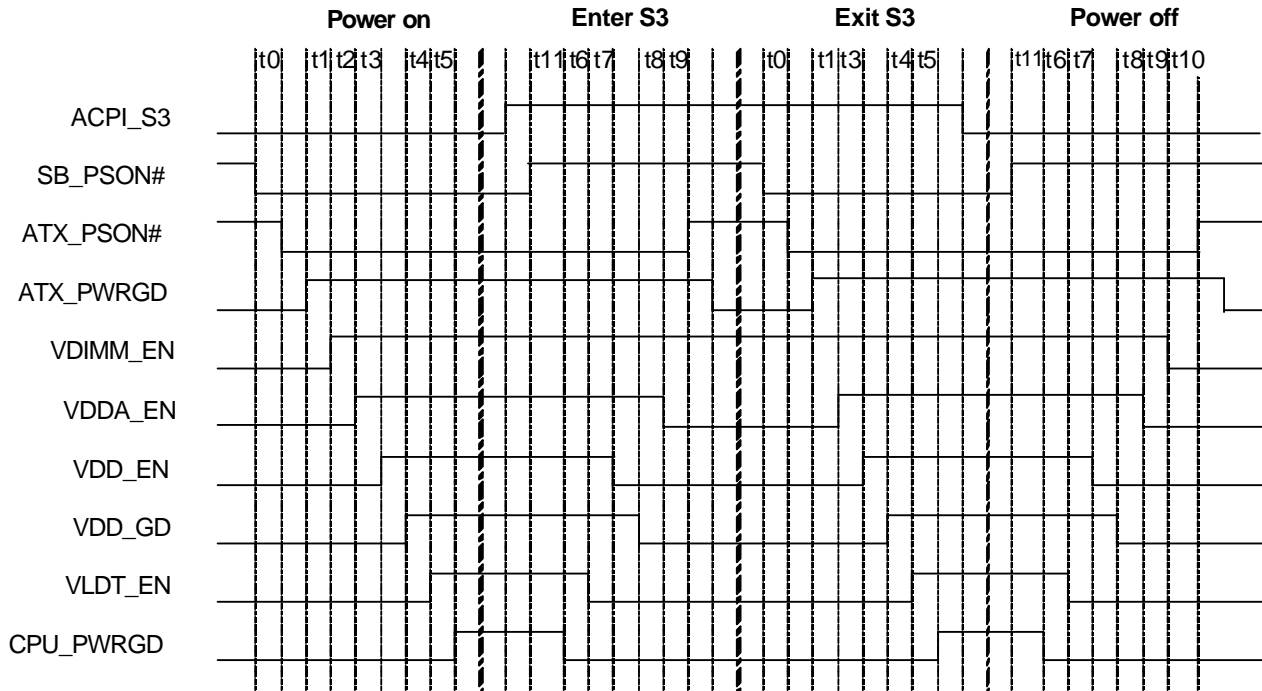
**■ Pin Description (Contd.)**

Pin No.	Pin Name	I/O Type	Function
12	VDIMM_EN	OD <sub>70</sub>	Active high. This pin is used to enable the function of the PWM for VDIMM voltage generation.
13	VDD_EN	OD <sub>70</sub>	Active high. This pin is used to enable the function of the PWM for VDD voltage generation.
14	VDDA_EN	OD <sub>70</sub>	Active high. This pin is used to enable the function of the VDDA power for ClawHammer.
15	VLDT_EN	OD <sub>70</sub>	Active high. This pin is used to enable the function of the VLDT power for ClawHammer.
16	5VSB		Power

**■ Ordering Information**

Part Number	Marking	Package	Operating Ambient Temperature Range
ATPA02G	ATPA02G yyww AB xxxxxxx ##	SOP-16	- 30°C to 85°C

Note: yy:year (last two digits)  
 ww:week  
 xxxxxxx:wafer lot number  
 ##:wafer number (It is a representative if a string of wafer are used.)

**■ Time Sequence**

**■ AC Timing Parameter**

Item	Description	Timing		
		Min	Typical	Max
t0	SB_PSON# falling to ATX_PSON# falling	1μs	3μs	6μs
t1	ATX_PWRGD rising to VDIMM_EN rising	40μs	60μs	80μs
t2	VDIMM_SEN rising to VDDA_EN rising	150ms	190ms	230ms
t3	VDDA_SEN rising to VDD_EN rising	3ms	4ms	5ms
t4	VDD_GD rising to VLDT_EN rising	3ms	4ms	5ms
t5	VLDT_SEN rising to CPU_PWRGD rising	3ms	4ms	5ms
t6	CPU_PWRGD falling to VLDT_EN falling	3ms	4ms	5ms
t7	VLDT_SEN falling (0.85V) to VDD_EN falling	7ms	10ms	13ms
t8	VDD_GD falling to VDDA_EN falling	315ms	400ms	485ms
t9	VDDA_SEN falling to VDIMM_EN falling	7ms	10ms	13ms
t10	VDIMM_SEN falling to ATX_PSON# rising	150ms	190ms	230ms
t11	SB_PSON# rising to CPU_PWRGD falling	3ms	4ms	5ms

Note: All specified timing is simulated at pull\_up resistor 9K, w/o power capacitance.

**■ Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Power Supply	V <sub>CC</sub>	-0.5V to 7V	V
Input Voltage	V <sub>CC</sub>	-0.5V to V <sub>CC</sub> +0.5V	V
Output Voltage	V <sub>CC</sub>	-0.5V to V <sub>CC</sub> +0.5V	V

Note: Exceeding the absolute maximum rating may damage the device.

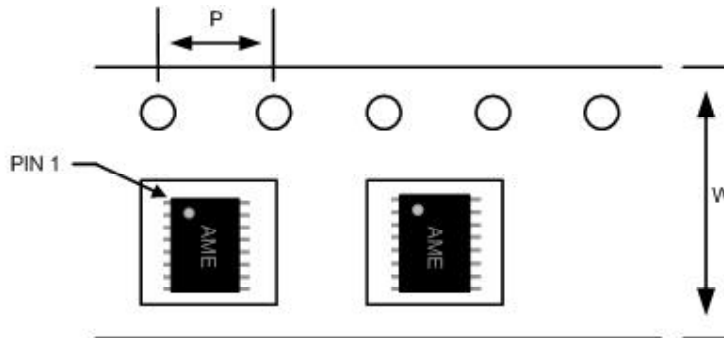
**■ Recommended Operation Conditions**

Parameter	Symbol	Rating	Unit
Ambient Temperature Range	T <sub>A</sub>	- 30 to 85	°C
Storage Temperature Range	T <sub>STG</sub>	- 55 to 125	°C

**■ Electrical Specifications**

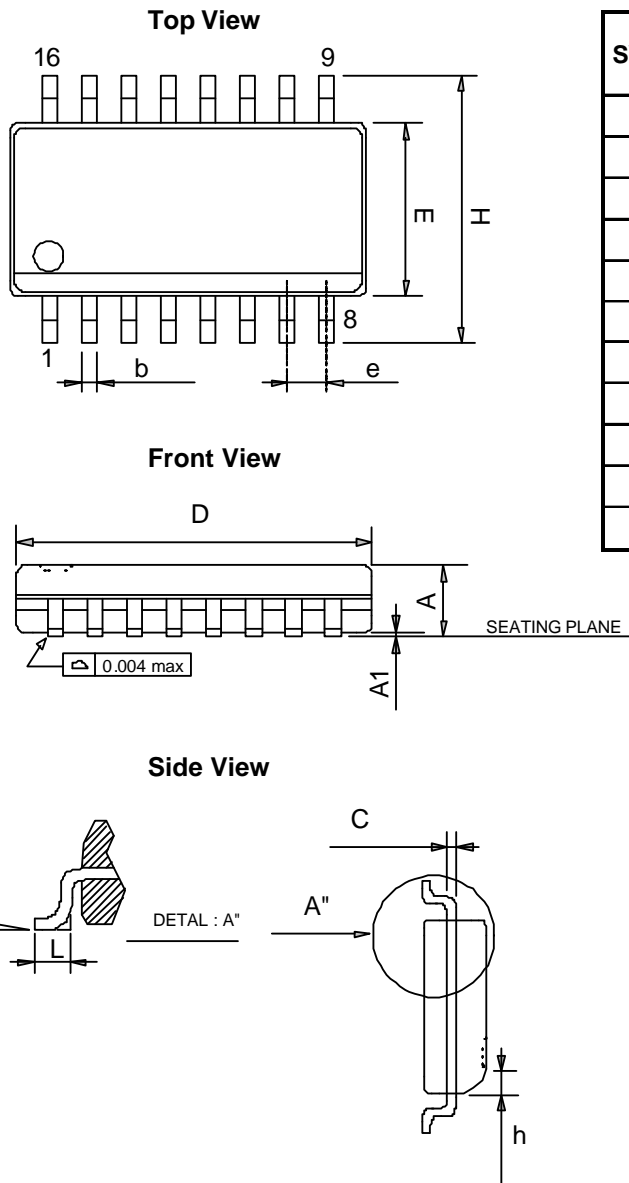
V<sub>CC</sub>=5V, T<sub>A</sub>=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Trigger point for VDIMM_SEN	V <sub>TRIG</sub>	V <sub>CC</sub> =5.25V		1.85		V
		V <sub>CC</sub> =5V		1.75		V
		V <sub>CC</sub> =4.75V		1.65		V
Trigger point for VDDA_SEN	V <sub>TRIG, VDDA</sub>	V <sub>CC</sub> =5.25V		2.3		V
		V <sub>CC</sub> =5V		2.2		V
		V <sub>CC</sub> =4.75V		2.1		V
Hysteresis for VDDA_SEN and VDIMM_SEN	V <sub>HYST</sub>			100		mV
Trigger point for VLDT_SEN	V <sub>TRIG, LDT</sub>	V <sub>CC</sub> =5.25V		0.88		V
		V <sub>CC</sub> =5V		0.85		V
		V <sub>CC</sub> =4.75V		0.83		V
Hysteresis for VLDT_SEN	V <sub>HYST, LDT</sub>			100		mV
Logic High Level	V <sub>IH</sub>		2			V
Logic Low Level	V <sub>IL</sub>				0.8	V

**■ Tape and Reel Dimension**
**SOP-16**

**Carrier Tape, Number of Components Per Reel and Reel Size**

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
SOP-16	12.0±0.1 mm	4.0±0.1 mm	2500pcs	330±1 mm



**■ Package Dimension**
**SOP-16**


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.40TYP		0.016TYP	
C	0.20TYP		0.008TYP	
e	1.27TYP		0.050TYP	
E	3.81	4.00	0.150	0.157
D	9.80	10.00	0.386	0.394
h	0.38TYP		0.015TYP	
H	5.80	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
q	0°	8°	0°	8°



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