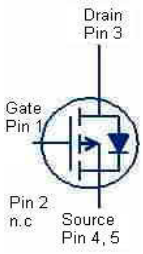
OptiMOS®-P Power-Transistor

Features

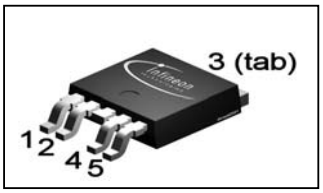
- P-Channel
- Enhancement mode
- Logic level
- 175°C operating temperature
- Avalanche rated
- d*v*/d*t* rated
- High current rating
- Pb-free lead-plating, RoHS compliant

Product Summary

V_{DS}	-30	V
$R_{DS(on),max}$	7	mΩ
I_D	-50	A



PG-TO252-5



Type	Package	Marking	Lead Free
SPD50P03L G	PG-TO252-5	50P03L	Yes

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[1)]	-50	A
		T_C=100 °C[1)]	-50	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C	-200	
Avalanche energy, single pulse	E_{AS}	I_D=-50 A, R_{GS}=25 Ω	256	mJ
Reverse diode d*v*/d*t*	d*v*/d*t*	I_D=-50 A, V_{DS}=24 V, d*i*/d*t*=-200 A/µs, $T_{j,max}$=175 °C	-6	kV/µs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	150	W
Operating and storage temperature	T_j, T_{stg}		-55…+175	°C
ESD class HBM			1C	
Soldering temperature			260	
IEC climatic category; DIN IEC 68-1			55/175/56	

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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	75	
		6 cm^2 cooling area[2)]	-	-	50	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=-250 µA	-30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250 µA	-1	-1.5	-2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=-30 V, V_{GS}=0 V, T_j=25 °C	-	-0.1	-1	µA
		V_{DS}=-30 V, V_{GS}=0 V, T_j=175 °C	-	-10	-100	
Gate-source leakage current	I_{GSS}	V_{GS}=-20 V, V_{DS}=0 V	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=-4.5 V, I_D=-30 A	-	8.5	12.5	mΩ
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=-10 V, I_D=-50 A	-	5.7	7.0	
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=-50 A	47	94	-	S

[1)] Current is limited by bondwire; with an R_{thJC}=1 K/W the chip is able to carry 123 A.

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=-25 V, f=1 MHz	-	4590	6880	pF
Output capacitance	C_{oss}		-	1220	1830	
Reverse transfer capacitance	C_{rss}		-	1000	1500	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-15 V, V_{GS}=-10 V, I_D=-1 A, R_G=6 Ω	-	14.8	22	ns
Rise time	t_r		-	21.7	32	
Turn-off delay time	$t_{d(off)}$		-	139	208	
Fall time	t_f		-	104	156	
Gate Charge Characteristics[3)]						
Gate to source charge	Q_{gs}	V_{DD}=-24 V, I_D=-50 A	-	-14	-19	nC
Gate to drain charge	Q_{gd}		-	-35	-53	
Gate charge total	Q_g	V_{DD}=-24 V, I_D=-50 A, V_{GS}=0 to -10 V	-	-95	-126	
Gate plateau voltage	$V_{plateau}$	V_{DD}=-24 V, I_D=-50 A	-	-3.0	-	V
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	-50	A
Diode pulse current	$I_{S,pulse}$		-	-	-200	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=50 A, T_j=25 °C	-	-1	-1.65	V
Reverse recovery time	t_{rr}	V_R=-15 V, I_F=$\|I_S\|$, di_F/dt=100 A/µs	-	38	47	ns
Reverse recovery charge	Q_{rr}		-	46	57	nC

[3)] See figure 16 for gate charge parameter definition

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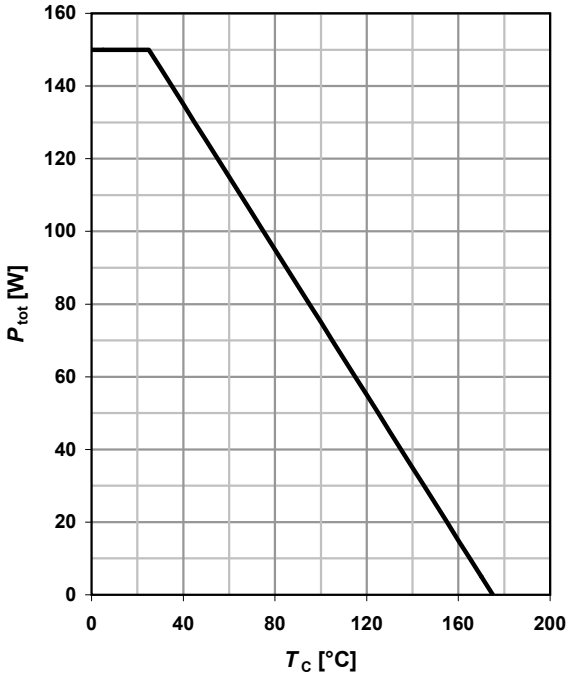
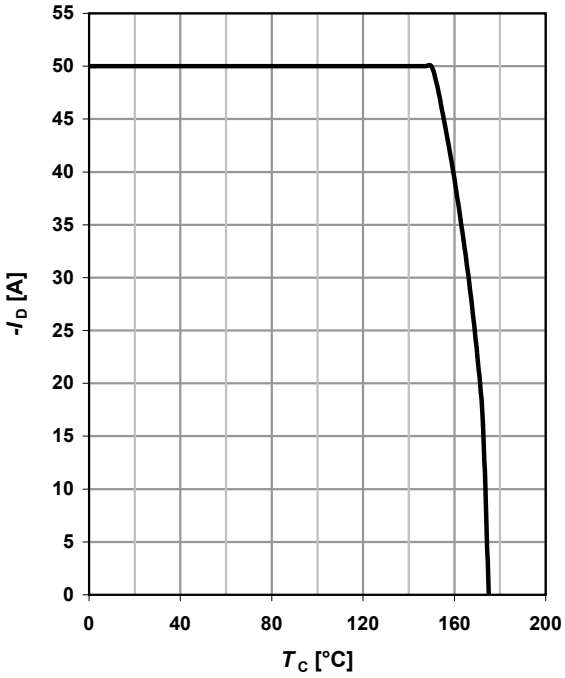
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

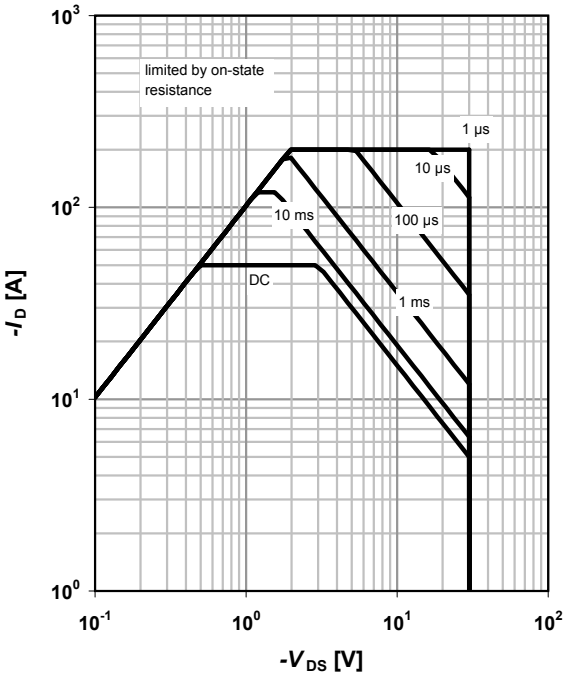
$I_D=f(T_C)$; $|V_{GS}|\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

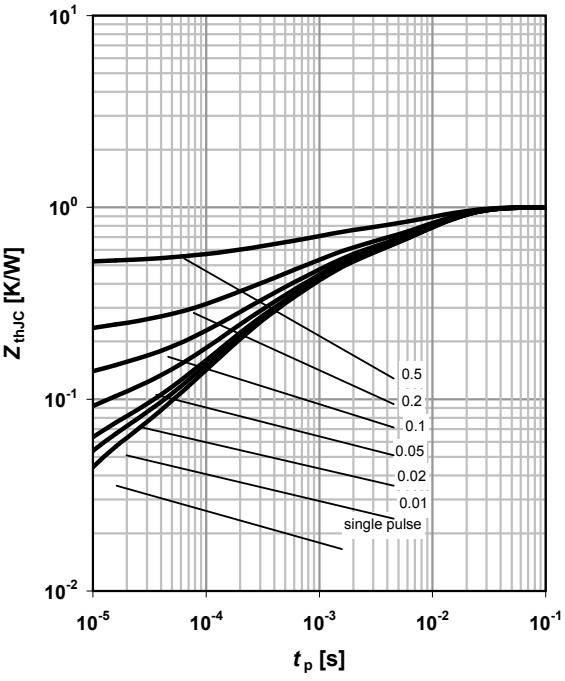
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

parameter: $D=t_p/T$



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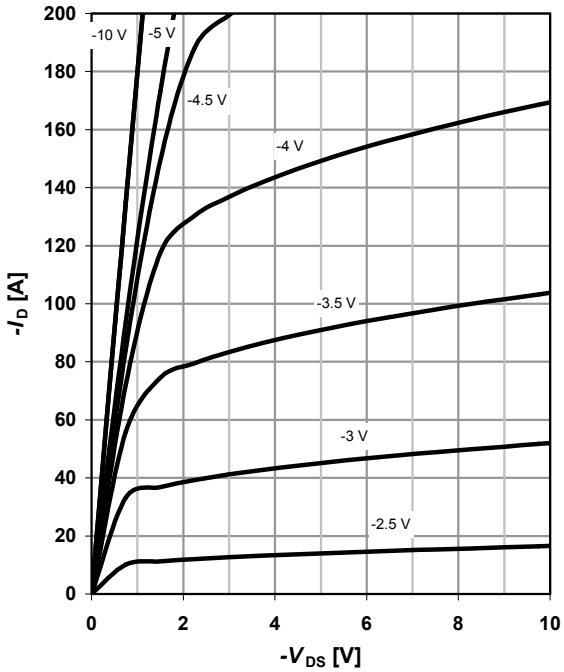
5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

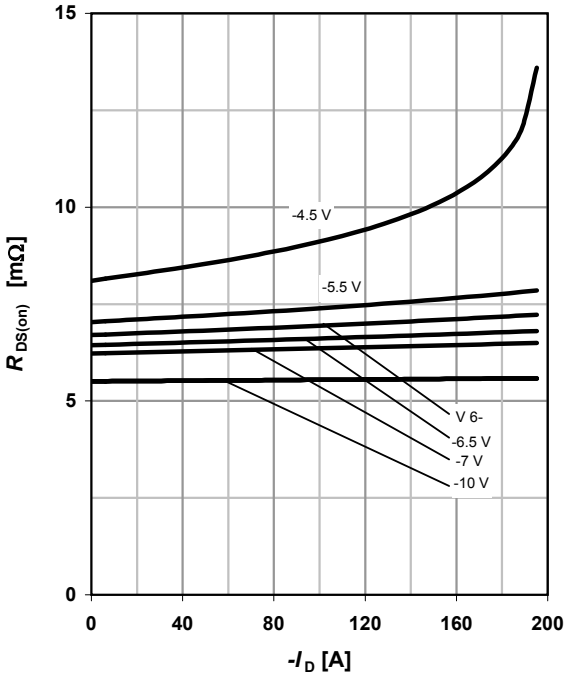
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

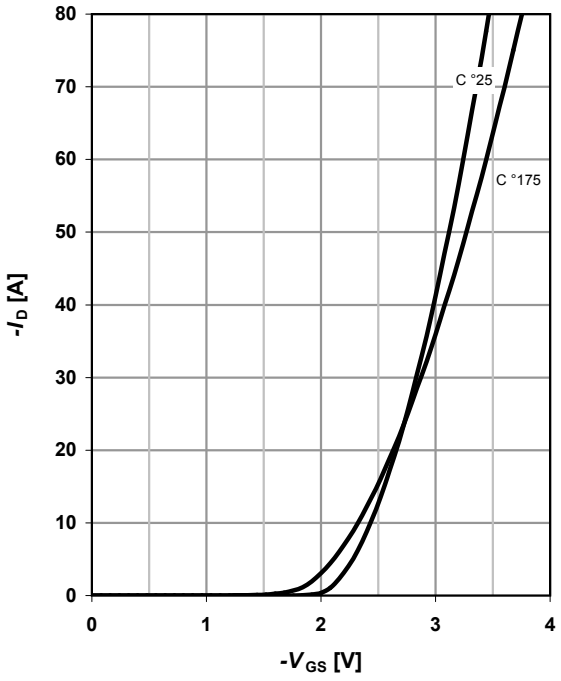
parameter: V_{GS}



7 Typ. transfer characteristics

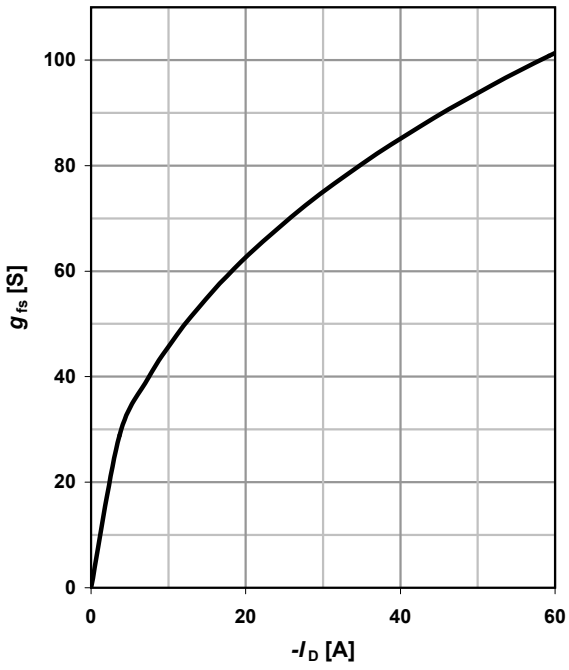
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



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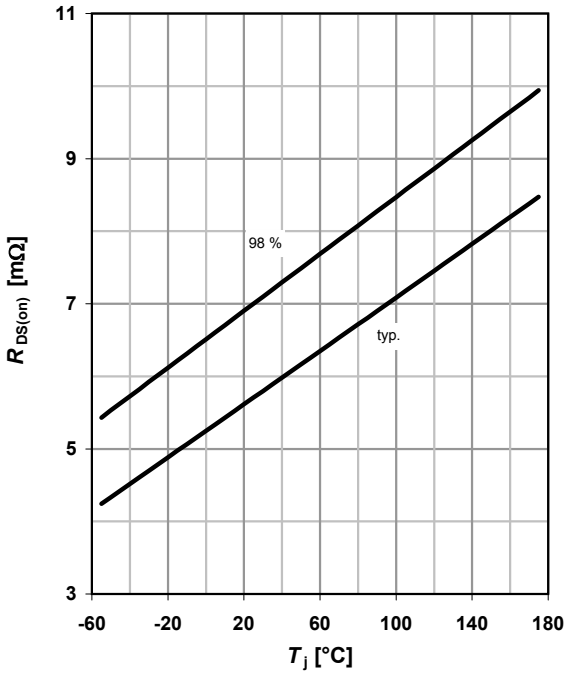
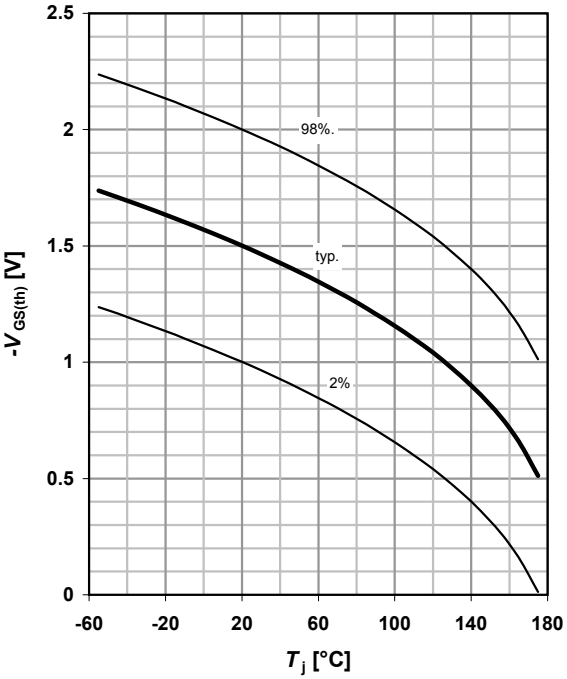
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=-50 A; V_{GS}=-10 V



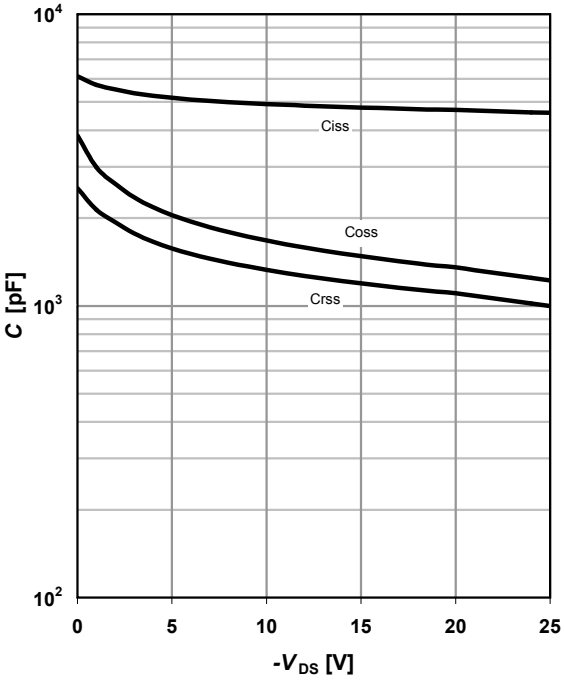
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=-250 µA



11 Typ. capacitances

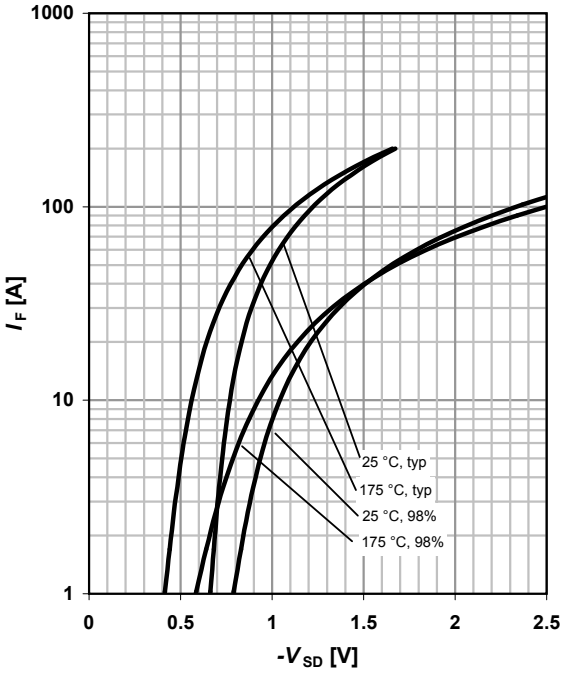
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

parameter: T_j



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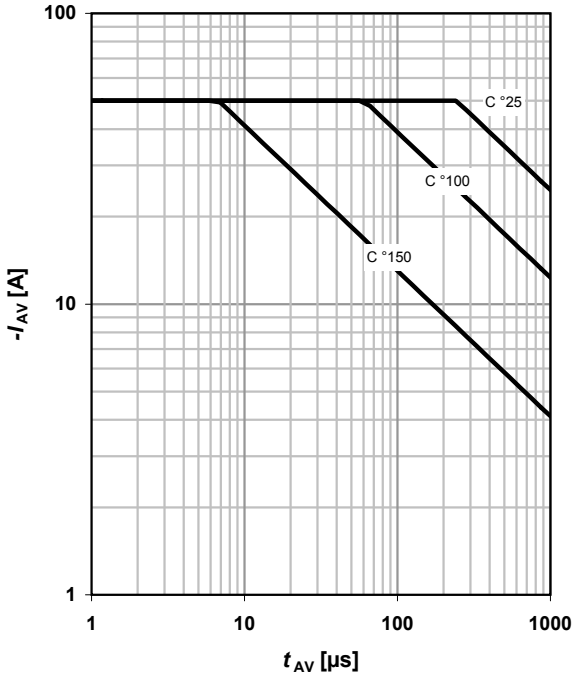
13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

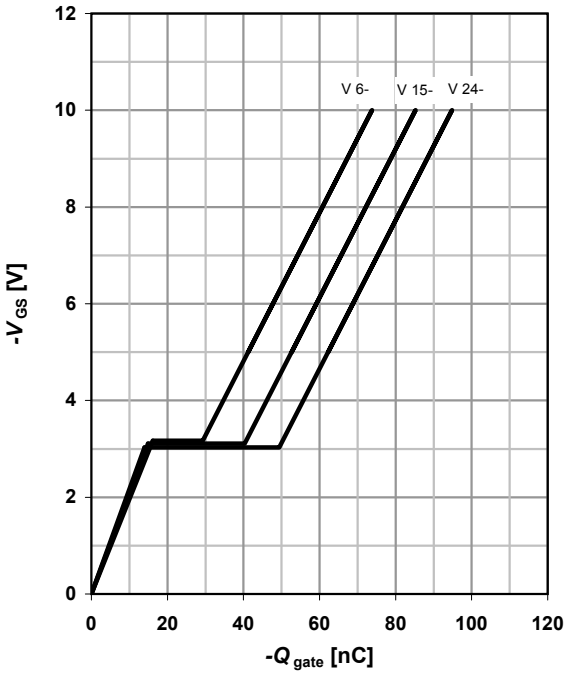
parameter: $T_{j(start)}$



14 Typ. gate charge

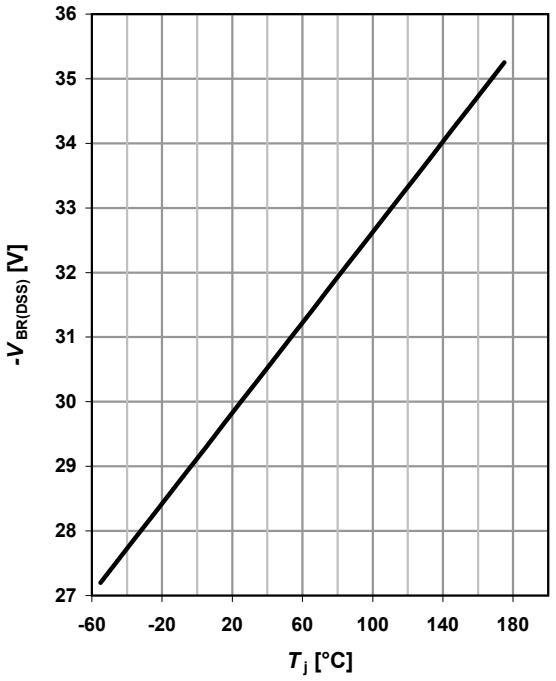
V_{GS}=f(Q_{gate}); I_D=-50 A pulsed

parameter: V_{DD}

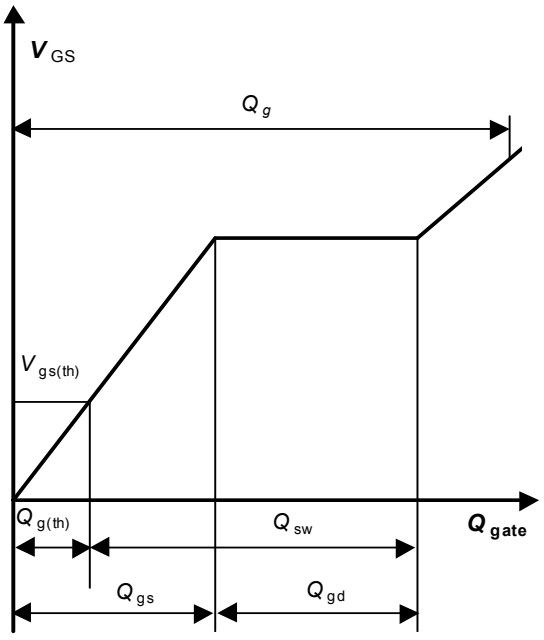


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=-250 µA



16 Gate charge waveforms



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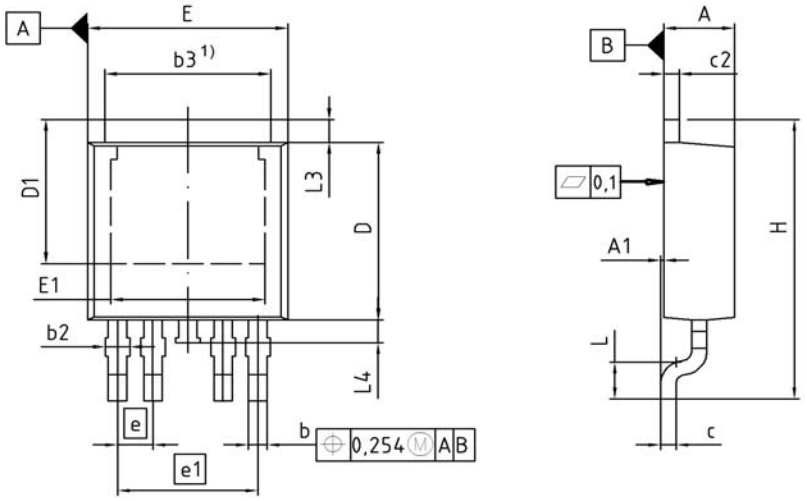
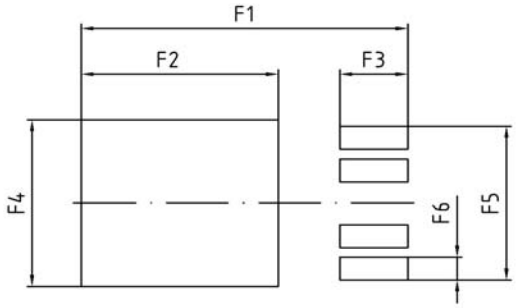
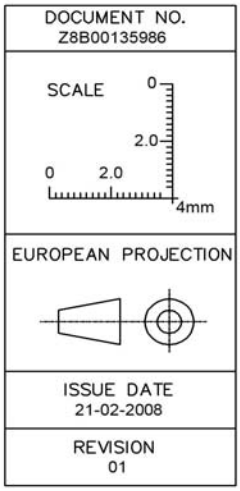
Package Outline PG-TO252-5





Remark:
1) does not include mold flash

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.35	0.087	0.093
A1	0.00	0.15	0.000	0.006
b	0.50	0.70	0.020	0.028
b2	0.50	0.85	0.020	0.033
b3	5.30	5.50	0.209	0.217
c	0.46	0.58	0.018	0.023
c2	0.46	0.58	0.018	0.023
D	6.02	6.22	0.237	0.245
D1	5.14	5.34	0.202	0.210
E	6.45	6.65	0.254	0.262
E1	4.90	5.10	0.193	0.201
e	1.14		0.045	
e1	4.56		0.180	
N	5		5	
H	9.48	10.48	0.373	0.413
L	1.20	1.40	0.047	0.055
L3	0.90	1.10	0.035	0.043
L4	0.65	0.95	0.026	0.037
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.26	5.46	0.207	0.215
F6	0.70	0.90	0.028	0.035



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