# **Power MOSFET**

-30 V, -1.95 A, Single, P-Channel, SOT-23

## **Features**

- Leading Planar Technology for Low Gate Charge / Fast Switching
- Low R<sub>DS(ON)</sub> for Low Conduction Losses
- SOT-23 Surface Mount for Small Footprint (3 X 3 mm)
- Pb–Free Package May be Available. The G–Suffix Denotes a Pb–Free Lead Finish

## **Applications**

- DC to DC Conversion
- Load/Power Switch for Portables and Computing
- Motherboard, Notebooks, Camcorders, Digital Camera's, etc.
- Battery Charging Circuits

## **MAXIMUM RATINGS** (T<sub>.I</sub> = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	-30	V
Gate-to-Source Voltage			V <sub>GS</sub>	-20	V
Drain Current (Note 1)	t < 10 s T <sub>A</sub> = 25°C		I <sub>D</sub>	-1.95	Α
		T <sub>A</sub> = 70°C		-1.56	
Power Dissipation (Note 1)	t < 10 s		P <sub>D</sub>	1.25	W
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}C$	I <sub>D</sub>	-1.13	Α
		T <sub>A</sub> = 70°C		-0.90	
Power Dissipation (Note 1)	Stead	dy State	P <sub>D</sub>	0.4	W
Pulsed Drain Current	t <sub>p</sub> =	10 μs	I <sub>DM</sub>	-6.8	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	–55 to 150	ô
Source Current (Body Diode)			I <sub>S</sub>	-1.25	Α
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)			TL	260	°C

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	300	°C/W
Junction-to-Ambient - t = 10 s (Note 1)	$R_{ heta JA}$	100	

<sup>1.</sup> Surface–mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).

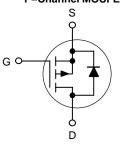


## ON Semiconductor®

## http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> Max (Note 1)	
-30 V	155 mΩ @ –10 V	4.05.4	
	240 mΩ @ -4.5 V	–1.95 A	

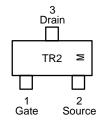
## P-Channel MOSFET



## MARKING DIAGRAM/ PIN ASSIGNMENT



**SOT-23 CASE 318** *Style 21* 



TR2 = Specific Device Code M = Date Code

## **ORDERING INFORMATION**

Device	Package	Shipping†
NTR4502PT1	SOT-23	3000 / Tape & Reel
NTR4502PT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NTR4502PT3	SOT-23	10000 / Tape & Reel
NTR4502PT3G	SOT-23 (Pb-Free)	10000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## **Electrical Characteristics** ( $T_J = 25$ °C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS						-	
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$		-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = -30 \text{ V}$	T <sub>J</sub> = 25°C			-1	μΑ
			T <sub>J</sub> = 55°C			-10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20$	V			±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_{D} = -250$	μΑ	-1.0		-3.0	V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	$V_{GS} = -10 \text{ V}, I_D = -1.9$	5 A		155	200	mΩ
		$V_{GS} = -4.5 \text{ V}, I_D = -1.5 \text{ A}$			240	350	
Forward Transconductance	9FS	$V_{DS} = -10 \text{ V}, I_{D} = -1.25 \text{ A}$			3		S
CHARGES AND CAPACITANCES	•						•
Input Capacitance	C <sub>ISS</sub>	$V_{GS} = 0 \text{ V, f} = 1 \text{ MHz, } V_{DS} = -15 \text{ V}$			200		pF
Output Capacitance	C <sub>OSS</sub>				80		1
Reverse Transfer Capacitance	C <sub>RSS</sub>				50		
Total Gate Charge	Q <sub>G(TOT)</sub>	$V_{GS} = -10 \text{ V}, V_{DS} = -15 \text{ V}; I_{D} = -1.95 \text{ A}$			6	10	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>				0.3		
Gate-to-Source Charge	Q <sub>GS</sub>				1		
Gate-to-Drain Charge	$Q_{GD}$				1.7		
SWITCHING CHARACTERISTICS (Note	4)						•
Turn-On Delay Time	t <sub>d(ON)</sub>	$V_{GS} = -10 \text{ V}, V_{DD} = -19 \text{ I}_{D} = -195 \text{ A}, R_{G} = 6 \text{ A}$	5 V,		5.2	10	ns
Rise Time	t <sub>r</sub>	$I_D = -1.95 \text{ A}, R_G = 6 \Omega$			12	20	1
Turn-Off Delay Time	t <sub>d(OFF)</sub>				19	35	1
Fall Time	t <sub>f</sub>				17.5	30	1
DRAIN-SOURCE DIODE CHARACTERIS	STICS (Note 3)						
Forward Diode Voltage	V <sub>SD</sub>	$V_{GS} = 0 \text{ V, } I_S = -1.25 \text{ A}$			-0.8	-1.2	V
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V}, dI_{SD}/d_t = 100 \text{ A/}\mu\text{s}, I_S = -1.25 \text{ A}$			23		ns

Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).
 Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

-ID, DRAIN CURRENT (A)

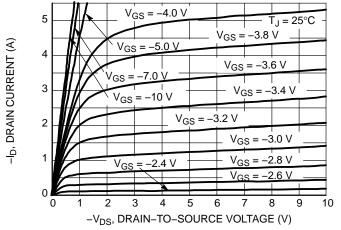


Figure 1. On-Region Characteristics

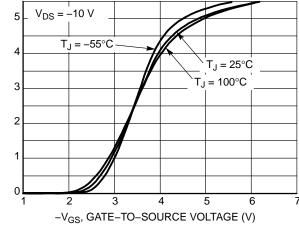


Figure 2. Transfer Characteristics

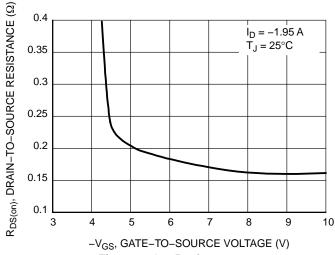


Figure 3. On–Resistance versus Gate–to–Source Voltage

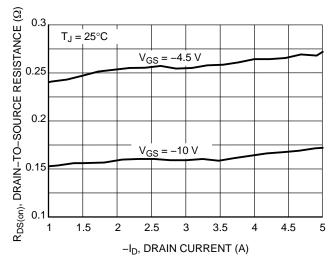


Figure 4. On-Resistance versus Drain Current and Gate Voltage

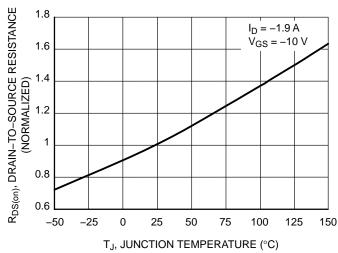


Figure 5. On–Resistance Variation with Temperature

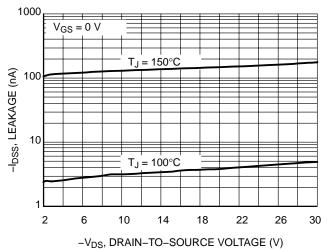


Figure 6. Drain-to-Source Leakage Current versus Voltage

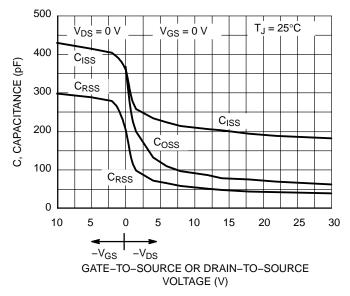


Figure 7. Capacitance Variation

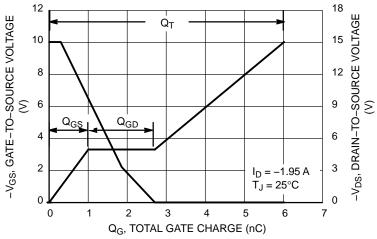


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

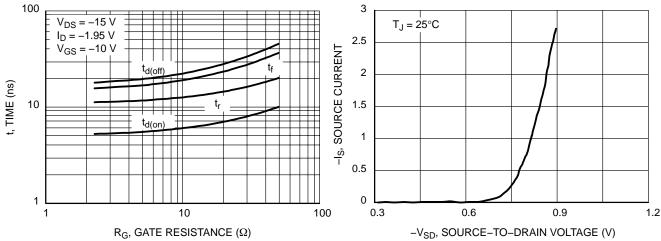
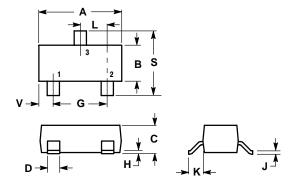


Figure 9. Resistive Switching Time Variation versus Gate Resistance

Figure 10. Diode Forward Voltage versus Current

## **PACKAGE DIMENSIONS**

SOT-23 (TO-236)CASE 318-08 **ISSUE AK** 



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF PASE MATERIAL
- BASE MATERIAL.
  4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

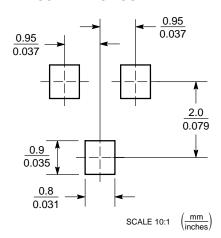
	INCHES		MILLIM	ETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.1102	0.1197	2.80	3.04	
В	0.0472	0.0551	1.20	1.40	
С	0.0350	0.0440	0.89	1.11	
D	0.0150	0.0200	0.37	0.50	
G	0.0701	0.0807	1.78	2.04	
Н	0.0005	0.0040	0.013	0.100	
J	0.0034	0.0070	0.085	0.177	
K	0.0140	0.0285	0.35	0.69	
L	0.0350	0.0401	0.89	1.02	
S	0.0830	0.1039	2.10	2.64	
V	0.0177	0.0236	0.45	0.60	

STYLE 21:

PIN 1. GATE 2. SOURCE

- 3. DRAIN

## **SOLDERING FOOTPRINT\***



<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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