

AO3421
P-Channel Enhancement Mode Field Effect Transistor

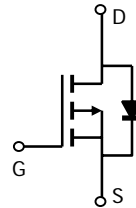
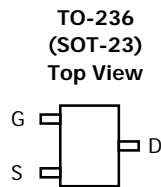
General Description

The AO3421/L uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. *AO3421 and AO3421L are electrically identical.*

- RoHS Compliant
- AO3421L is Halogen Free

Features

- $V_{DS} (V) = -30V$
- $I_D = -2.6 A (V_{GS} = -10V)$
- $R_{DS(ON)} < 130m\Omega (V_{GS} = -10V)$
- $R_{DS(ON)} < 200m\Omega (V_{GS} = -4.5V)$


Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	$T_A=25^\circ C$	-2.6	A
	$T_A=70^\circ C$	-2.2	
Pulsed Drain Current ^B	I_{DM}	-20	
Power Dissipation ^A	$T_A=25^\circ C$	1.4	W
	$T_A=70^\circ C$	1	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	70	90	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	100	125
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	63	80	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.4	-1.9	-3	V
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-5			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-2.6A T _J =125°C		97	130	mΩ
		V _{GS} =-4.5V, I _D =-2A		166	200	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-2.5A	3	3.8		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.82	-1	V
I _S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		302	370	pF
C _{oss}	Output Capacitance			50.3		pF
C _{riss}	Reverse Transfer Capacitance			37.8		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		12	18	Ω
SWITCHING PARAMETERS						
Q _{g(10)}	Total Gate Charge(10V)	V _{GS} =-10V, V _{DS} =-15V, I _D =-2.6A		6.8	9	nC
Q _{g(4.5)}	Total Gate Charge(4.5V)			2.4		nC
Q _{gs}	Gate Source Charge			1.6		nC
Q _{gd}	Gate Drain Charge			0.95		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =5.8Ω, R _{GEN} =3Ω		7.5		ns
t _r	Turn-On Rise Time			3.2		ns
t _{D(off)}	Turn-Off DelayTime			17		ns
t _f	Turn-Off Fall Time			6.8		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-2.6A, dI/dt=100A/μs		16.8	22	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-2.6A, dI/dt=100A/μs		10		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6,12,14 are obtained using <300μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

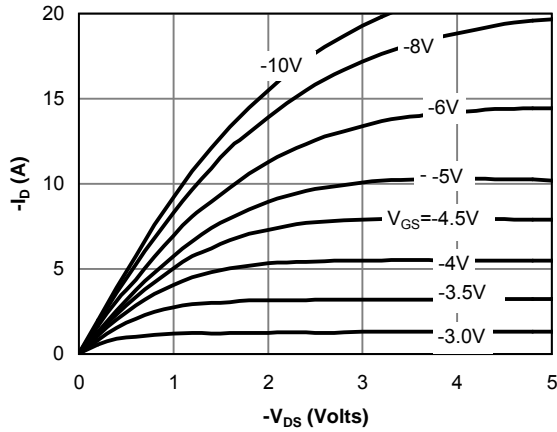


Fig 1: On-Region Characteristics

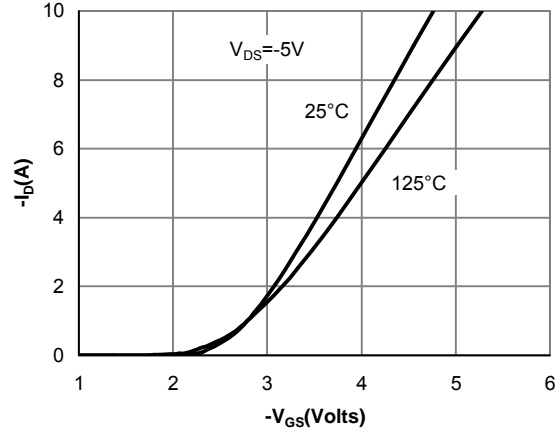


Figure 2: Transfer Characteristics

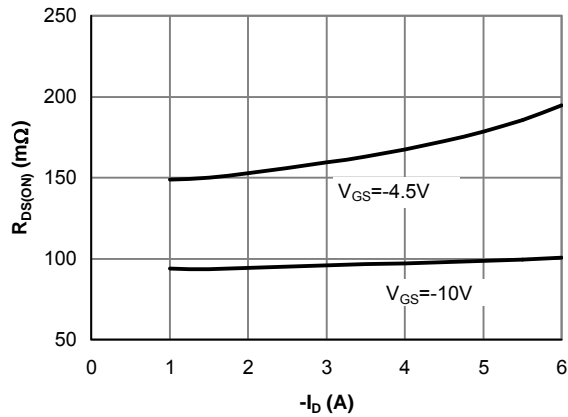


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

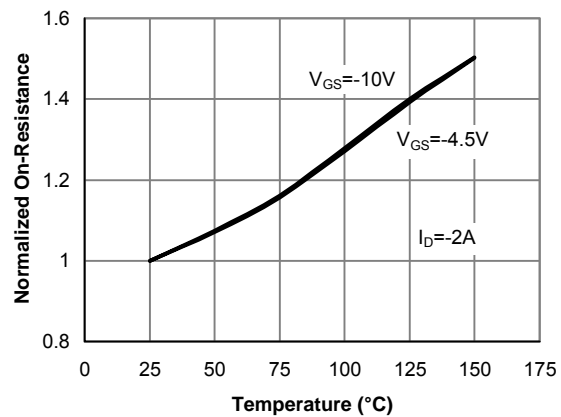


Figure 4: On-Resistance vs. Junction Temperature

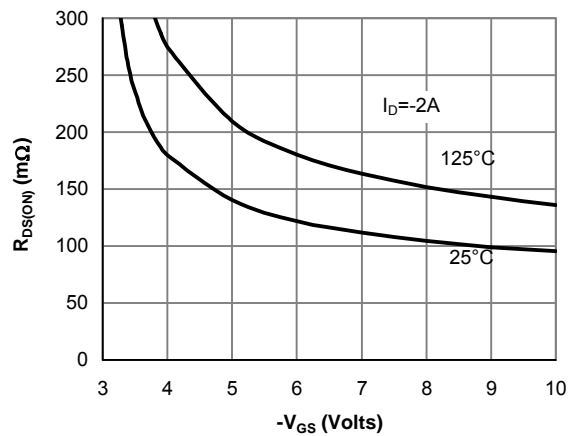


Figure 5: On-Resistance vs. Gate-Source Voltage

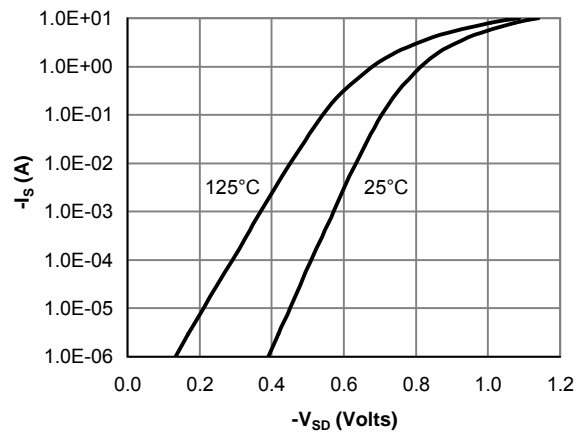


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

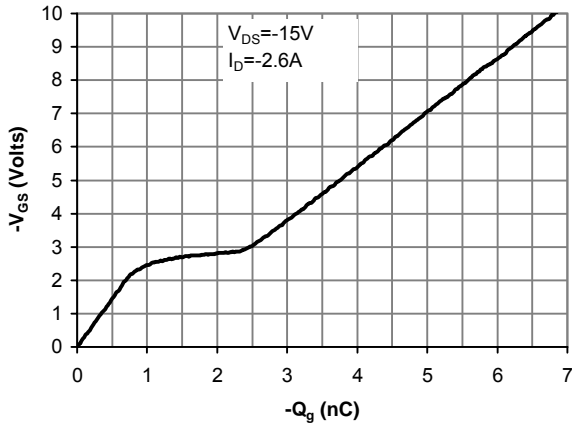


Figure 7: Gate-Charge Characteristics

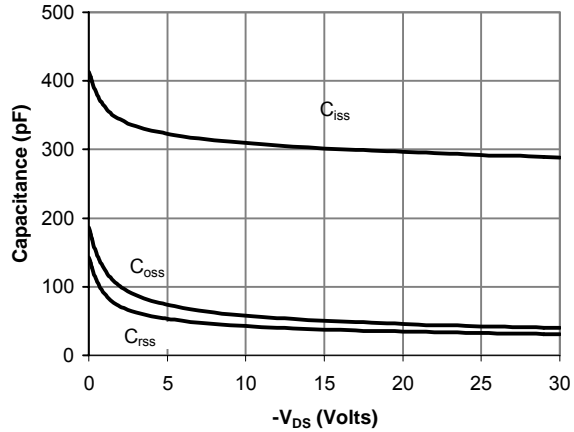


Figure 8: Capacitance Characteristics

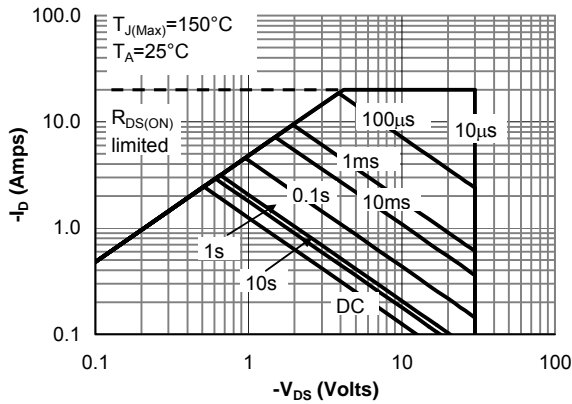


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

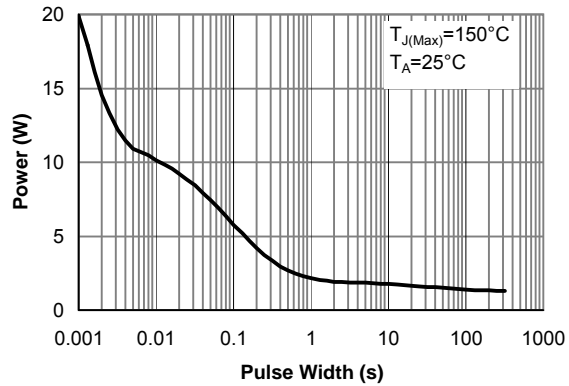


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

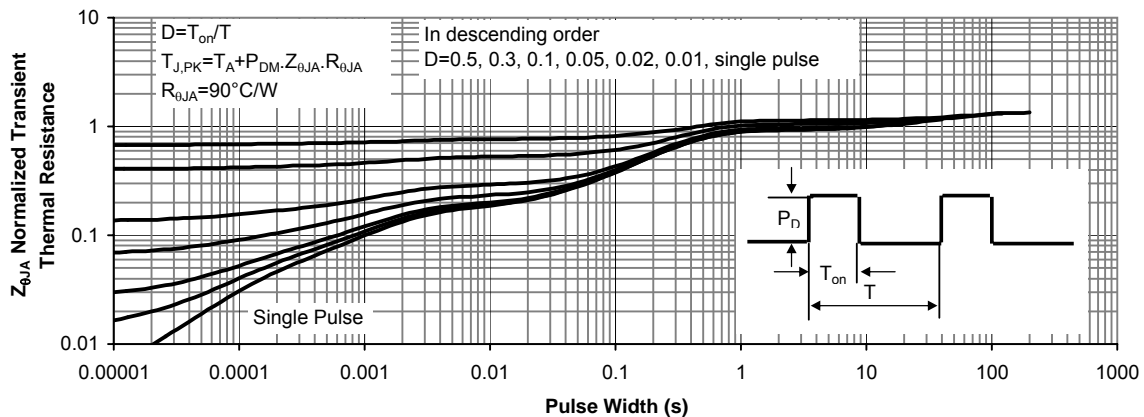


Figure 11: Normalized Maximum Transient Thermal Impedance