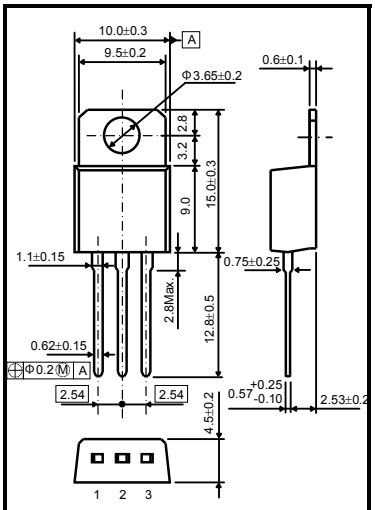
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (Ultra-High-Speed U-MOSⅢ)

TK55D10J1

Switching Regulator Applications

- High-Speed switching
- Low gate charge: Q_g = 110 nC (typ.)
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 8.4 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 110S
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 100 V)
- Enhancement mode: V_{th} = 1.1 to 2.3 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



1: Gate
2: Drain (Heat Sink)
3: Source

JEDEC	-
JEITA	-
TOSHIBA	2-10V1A

Weight: 1.35 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

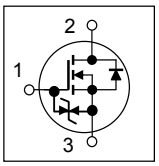
Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	100	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	100	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	55	A
	Pulse (Note 1)	I_{DP}	210	
Drain power dissipation (Tc = 25°C)		P_D	140	W
Single pulse avalanche energy (Note 2)		E_{AS}	382	mJ
Avalanche current		I_{AR}	55	A
Repetitive avalanche energy (Note 3)		E_{AR}	9.4	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 50	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	0.89	°C/W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	83.3	°C/W

Internal Connection



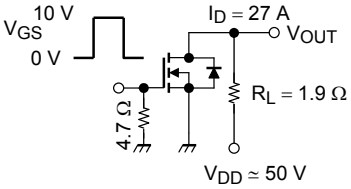
Note 1: Ensure that the channel and lead temperatures do not exceed 150°C.

Note 2: V_{DD} = 25 V, T_{ch} = 25°C, L = 200 μH, I_{AR} = 55 A , R_G = 1Ω

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.

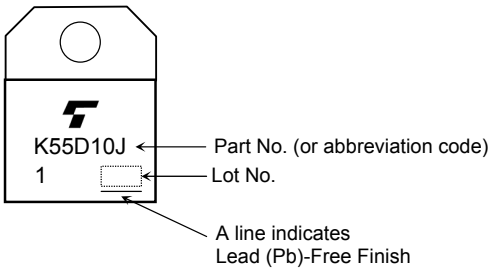
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = -20 V	55	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.1	—	2.3	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 27A	—	9.0	12.0	mΩ
			V_{GS} = 10 V, I_D = 27A	—	8.4	10.5	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 27 A	55	110	—	S
Input capacitance		C_{iss}	V_{DS} = 10V, V_{GS} = 0 V, f = 1 MHz	—	5700	—	pF
Reverse transfer capacitance		C_{rss}		—	390	—	
Output capacitance		C_{oss}		—	1000	—	
Switching time	Rise time	t_r		—	7	—	ns
	Turn-ON time	t_{on}		—	30	—	
	Fall time	t_f		—	20	—	
	Turn-OFF time	t_{off}	Duty ≦ 1%, t_w = 10 μs	—	130	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ 80 V, V_{GS} = 5 V, I_D = 55A	—	63	—	nC
			V_{DD} ≃ 80 V, V_{GS} = 10 V, I_D = 55A	—	110	—	
Gate-source charge 1		Q_{gs1}	V_{DD} ≃ 80 V, V_{GS} = 10 V, I_D = 55A	—	17	—	
Gate-drain (“miller”) charge		Q_{gd}		—	32	—	
Gate switch charge		Q_{sw}		—	38	—	

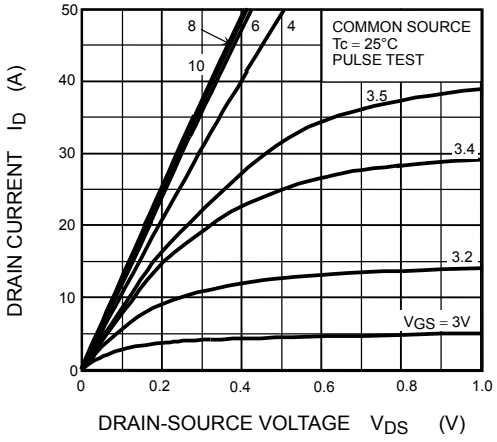
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	55	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	220	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 55 A, V_{GS} = 0 V	—	−0.9	−1.2	V
Reverse recovery time	t_{rr}	I_{DR} = 55 A, V_{GS} = 0 V,	—	67	—	ns
Reverse recovery charge	Q_{rr}	dI_{DR}/dt = 50 A/μs	—	84	—	nC

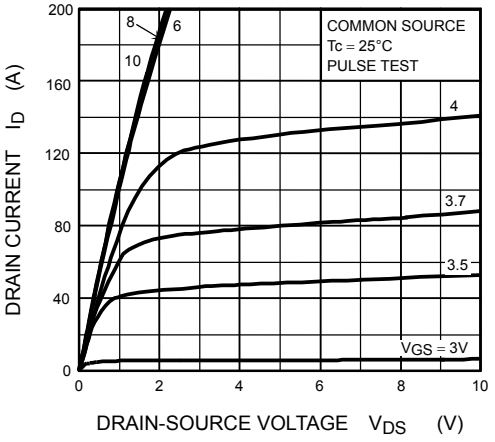
Marking



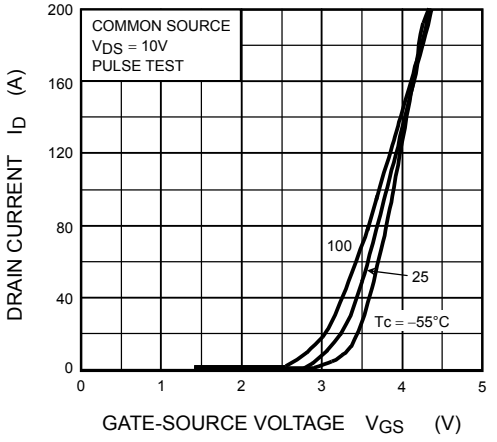
$I_D - V_{DS}$



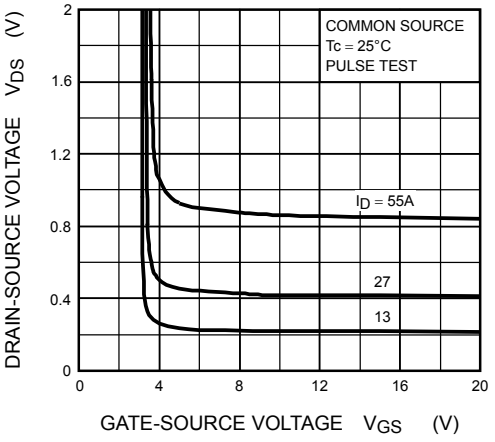
$I_D - V_{DS}$



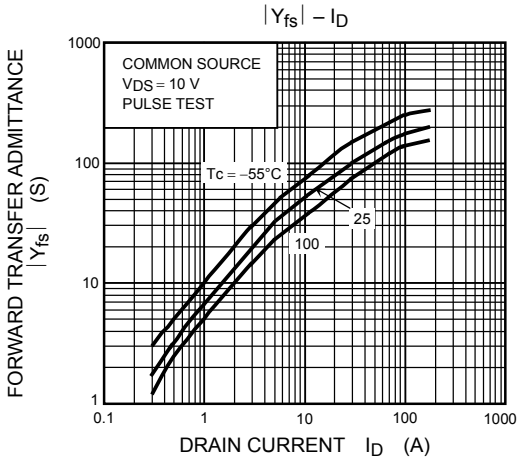
$I_D - V_{GS}$



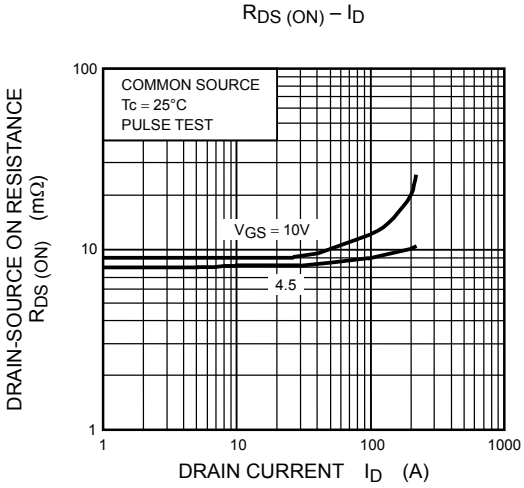
$V_{DS} - V_{GS}$



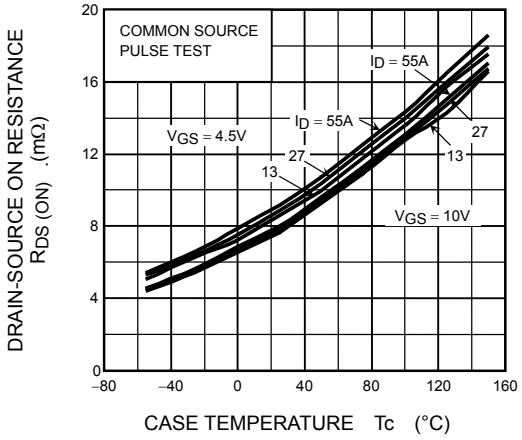
$|Y_{fs}| - I_D$



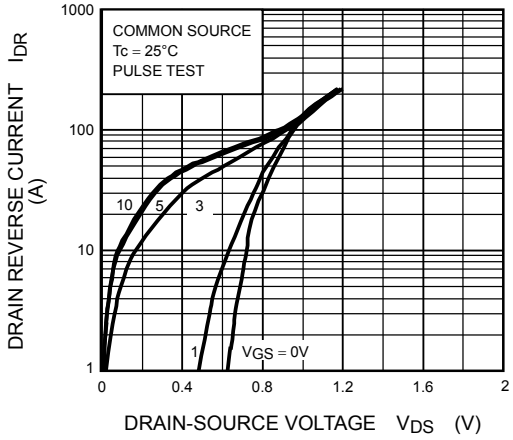
$R_{DS\ (ON)} - I_D$



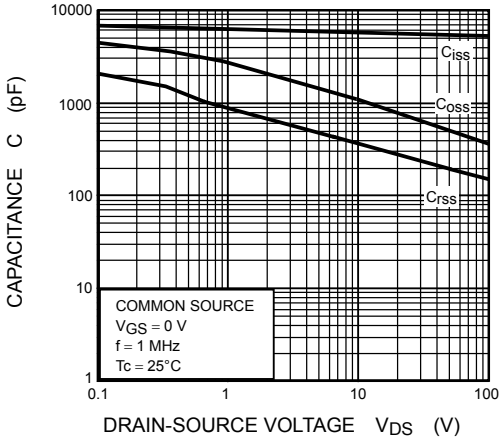
$R_{DS\ (ON)}$ – Tc



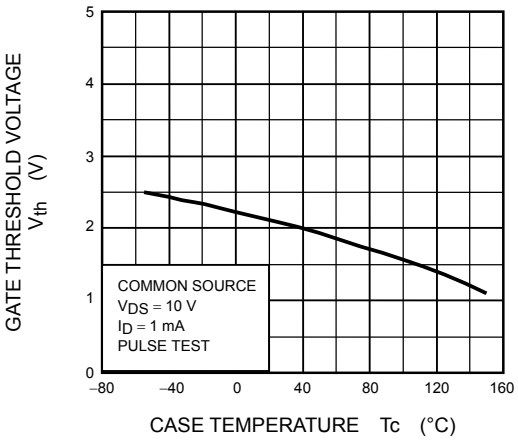
I_{DR} – V_{DS}



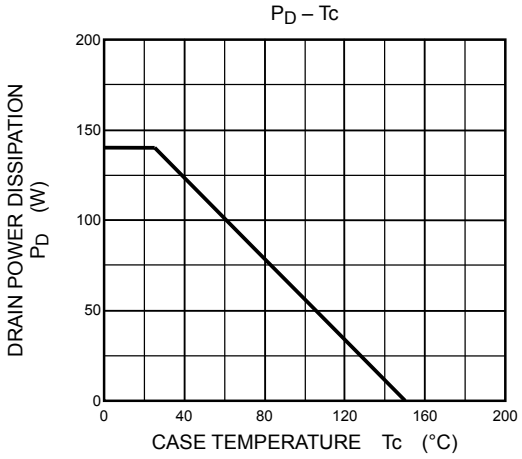
CAPACITANCE – V_{DS}



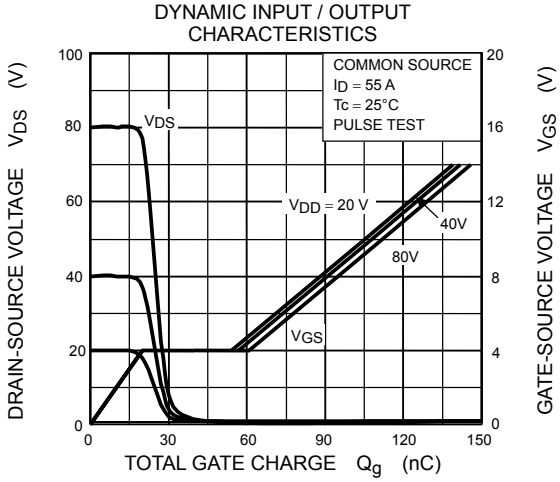
V_{th} – Tc



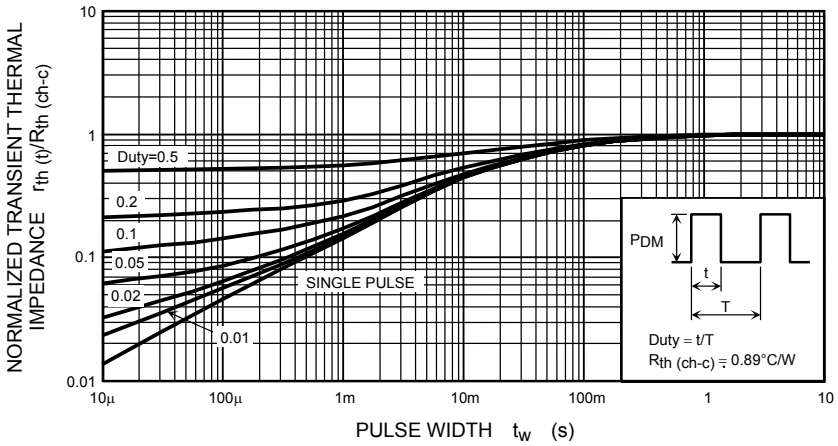
P_D – Tc



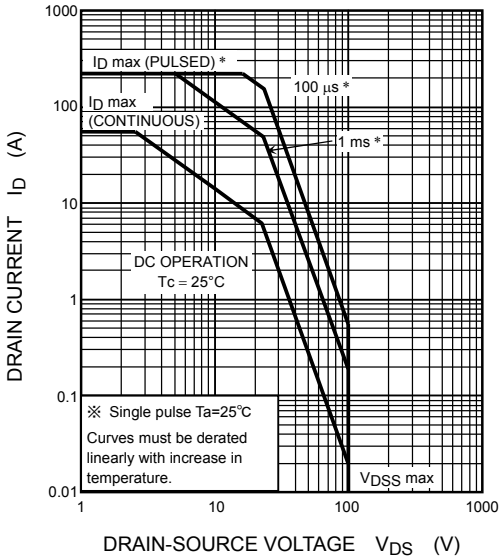
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



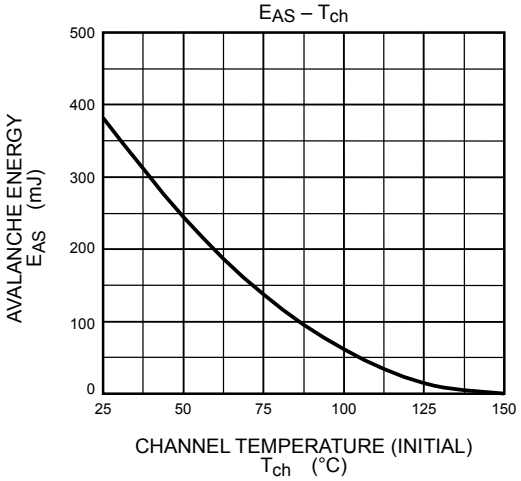
$r_{th}/R_{th\ (ch\text{-}c)} - t_w$

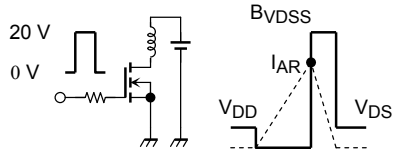


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





TEST CIRCUIT WAVE FORM

$R_G = 1\Omega$
$V_{DD} = 25$ V, L = 200μH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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20070701-EN

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