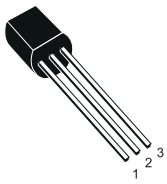
STQ1NC60R

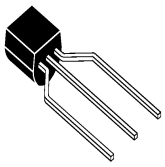
N-CHANNEL 600V - 12Ω - 0.3A TO-92
PowerMESH™II Power MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STQ1NC60R	600 V	< 15 Ω	0.3 A

- TYPICAL $R_{DS}(on)$ = 12 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED



TO-92
BULK



TO-92
(AMMOPACK)

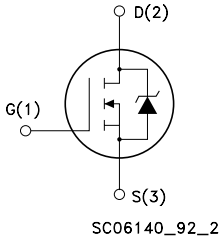
DESCRIPTION

Using the latest high voltage MESH OVERLAY™II process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- LOW SWITCH MODE POWER SUPPLIES (SMPS)
- BATTERY CHARGER

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STQ1NC60R	Q1NC60R	TO-92	BULK
STQ1NC60R-AP	Q1NC60R	TO-92	AMMOPACK

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	600	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	600	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at T_C = 25° C	0.3	A
I_D	Drain Current (continuous) at T_C = 100° C	0.19	A
I_{DM} (•)	Drain Current (pulsed)	1.2	A
P_{TOT}	Total Dissipation at T_C = 25° C	3.1	W
	Derating Factor	0.025	W/° C
dv/dt (1)	Peak Diode Recovery voltage slope	3	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-65 to 150 -65 to 150	℃ ℃

(•) Pulse width limited by safe operating area
(1) I_{SD} ≤0.3A, di/dt ≤100A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}.

THERMAL DATA

		TO-92	
Rthj-amb	Thermal Resistance Junction-ambient Max	120	°C/W
Rthj-lead	Thermal Resistance Junction-lead Max	40	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	260	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	0.3	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	60	mJ

ELECTRICAL CHARACTERISTICS (TCASE =25°C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 0.3 A		12	15	Ω

ELECTRICAL CHARACTERISTICS (TCASE =25°C UNLESS OTHERWISE SPECIFIED)
DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D = 0.3 A		0.87		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		108 18 2.5		pF pF pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 300 V, I_D = 0.5 A R_G = 4.7Ω V_{GS} = 10 V (Resistive Load see, Figure 3)		7.2 8		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 480V, I_D = 1 A, V_{GS} = 10V, R_G = 4.7Ω		7.3 3.4 2.5	10	nC nC nC

SWITCHING OFF

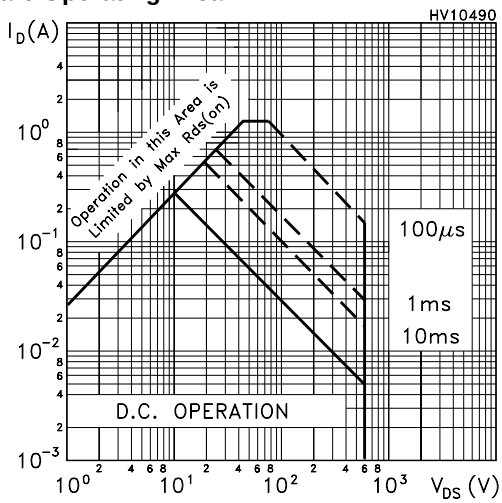
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 480V, I_D = 1 A, R_G = 4.7Ω, V_{GS} = 10V (Inductive Load see, Figure 5)		33 11 43		ns ns ns

SOURCE DRAIN DIODE

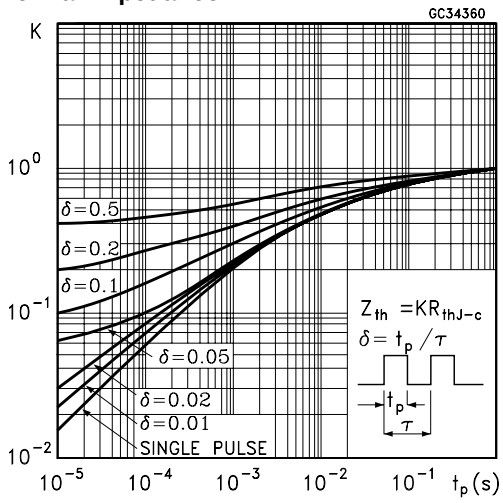
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				0.3 1.2	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 0.3 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 1 A, di/dt = 100A/µs V_{DD} = 25 V, T_j = 150°C (see test circuit, Figure 5)		450 720 3.2		ns µC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

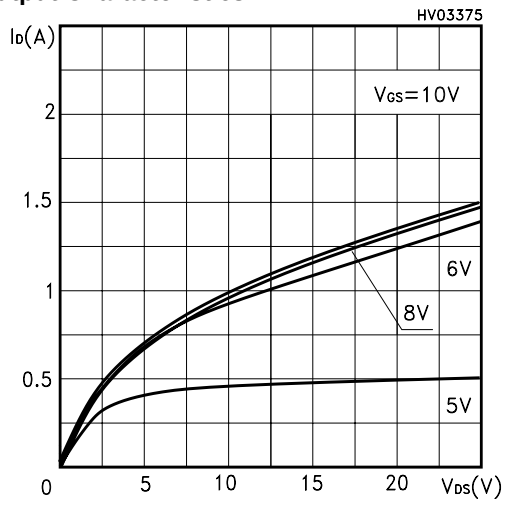
Safe Operating Area



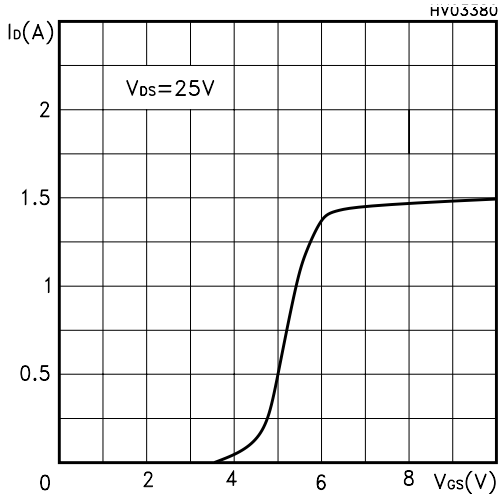
Thermal Impedance



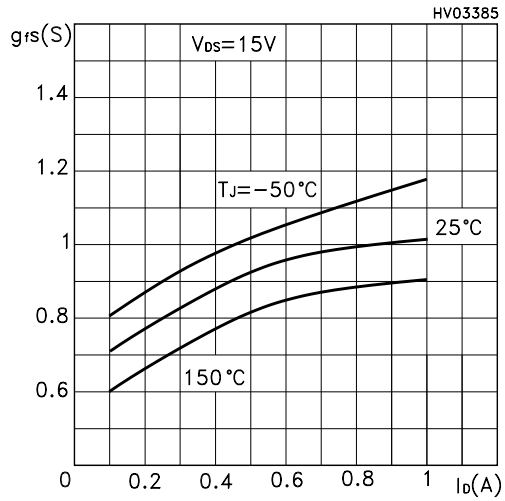
Output Characteristics



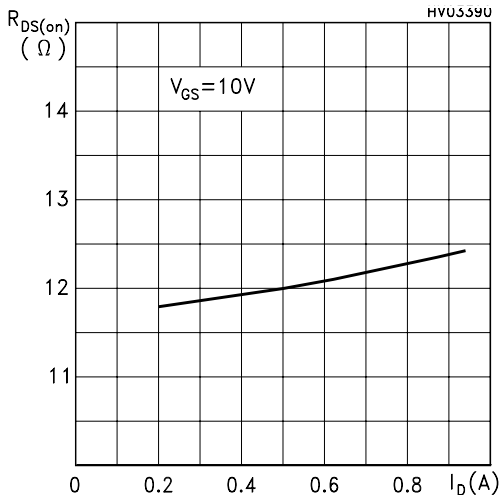
Transfer Characteristics



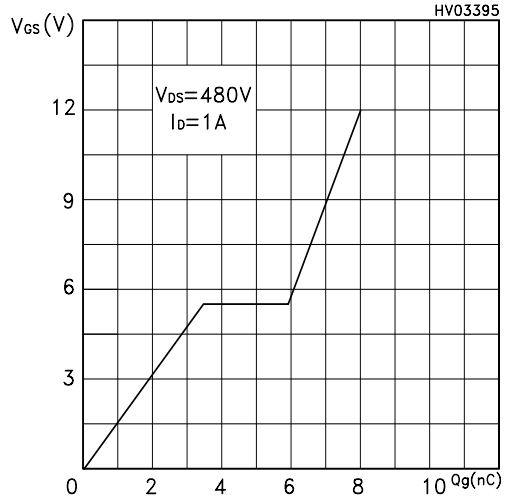
Tranconductance



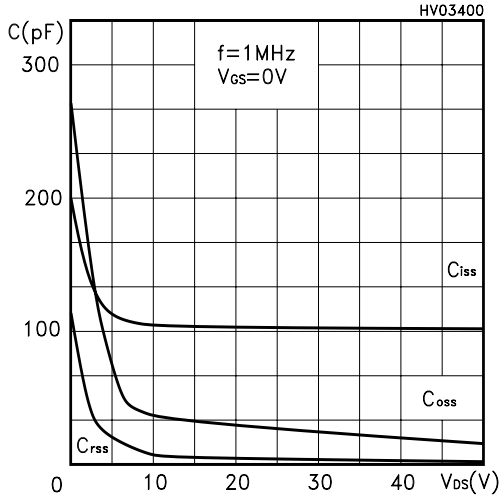
Static Drain-Source On Resistance



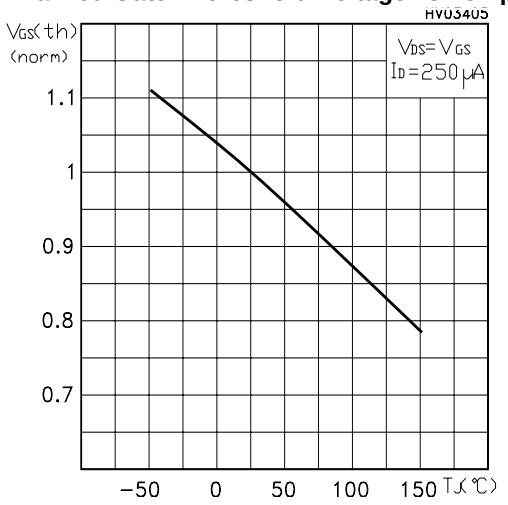
Gate Charge vs Gate-source Voltage



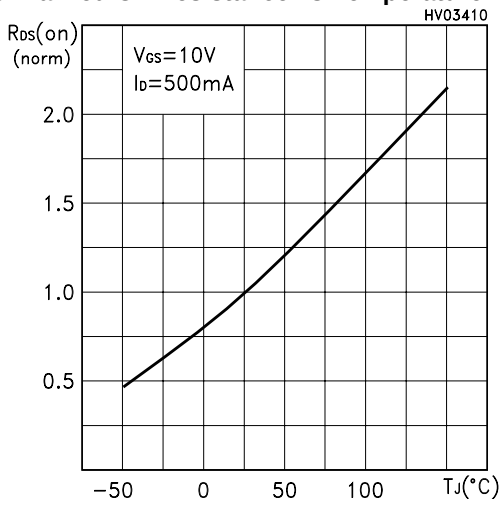
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

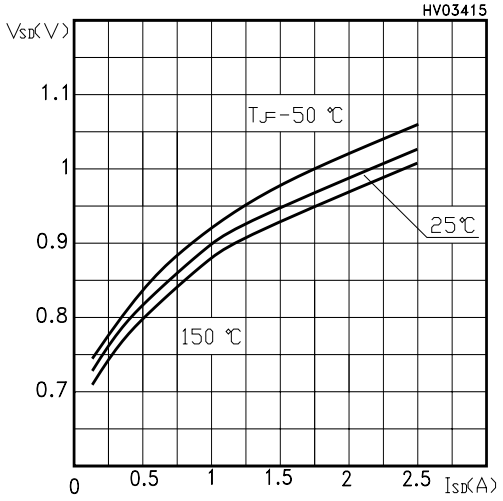


Fig. 1: Unclamped Inductive Load Test Circuit

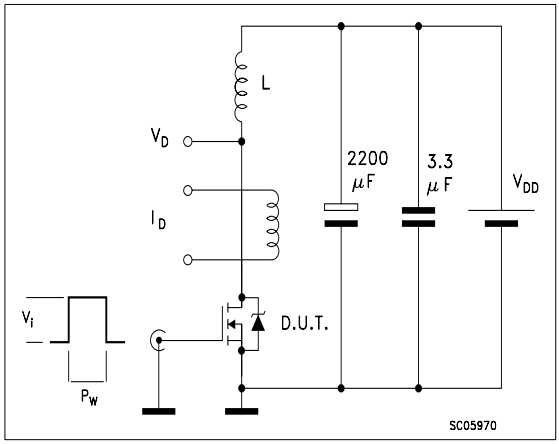


Fig. 2: Unclamped Inductive Waveform

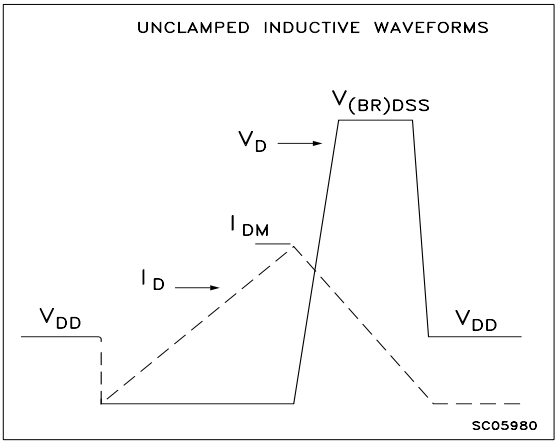


Fig. 3: Switching Times Test Circuit For Resistive Load

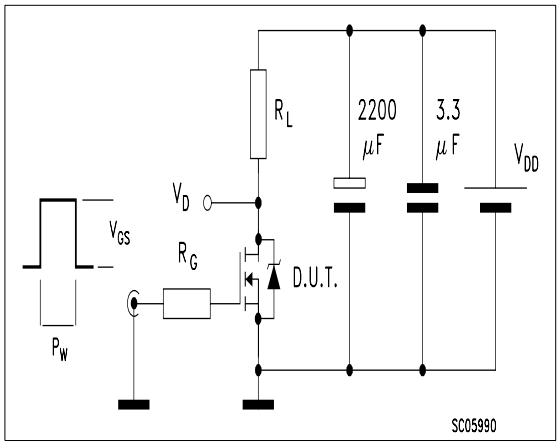


Fig. 4: Gate Charge test Circuit

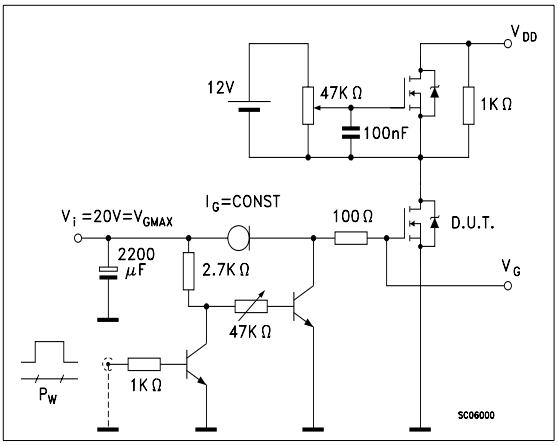
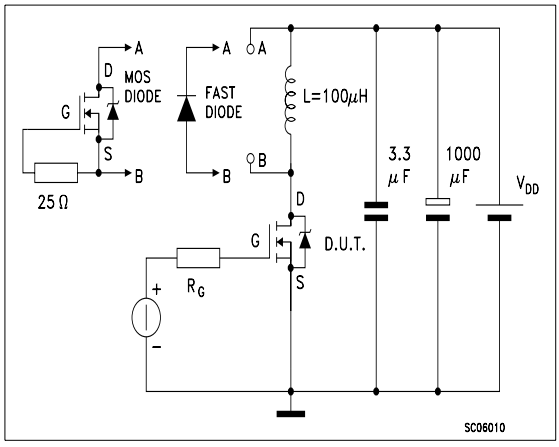
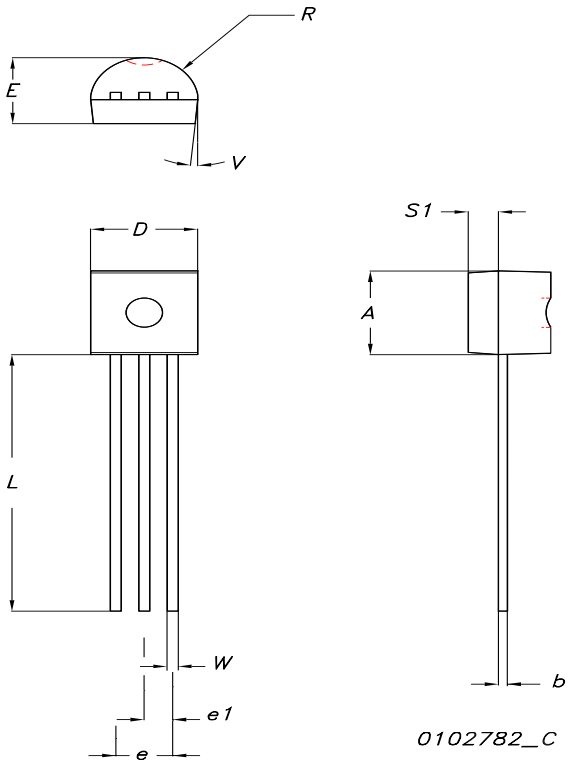


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



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DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A1			4.8			0.19
T			3.8			0.15
T1			1.6			0.06
T2			2.3			0.09
d			0.48			0.02
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
l1	3			0.11		
delta P	-1		1	-0.04		0.04