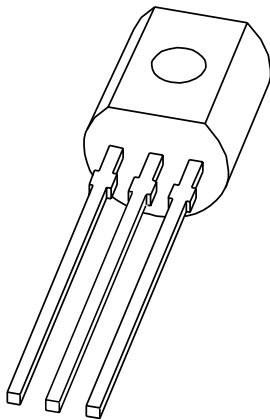


# DATA SHEET



## **BSN254; BSN254A** N-channel enhancement mode vertical D-MOS transistor

Product specification  
Supersedes data of 1997 Jun 23

2002 Feb 19

# N-channel enhancement mode vertical D-MOS transistor

## BSN254; BSN254A

### FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low  $R_{DSon}$ .

### APPLICATIONS

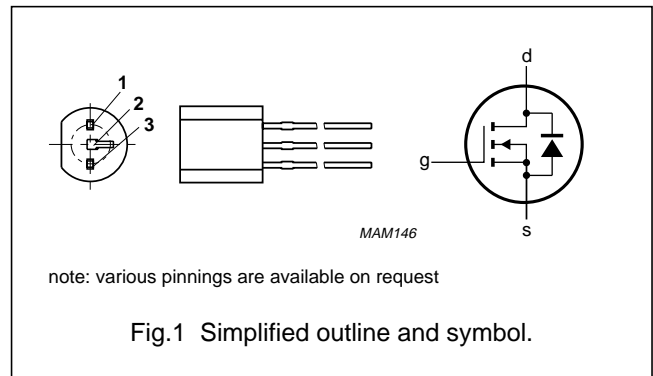
- Line current interruptor in telephone sets
- Relay, high-speed and line transformer drivers.

### DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT54 (TO-92) variant package.

### PINNING - SOT54 variant

PIN	DESCRIPTION	
	BSN254	BSN254A
1	gate	source
2	drain	gate
3	source	drain



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	250	V
$I_D$	drain current (DC)		–	310	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$	–	1	W
$R_{DSon}$	drain-source on-state resistance	$I_D = 300\text{ mA}; V_{GS} = 10\text{ V}$	2.8	5	$\Omega$
$V_{GSth}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}$	–	2	V

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	250	V
$V_{GSO}$	gate-source voltage (DC)	open drain	–	$\pm 20$	V
$I_D$	drain current (DC)		–	310	mA
$I_{DM}$	peak drain current		–	1.25	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}; \text{note 1}$	–	1	W
$T_{stg}$	storage temperature		–55	+150	$^\circ\text{C}$
$T_j$	junction temperature		–	150	$^\circ\text{C}$

### Note

1. Device mounted on a printed-circuit board; maximum lead length 4 mm; mounting pad for drain lead minimum  $10 \times 10\text{ mm}$ .

## N-channel enhancement mode vertical D-MOS transistor

BSN254; BSN254A

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient; note 1	125	K/W

#### Note

1. Device mounted on a printed-circuit board; maximum lead length 4 mm; mounting pad for drain lead minimum  $10 \times 10$  mm.

### CHARACTERISTICS

$T_j = 25$  °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}; V_{GS} = 0$	250	–	–	V
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	–	–	$\pm 100$	nA
$V_{GSth}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$	0.8	–	2	V
$R_{DSon}$	drain-source on-state resistance	$I_D = 20\ \text{mA}; V_{GS} = 2.4\ \text{V}$	–	–	7.5	$\Omega$
		$I_D = 300\ \text{mA}; V_{GS} = 10\ \text{V}$	–	2.8	5	$\Omega$
$I_{DSS}$	drain-source leakage current	$V_{DS} = 200\ \text{V}; V_{GS} = 0$	–	–	1	$\mu\text{A}$
$ Y_{fs} $	transfer admittance	$I_D = 300\ \text{mA}; V_{DS} = 25\ \text{V}$	200	600	–	mS
$C_{iss}$	input capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	100	120	pF
$C_{oss}$	output capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	21	30	pF
$C_{rss}$	feedback capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	10	15	pF
<b>Switching times</b> (see Figs 2 and 3)						
$t_{on}$	turn-on time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V}; V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	6	10	ns
$t_{off}$	turn-off time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V}; V_{GS} = 10\ \text{to}\ 0\ \text{V}$	–	47	60	ns

N-channel enhancement mode vertical D-MOS transistor

BSN254; BSN254A

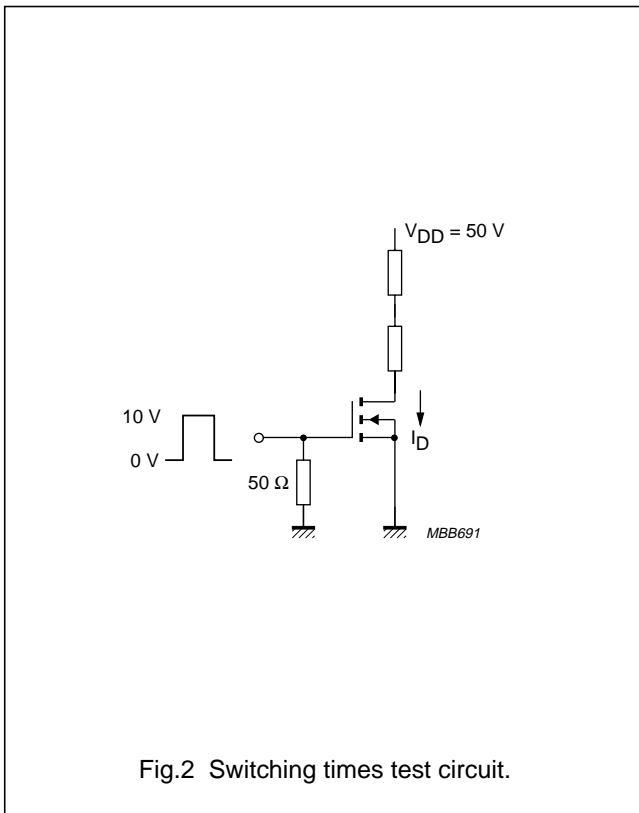


Fig.2 Switching times test circuit.

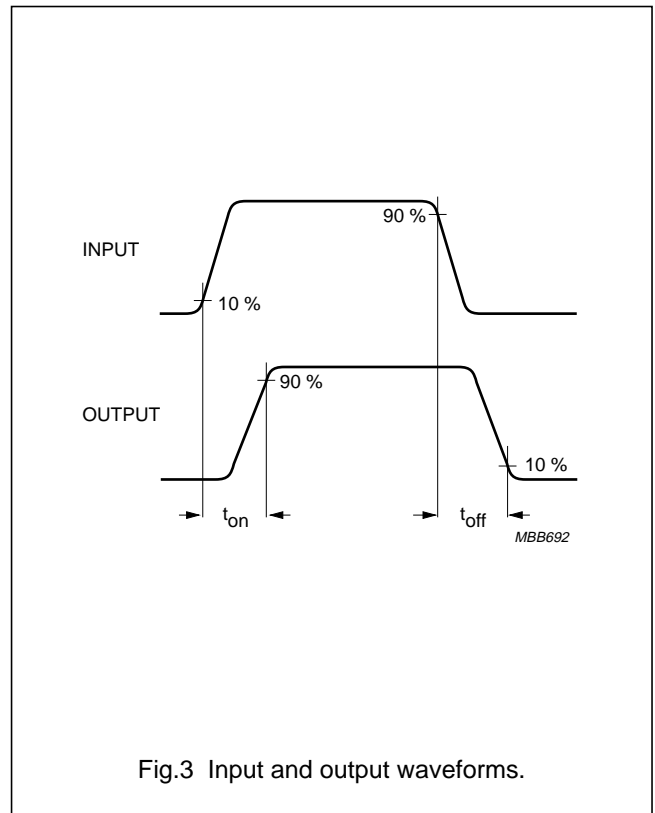


Fig.3 Input and output waveforms.

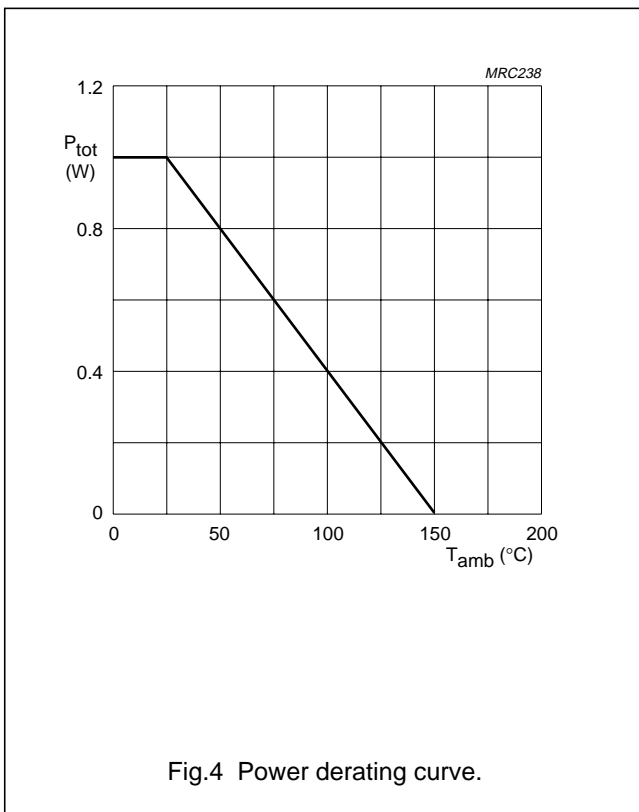


Fig.4 Power derating curve.

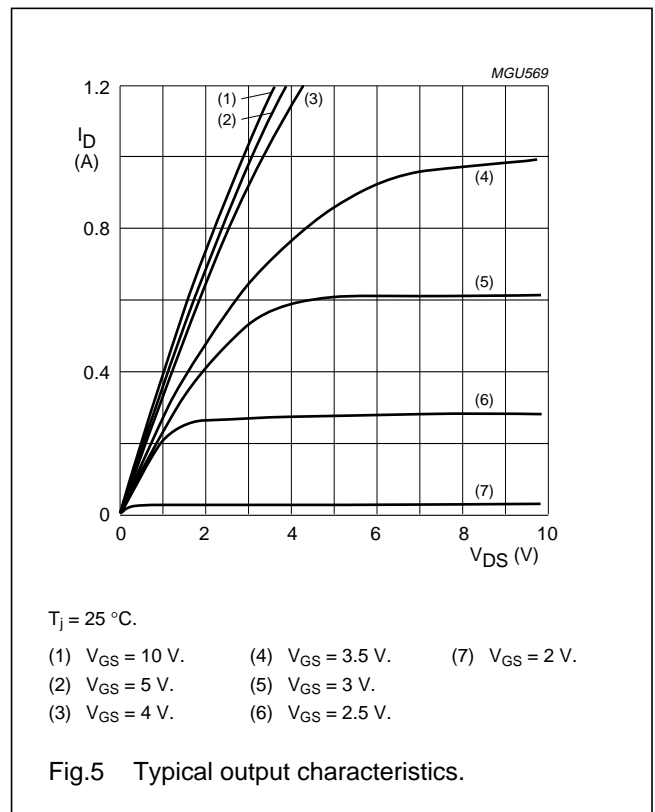
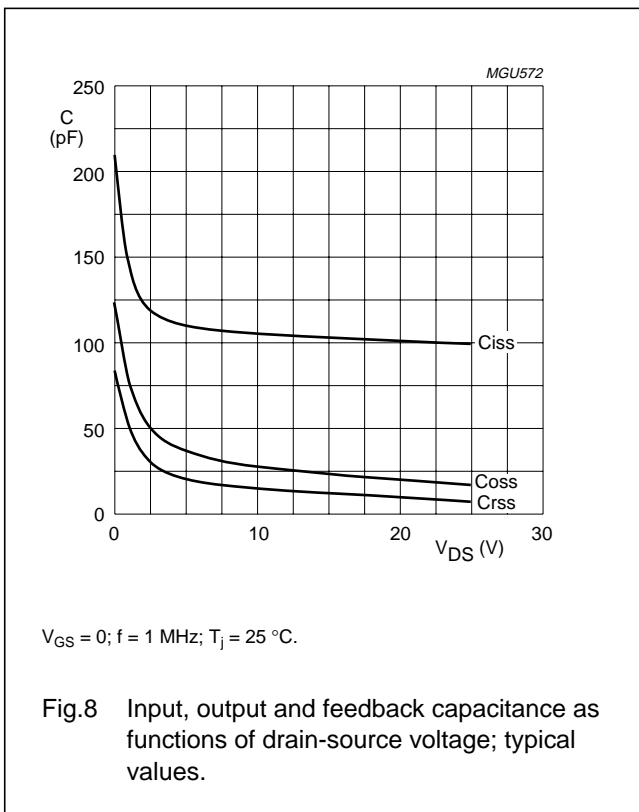
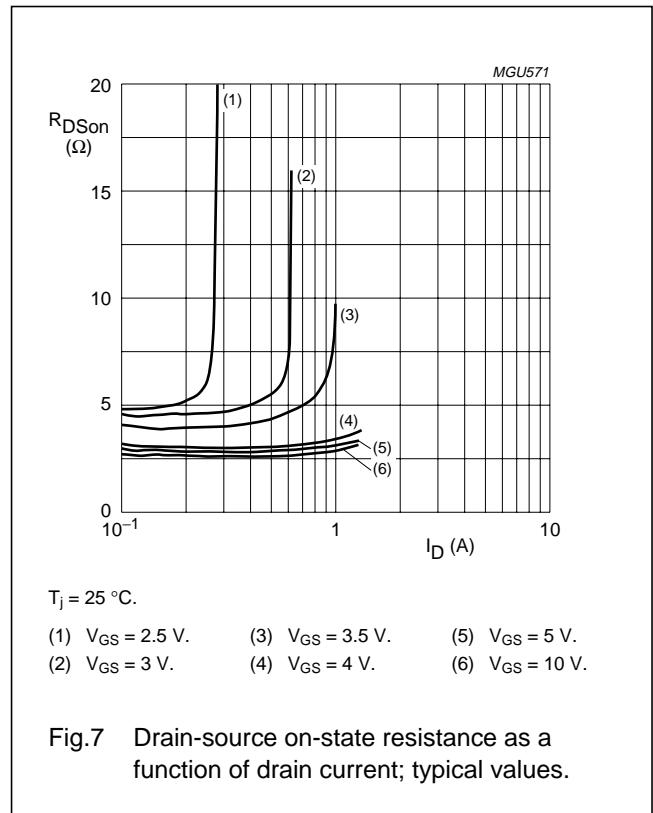
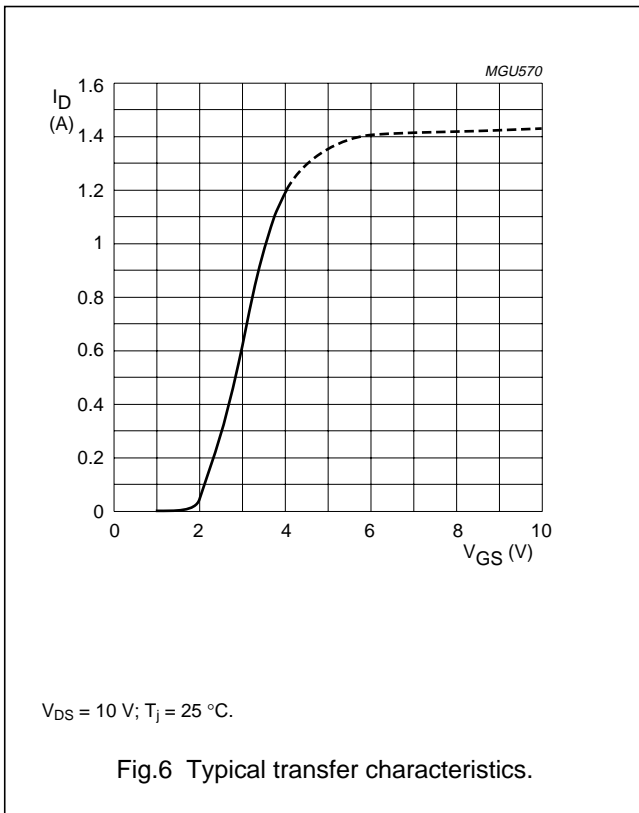


Fig.5 Typical output characteristics.

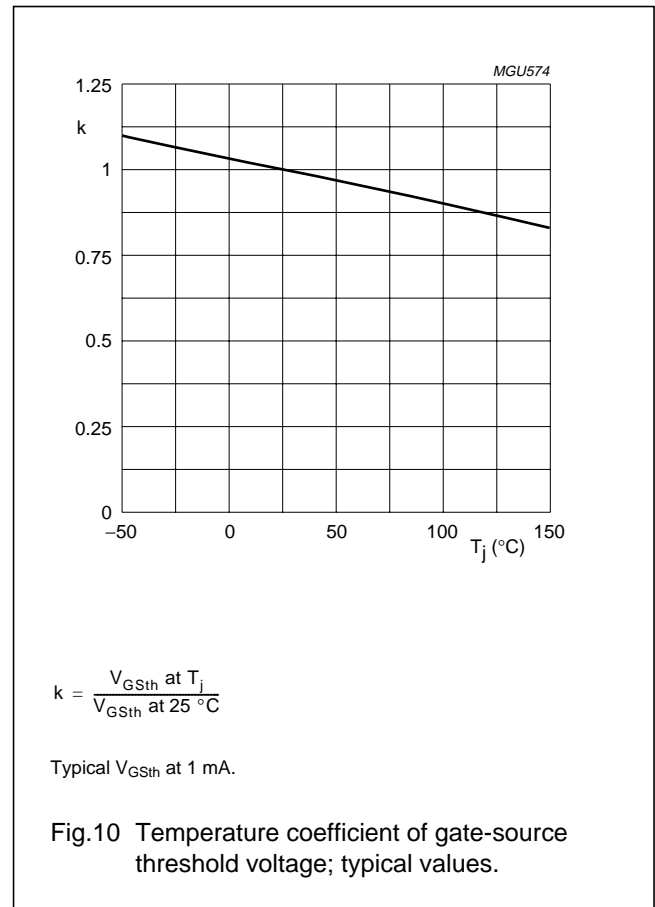
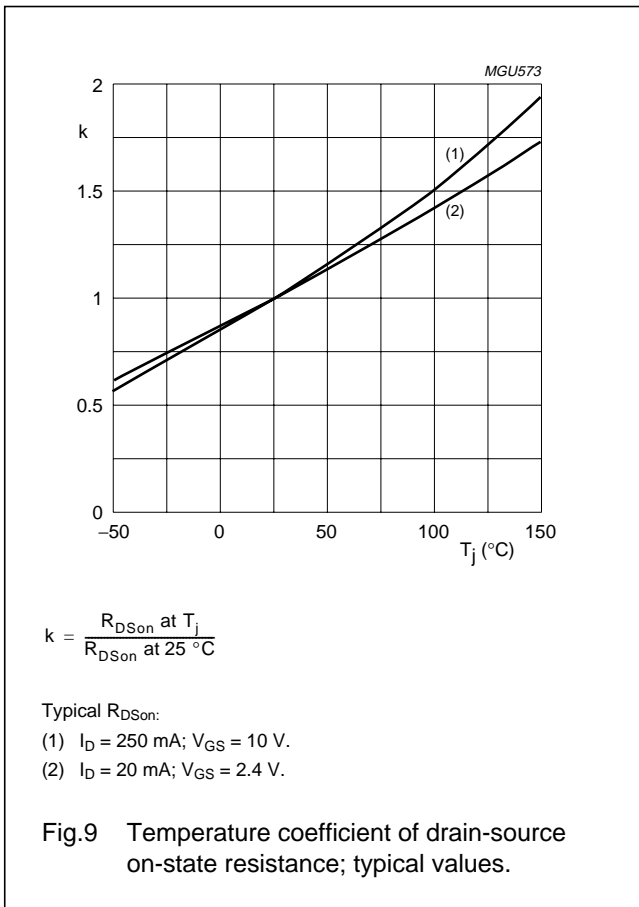
N-channel enhancement mode vertical D-MOS transistor

BSN254; BSN254A



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BSN254; BSN254A



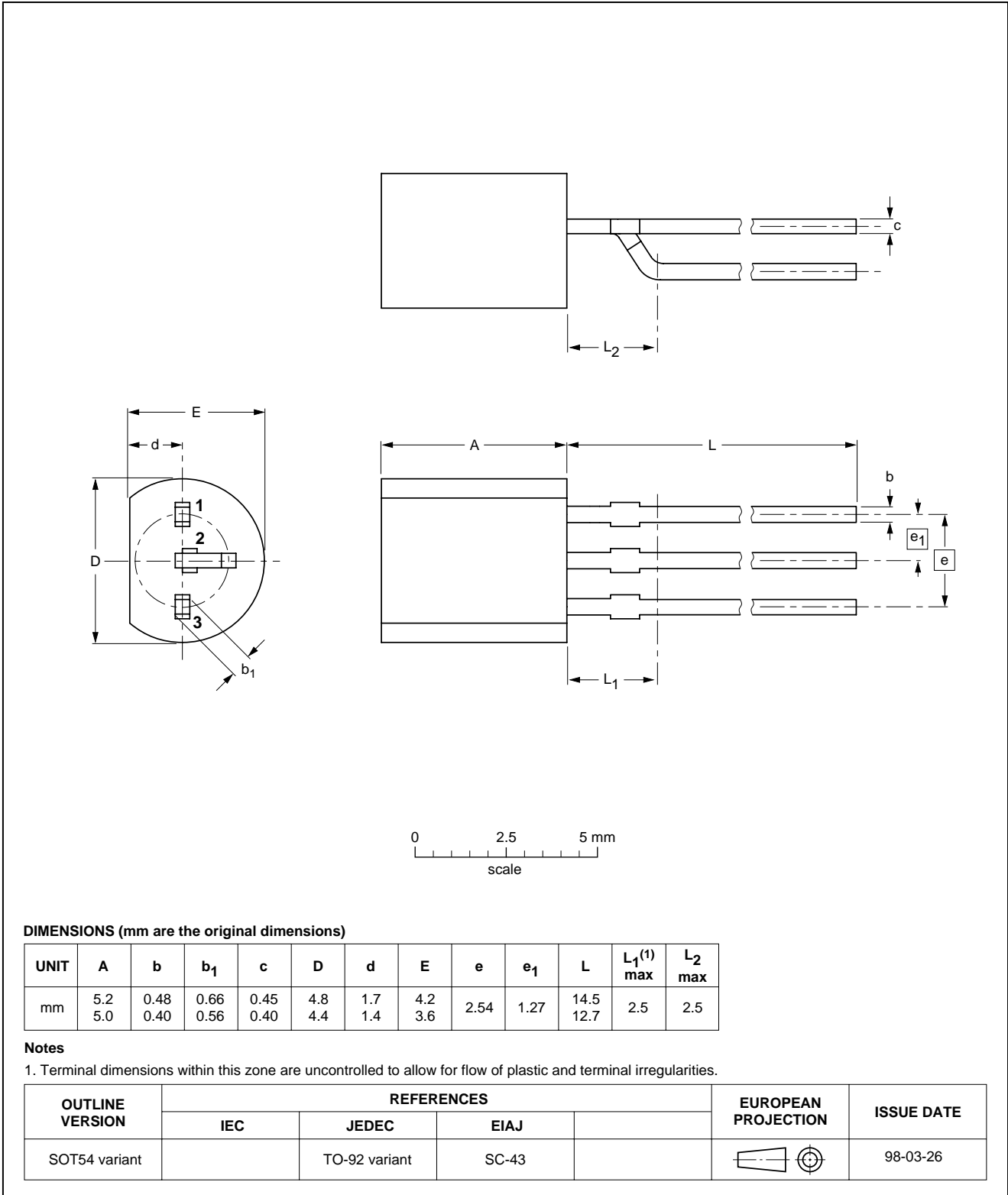
N-channel enhancement mode  
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BSN254; BSN254A

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



## N-channel enhancement mode vertical D-MOS transistor

BSN254; BSN254A

### DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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N-channel enhancement mode  
vertical D-MOS transistor

BSN254; BSN254A

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**NOTES**

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N-channel enhancement mode  
vertical D-MOS transistor

BSN254; BSN254A

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N-channel enhancement mode  
vertical D-MOS transistor

BSN254; BSN254A

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**NOTES**

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