

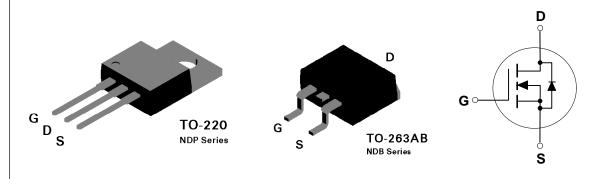
## NDP6030L / NDB6030L N-Channel Logic Level Enhancement Mode Field Effect Transistor

### **General Description**

These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

### **Features**

- 52 A, 30 V.  $R_{DS(ON)} = 0.0135 \Omega$  @  $V_{GS} = 10 V$  $R_{DS(ON)} = 0.020 \Omega$  @  $V_{GS} = 4.5 V$ .
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- 175°C maximum junction temperature rating.



Absolute Maximum Ratings	T = 25°C unless otherwise noted

Symbol	Parameter	NDP6030L	NDB6030L	Units		
V <sub>DSS</sub>	Drain-Source Voltage	30				
$V_{GSS}$	Gate-Source Voltage - Continuous	± 16		V		
I <sub>D</sub>	Drain Current - Continuous	52		А		
	- Pulsed	156				
$P_{D}$	Total Power Dissipation @ T <sub>C</sub> = 25°C	75		W		
	Derate above 25°C	0.5				
$T_J$ , $T_{STG}$	Operating and Storage Temperature Range	-65 to 175				
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C		
THERMA	L CHARACTERISTICS					
R <sub>øJC</sub>	Thermal Resistance, Junction-to-Case	2		°C/W		
R <sub>øJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5		°C/W		

© 1998 Fairchild Semiconductor Corporation

Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE AVALANCHE RATINGS (Note 1)						
W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energ	gy $V_{DD} = 15 \text{ V}, I_{D} = 52 \text{ A}$				100	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Current	·				52	Α
OFF CHA	ARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, \ V_{GS} = 0 \text{ V}$				10	μA
			$T_{J} = 125^{\circ}C$			1	mA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	$V_{GS} = 16 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	$V_{GS} = -16 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA	
ON CHAP	RACTERISTICS (Note 1)	-				•	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1	1.6	3	V
			T <sub>J</sub> = 125°C	0.7	1	2.2	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_{D} = 26 \text{ A}$	<u> </u>		0.011	0.0135	Ω
			T <sub>J</sub> = 125°C		0.017	0.024	
		$V_{GS} = 4.5 \text{ V}, I_{D} = 21 \text{ A}$			0.018	0.02	
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$		60			Α
		$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}$	15				
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 26 \text{ A}$		32		S	
DYNAMIC	CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 15 \text{ V}, \ V_{GS} = 0 \text{ V},$			1350		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz			800		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			300		pF	

Symbol	Parameter	Conditions		Min	Тур	Max	Units
SWITCHI	ING CHARACTERISTICS (Note 1)	•					
t <sub>D(on)</sub>	Turn - On Delay Time	$V_{DD} = 15 \text{ V}, I_{D} = 52 \text{ A},$			8	16	nS
ţ,	Turn - On Rise Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 24 $\Omega$			130	250	nS
t <sub>D(off)</sub>	Turn - Off Delay Time			45	90	nS	
ţ,	Turn - Off Fall Time				108	200	nS
$\overline{Q_g}$	Total Gate Charge	V <sub>DS</sub> = 10 V		44	60	nC	
$Q_{gs}$	Gate-Source Charge	$I_D = 52 \text{ A}, V_{GS} = 10 \text{ V}$			6		nC
$Q_{gd}$	Gate-Drain Charge			14		nC	
DRAIN-S	OURCE DIODE CHARACTERISTICS						
I <sub>s</sub>	Maximum Continuos Drain-Source Di			52	Α		
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode			120	Α		
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 26 \text{ A} \text{ (Note 1)}$			0.93	1.3	V
			T <sub>1</sub> = 125°C		0.85	1.2	1

NDP6030L Rev.E

Note: 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

### **Typical Electrical Characteristics**

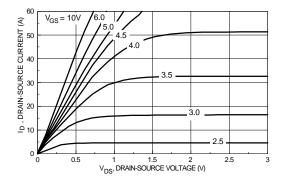


Figure 1. On-Region Characteristics.

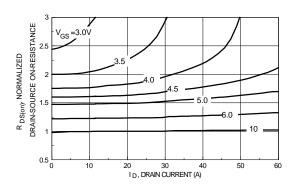


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

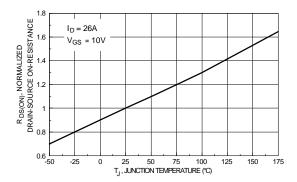


Figure 3. On-Resistance Variation with Temperature.

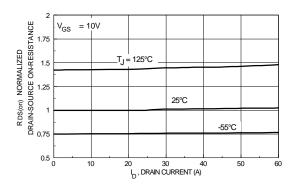


Figure 4. On-Resistance Variation with Drain Current and Temperature.

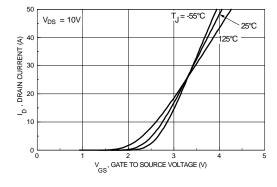


Figure 5. Transfer Characteristics.

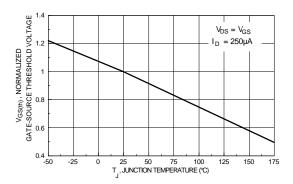


Figure 6. Gate Threshold Variation with Temperature.

### **Typical Electrical Characteristics (continued)**

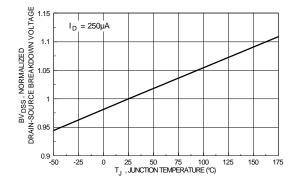


Figure 7. Breakdown Voltage Variation with Temperature.

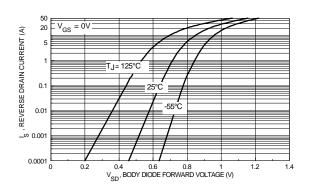


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.

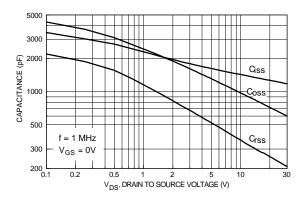


Figure 9. Capacitance Characteristics.

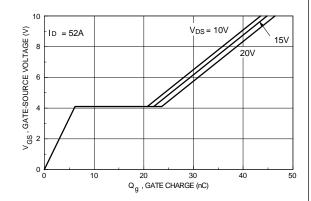


Figure 10. Gate Charge Characteristics.

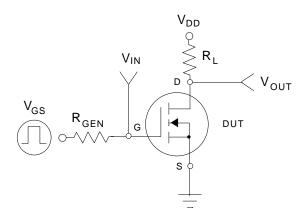


Figure 11. Switching Test Circuit.

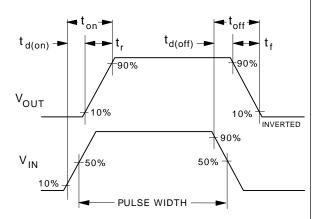
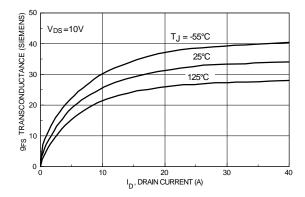


Figure 12. Switching Waveforms.

NDP6030L Rev.E

### **Typical Electrical Characteristics (continued)**



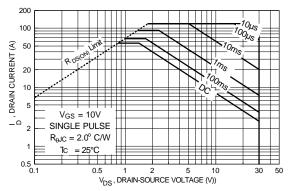


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. Maximum Safe Operating Area.

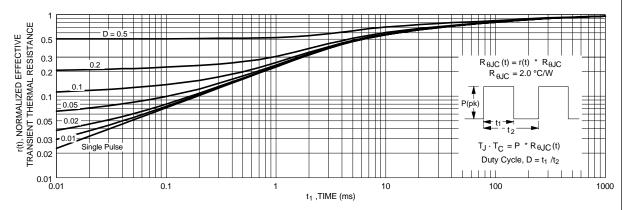
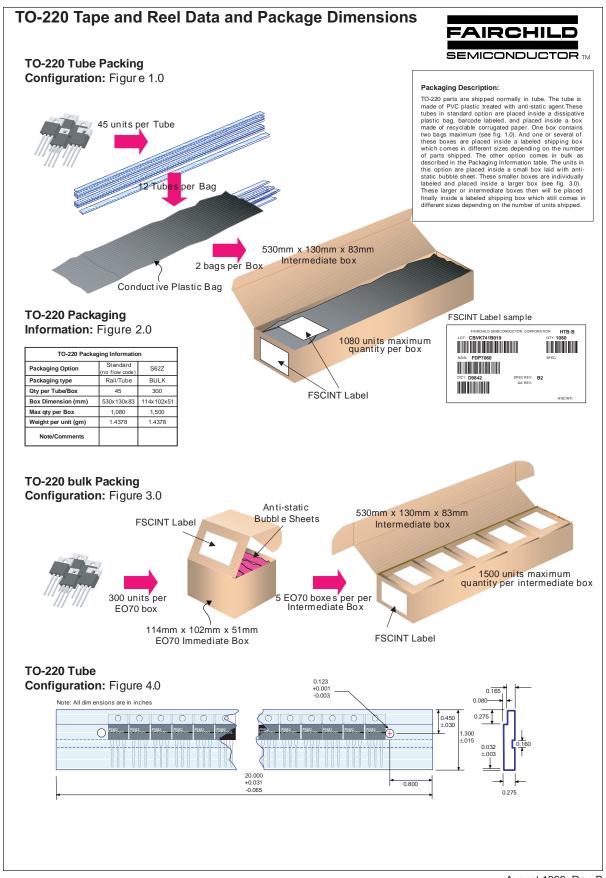


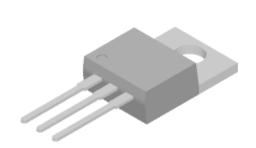
Figure 15. Transient Thermal Response Curve.

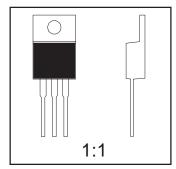
NDP6030L Rev.E



## TO-220 Tape and Reel Data and Package Dimensions, continued

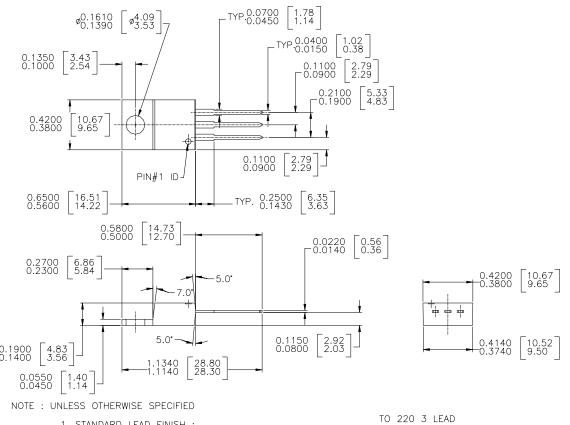
# TO-220 (FS PKG Code 37)





Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

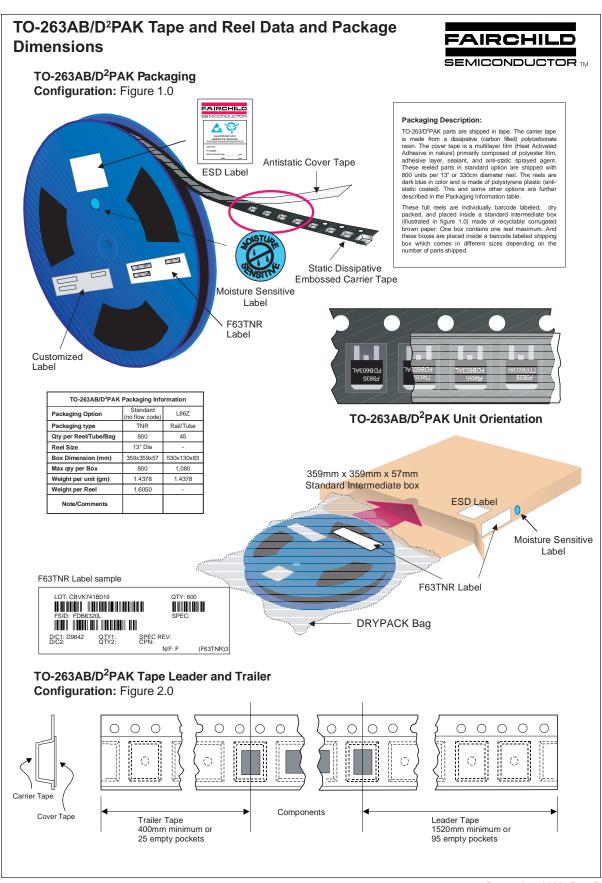
Part Weight per unit (gram): 1.4378



1. STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICRON MINIMUM
LEAD / TIN 15/85 ON OLIN 194 COPPER OR EQUIVALENT

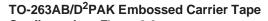
2. DIMENSION BASED ON JEDEC STANDARD TO-220 VARIATION AB, ISSUE J, DATED 3/24/87

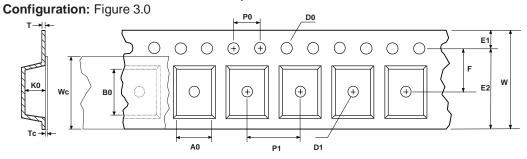
September 1998, Rev. A



September 1999, Rev. B

## TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued





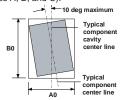
# **User Direction of Feed**

Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D²PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

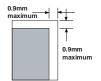
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)



Sketch B (Top View)
Component Rotation

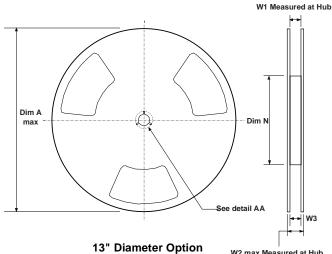


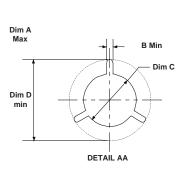
Sketch C (Top View)

Component lateral movement

# TO-263AB/D<sup>2</sup>PAK Reel Configuration:

Figure 4.0





W2 max Measured at Hub

Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
24mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.961 +0.078/-0.000 24.4 +2/0	1.197 30.4	0.941 - 0.1.079 23.9 - 27.4

# TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued TO-263AB/D<sup>2</sup>PAK (FS PKG Code 45) 1:1 Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters] Part Weight per unit (gram): 1.4378 **□** 1.32 8.84 8.53 1.02 **-** 5.08 -Ø0.25(M) B A(M) LAND PATTERN RECOMMENDATION 1.40 6.75 6.15 15.39 15.09 10.00 NOTES: UNLESS OTHERWISE SPECIFIED A) ALL DIMENSIONS ARE IN MILLIMETERS. B) STANDARD LEAD FINISH: 200 MICROINCHES / 5.08 MICROMETERS MIN. LEAD/TIN 15/85 ON OLIN 194 COPPER OR EQUIVALENT. C) MAXIMUM YERTICAL BURR ON HEATSINK NOT TO EXCEED 0.003 INCH / 0.05mm. D) NO PACKAGE CHIPS, CRACKS OR SURFACE IDENTIFICATION ALLOWED AFTER FORMING. E) REFERENCE JEDEC, TO—265, ISSUE C, VARIATION AB, DATED 2/92. 0.25 △ 0.10 B

August 1998, Rev. A

### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

FACT™ QFET™ FACT Quiet Series™ QS™

 $\begin{array}{lll} \mathsf{FAST}^{\circledast} & \mathsf{Quiet}\,\mathsf{Series}^{\mathsf{TM}} \\ \mathsf{FASTr}^{\mathsf{TM}} & \mathsf{SuperSOT}^{\mathsf{TM}}\text{-}3 \\ \mathsf{GTO}^{\mathsf{TM}} & \mathsf{SuperSOT}^{\mathsf{TM}}\text{-}6 \\ \mathsf{HiSeC}^{\mathsf{TM}} & \mathsf{SuperSOT}^{\mathsf{TM}}\text{-}8 \\ \end{array}$ 

### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### PRODUCT STATUS DEFINITIONS

### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. [