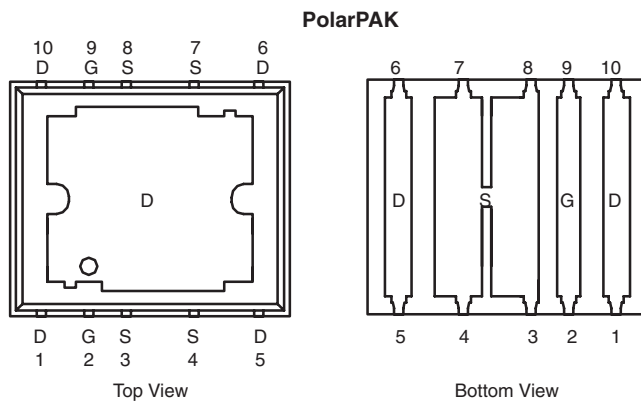


N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a		Q _g (Typ)
		Silicon Limit	Package Limit	
20	0.0034 at V _{GS} = 10 V	138	50	24 nC
	0.0055 at V _{GS} = 4.5 V	108	50	

[Package Drawing](http://www.vishay.com/doc?73398)
<http://www.vishay.com/doc?73398>



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE822DF-T1-E3 (Lead (Pb)-free)

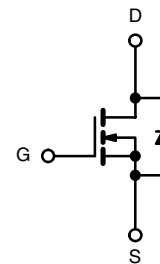
FEATURES

- TrenchFET[®] Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK[®] Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested



APPLICATIONS

- VRM
- DC-DC Conversion
- Synchronous Rectification



N-Channel MOSFET

[For Related Documents](http://www.vishay.com/ppg?74451)
<http://www.vishay.com/ppg?74451>

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	138 (Silicon Limit)	A
		50 ^a (Package Limit)	
		50 ^a	
		31 ^{b, c}	
Pulsed Drain Current	I _{DM}	80	A
		24.8 ^{b, c}	
Continuous Source-Drain Diode Current	I _S	50 ^a	A
		4.3 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	30	mJ
Avalanche Energy	E _{AS}	45	
Maximum Power Dissipation	P _D	104	W
		66	
		5.2 ^{b, c}	
		3.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

Notes:

- Package limited is 50 A.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 sec.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ sec	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top) ^a	Steady State	R_{thJC} (Drain)	1	1.2	
Maximum Junction-to-Case (Source) ^{a, c}		R_{thJC} (Source)	2.8	3.4	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
b. Maximum under Steady State conditions is 68 °C/W.
c. Measured at source pin (on the side of the package).

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

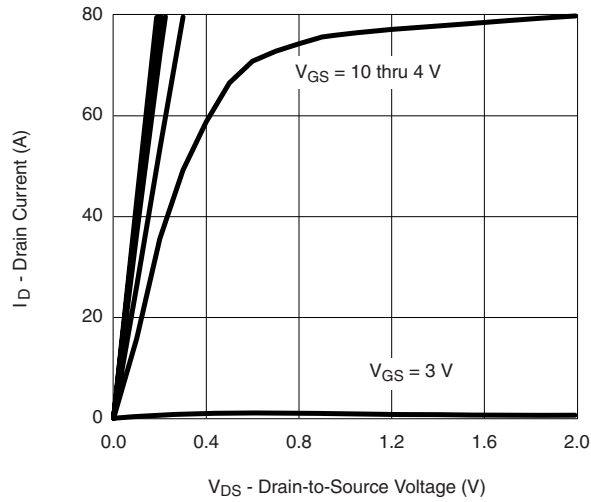
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ μ A		24.1		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-7.1			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	1.5	2.3	3.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	μ A
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	25			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 18.3$ A		0.0028	0.0034	Ω
		$V_{GS} = 4.5$ V, $I_D = 14.5$ A		0.0045	0.0055	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15$ V, $I_D = 18.3$ A		90		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10$ V, $V_{GS} = 0$ V, $f = 1$ MHz		4200		pF
Output Capacitance	C_{oss}		1000			
Reverse Transfer Capacitance	C_{riss}		320			
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 10$ V, $I_D = 20$ A		52	78	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A		24	36	
Gate-Drain Charge	Q_{gd}			13		
Gate Resistance	R_g	$f = 1$ MHz		1.0	1.5	Ω
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 1$ Ω $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω		50	75	ns
Rise Time	t_r		220	330		
Turn-Off Delay Time	$t_{d(off)}$		35	55		
Fall Time	t_f		20	30		
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 20$ V, $R_L = 1$ Ω $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω		15	25	
Rise Time	t_r		25	40		
Turn-Off Delay Time	$t_{d(off)}$		35	55		
Fall Time	t_f		10	15		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C			50	A
Pulse Diode Forward Current ^a	I_{SM}				80	
Body Diode Voltage	V_{SD}	$I_S = 10$ A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10$ A, $di/dt = 100$ A/ μ s, $T_J = 25$ °C		40	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			36	60	nC
Reverse Recovery Fall Time	t_a			19		ns
Reverse Recovery Rise Time	t_b			21		

Notes:

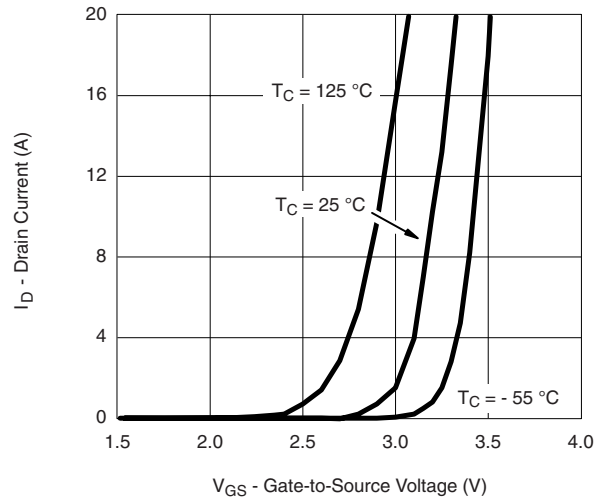
- a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

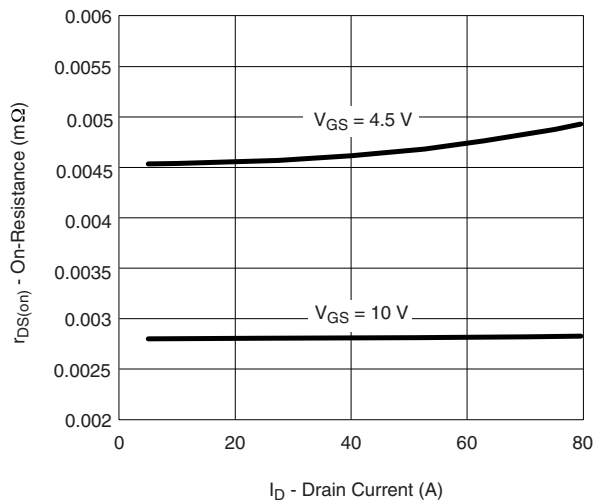
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



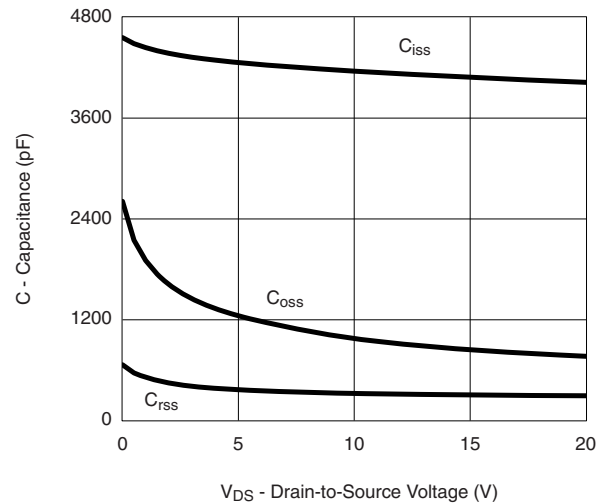
Output Characteristics



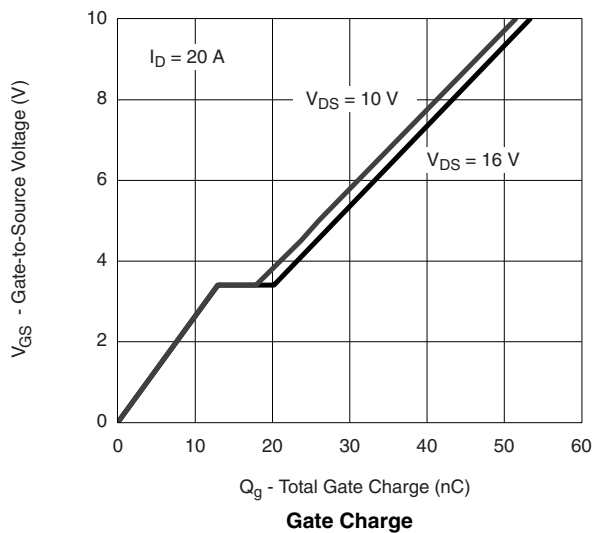
Transfer Characteristics



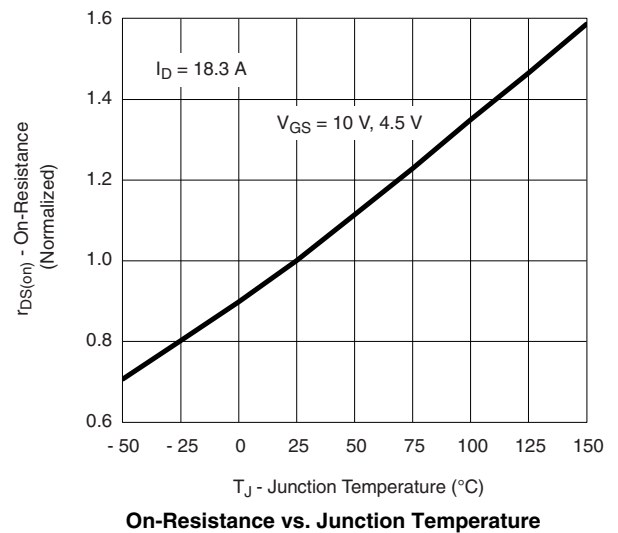
On-Resistance vs. Drain Current



Capacitance



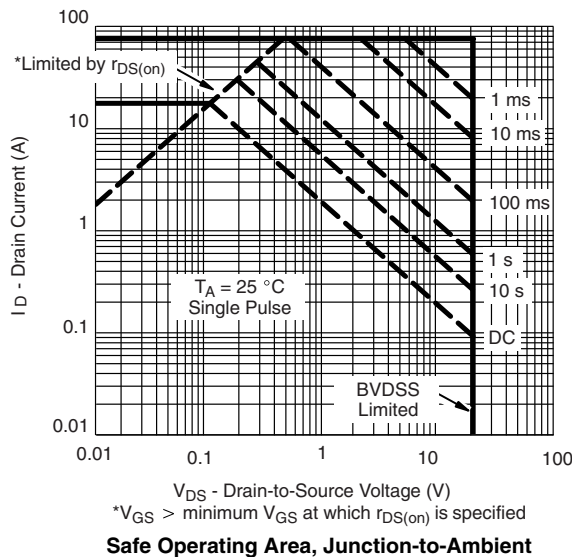
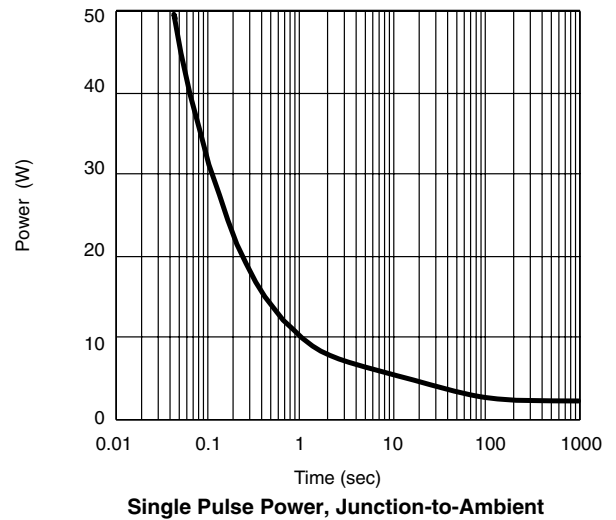
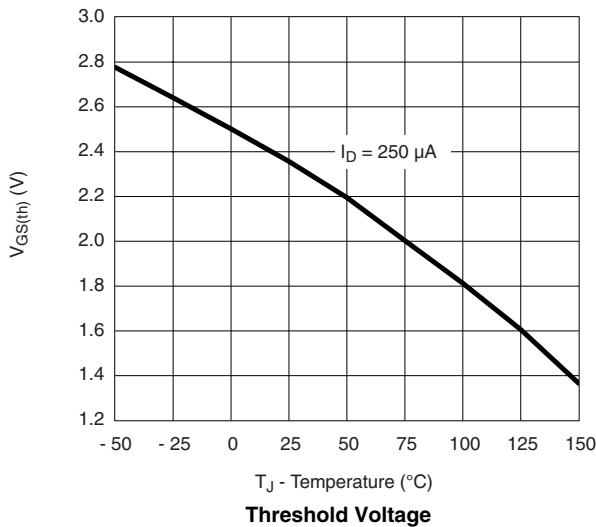
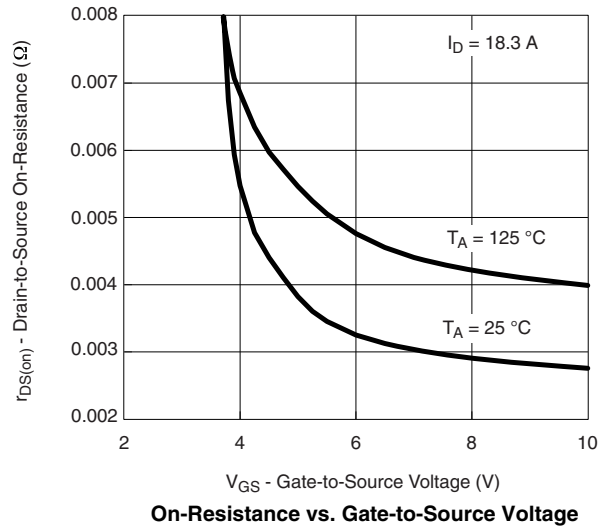
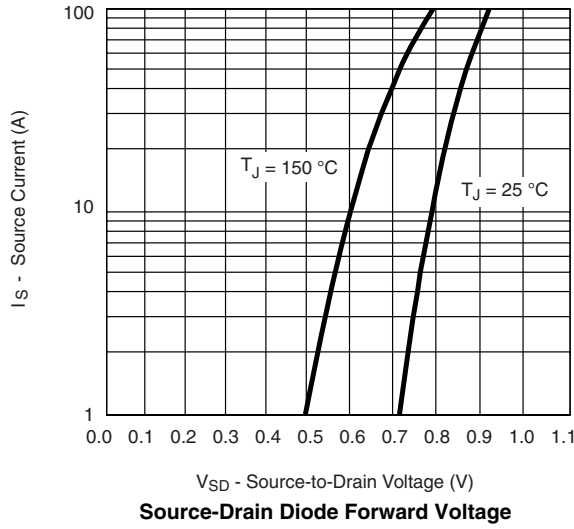
Gate Charge



On-Resistance vs. Junction Temperature

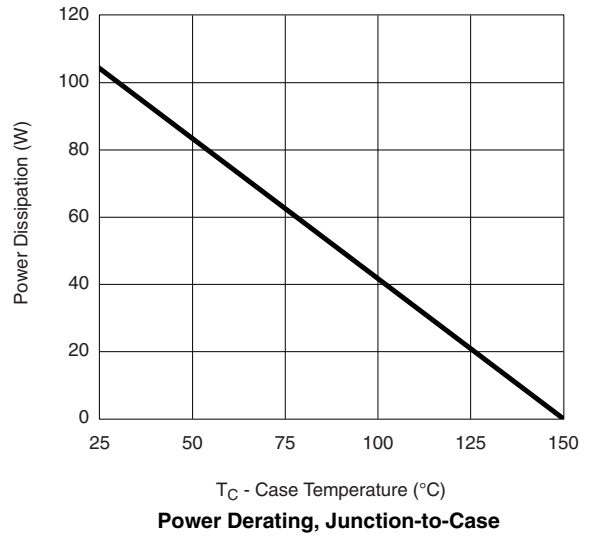
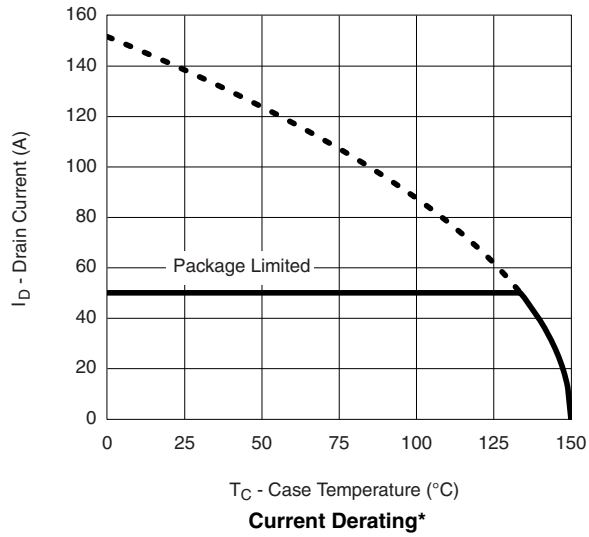


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





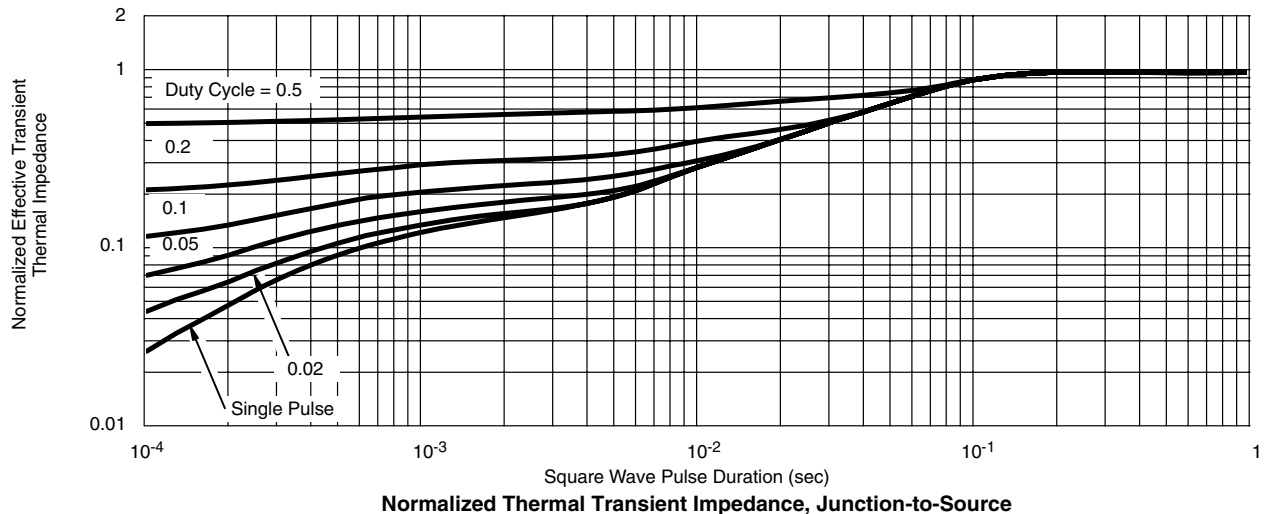
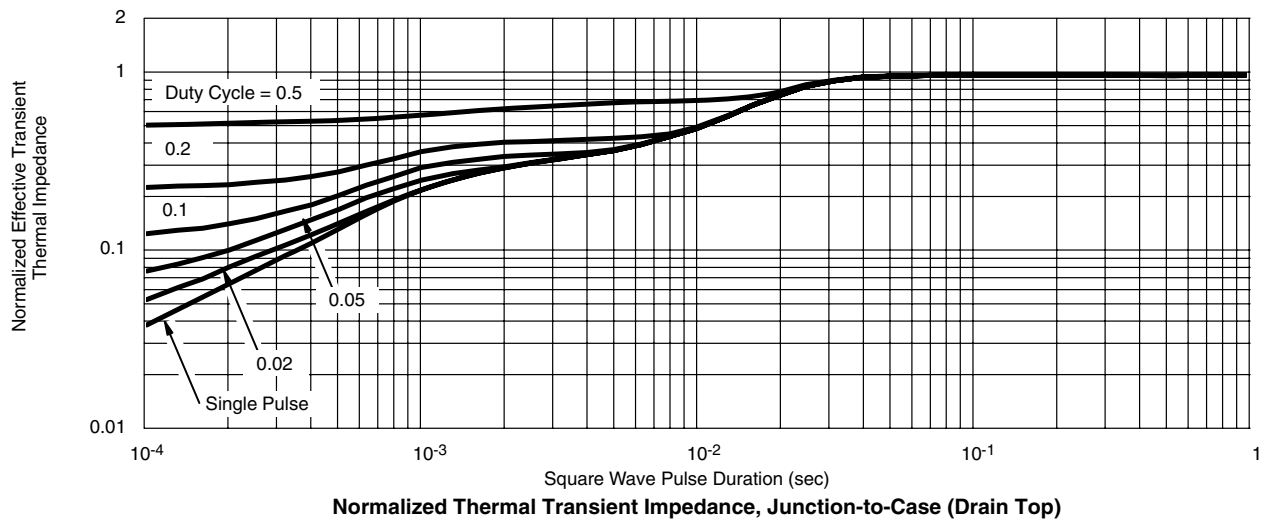
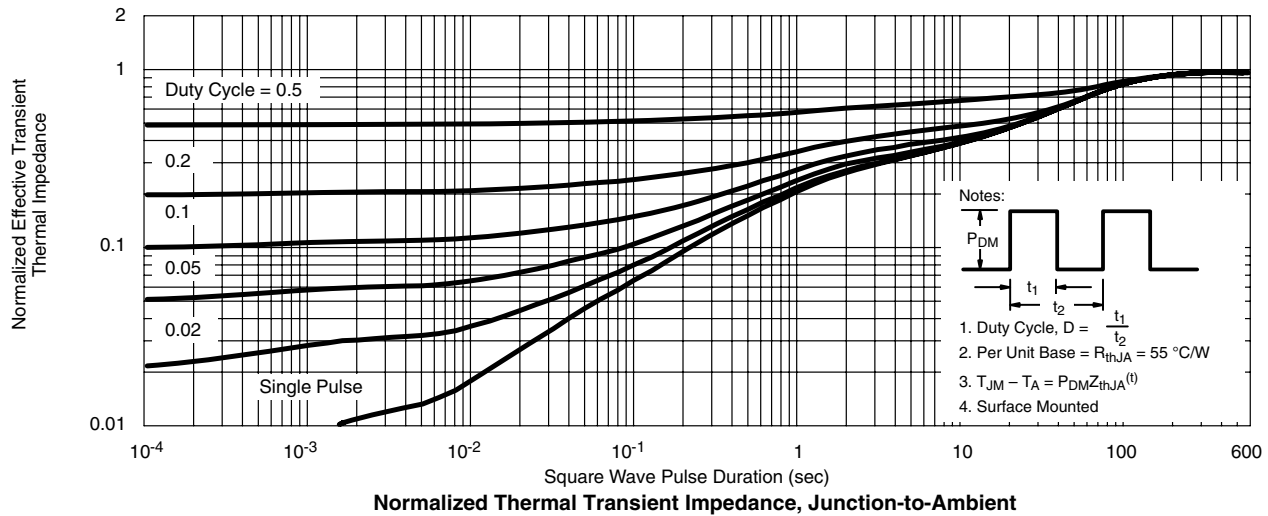
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?74451>.



Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.