P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVP4424C

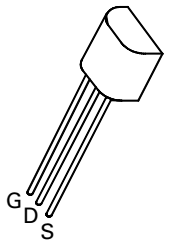
ISSUE 2 – SEPTEMBER 94

FEATURES

* 240 Volt V_{DS}
* $R_{DS(on)}$=9Ω
* Low threshold

APPLICATIONS

* Electronic Hook Switch



E-Line
TO92 Compatible

REFER TO ZVP4424A FOR GRAPHS

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	-240	V
Continuous Drain Current at T_{amb}=25°C	I_D	-200	mA
Pulsed Drain Current	I_{DM}	-1	A
Gate Source Voltage	V_{GS}	± 40	V
Power Dissipation at T_{amb}=25°C	P_{tot}	750	mW
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	TYP	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	-240			V	I_D=-1mA, V_{GS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	-0.7	-1.4	-2.0	V	ID=-1mA, V_{DS}= V_{GS}
Gate-Body Leakage	I_{GSS}			100	nA	V_{GS}=± 40V, V_{DS}=0V
Zero Gate Voltage Drain Current	I_{DSS}			-10 -100	μA μA	V_{DS}=-240 V, V_{GS}=0 V_{DS}=-190V, V_{GS}=0V, T=125°C
On-State Drain Current	$I_{D(on)}$	-0.75	-1.0		A	V_{DS}=-10 V, V_{GS}=-10V
Static Drain-Source On-State Resistance	$R_{DS(on)}$		7.1 8.8	9 11	Ω Ω	V_{GS}=-10V,I_D=-200mA V_{GS}=-3.5V,I_D=-100mA
Forward Transconductance (1) (2)	g_{fs}	125			mS	V_{DS}=-10V,I_D=-0.2A
Input Capacitance (2)	C_{iss}		100	200	pF	V_{DS}=-25V, V_{GS}=0V, f=1MHz
Common Source Output Capacitance (2)	C_{oss}		18	25	pF	
Reverse Transfer Capacitance (2)	C_{rss}		5	15	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		8	15	ns	V_{DD}≈-50V, I_D=-0.25A, V_{GEN}=-10V
Rise Time (2)(3)	t_r		8	15	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		26	40	ns	
Fall Time (2)(3)	t_f		20	30	ns	

(1) Measured under pulsed conditions. Width=300μs. Duty cycle ≤2% (2) Sample test.
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator