

FDN5632N_F085

N-Channel Logic Level PowerTrench® MOSFET

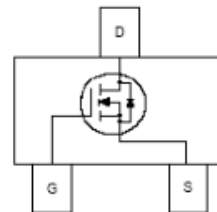
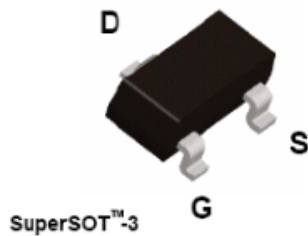
60V, 1.6A, 98mΩ

Features

- $R_{DS(on)} = 98m\Omega$ at $V_{GS} = 4.5V$, $I_D = 1.6A$
- $R_{DS(on)} = 82m\Omega$ at $V_{GS} = 10V$, $I_D = 1.7A$
- Typ $Q_{g(TOT)} = 9.2nC$ at $V_{GS} = 10V$
- Low Miller Charge
- Qualified to AEC Q101
- RoHS Compliant

Applications

- DC/DC converter
- Motor Drives



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($V_{GS} = 10\text{V}$)	1.7	A
	Pulsed	10	
P_D	Power Dissipation	1.1	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case	75	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in ² copper pad area	111	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
5632	FDN5632N_F085	SSOT3	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
		$T_A = 125^\circ\text{C}$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1	2.0	3	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 1.7\text{A}, V_{GS} = 10\text{V}$	-	57	82	m Ω
		$I_D = 1.6\text{A}, V_{GS} = 6\text{V}$	-	62	88	
		$I_D = 1.6\text{A}, V_{GS} = 4.5\text{V}$	-	70	98	
		$I_D = 1.7\text{A}, V_{GS} = 10\text{V}, T_A = 150^\circ\text{C}$	-	107	135	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	475	-	pF	
C_{oss}	Output Capacitance		-	60	-	pF	
C_{riss}	Reverse Transfer Capacitance		-	30	-	pF	
R_G	Gate Resistance	$f = 1\text{MHz}$	-	1.4	-	Ω	
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	$V_{DD} = 20\text{V}, I_D = 1.7\text{A}$	-	9.2	12	nC
Q_{gs}	Gate to Source Gate Charge			-	1.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	1.4	-	nC

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{on}	Turn-On Time	$V_{DD} = 30\text{V}$, $I_D = 1.0\text{A}$ $V_{GS} = 10\text{V}$, $R_{GEN} = 6\Omega$	-	-	30	ns
$t_{d(on)}$	Turn-On Delay Time		-	15	-	ns
t_r	Rise Time		-	1.7	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	5.2	-	ns
t_f	Fall Time		-	1.3	-	ns
t_{off}	Turn-Off Time		-	-	12.9	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 1.7\text{A}$	-	0.8	1.25	V
		$I_{SD} = 0.85\text{A}$	-	0.8	1.0	
t_{rr}	Reverse Recovery Time	$I_{SD} = 1.7\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	16.0	21	ns
Q_{rr}	Reverse Recovery Charge		-	7.9	10.3	nC

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics

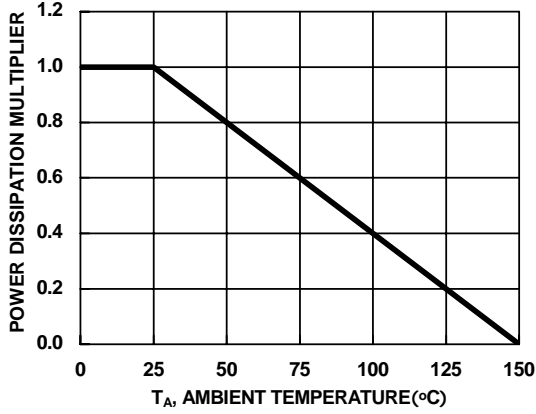


Figure 1. Normalized Power Dissipation vs Ambient Temperature

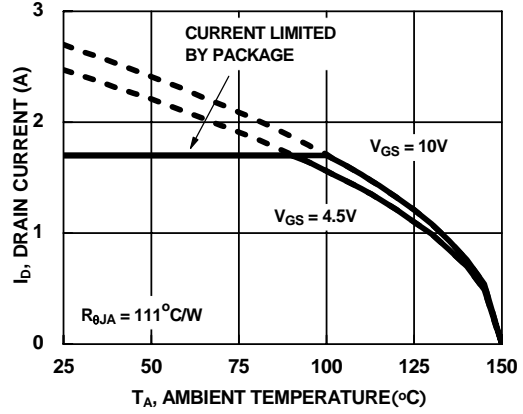


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

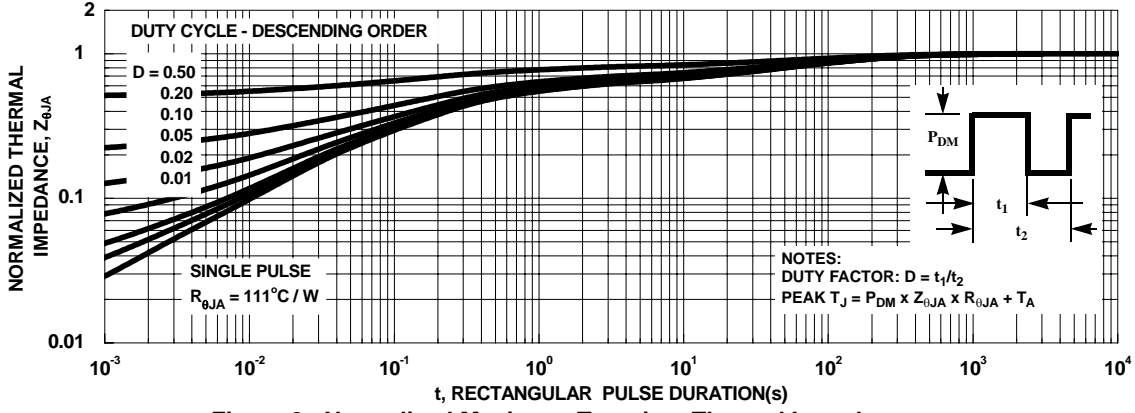


Figure 3. Normalized Maximum Transient Thermal Impedance

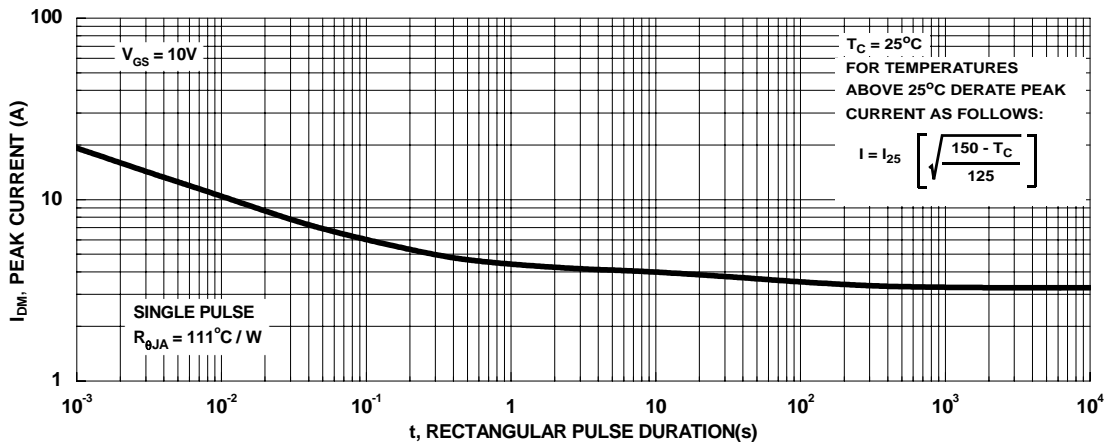


Figure 4. Peak Current Capability

Typical Characteristics

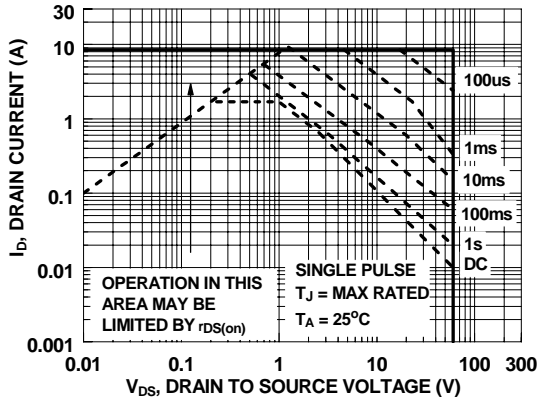


Figure 5. Forward Bias Safe Operating Area

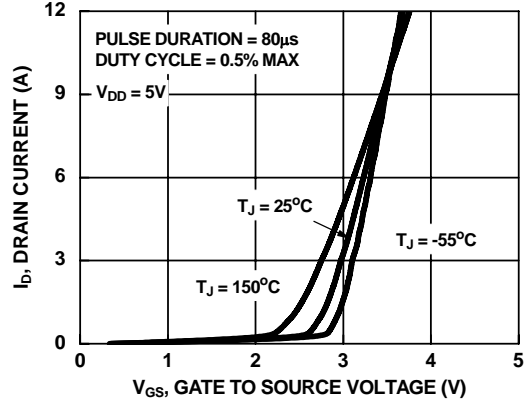


Figure 6. Transfer Characteristics

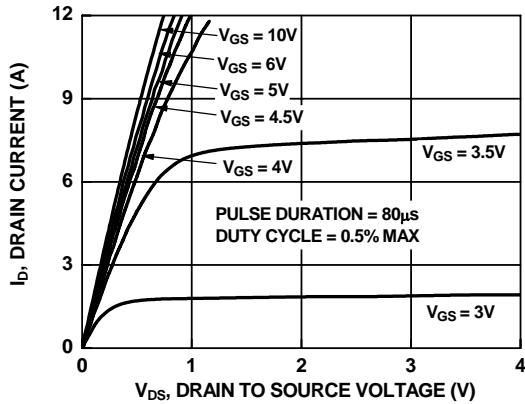


Figure 7. Saturation Characteristics

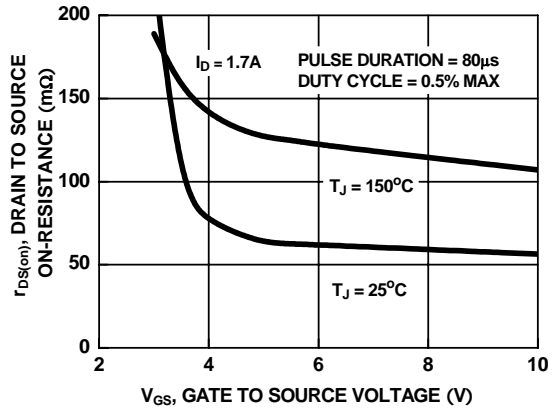


Figure 8. Drain to Source On-Resistance Variation vs Gate to Source Voltage

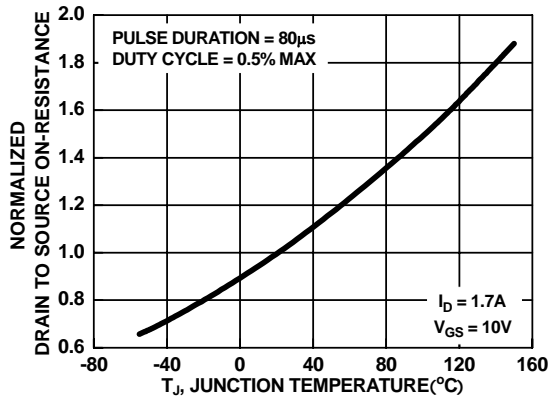


Figure 9. Normalized Drain to Source On-Resistance vs Junction Temperature

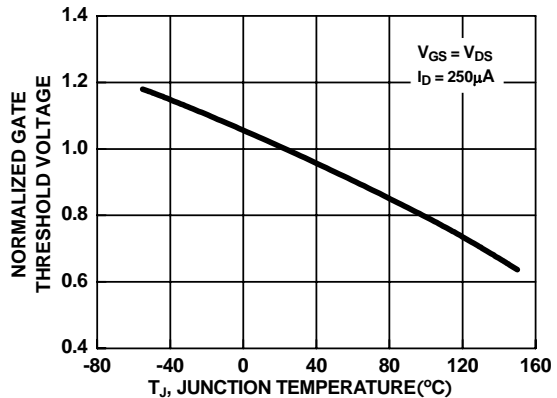


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristics

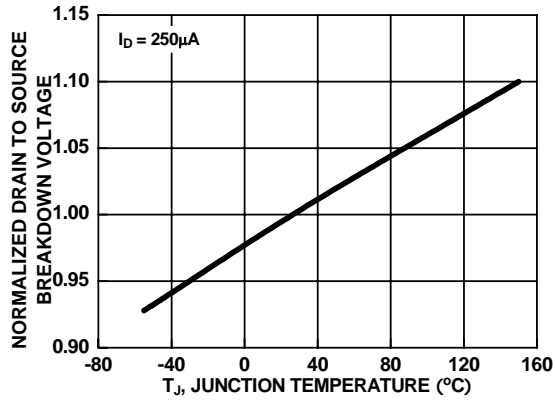


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

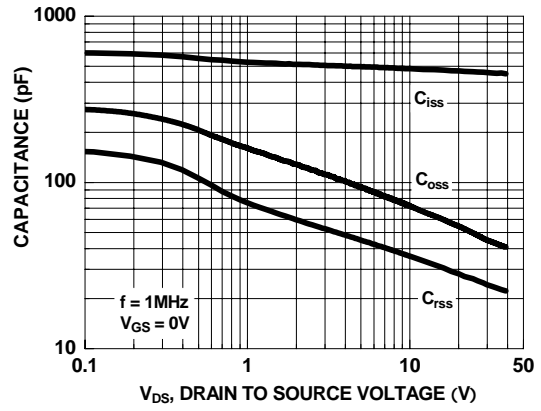


Figure 12. Capacitance vs Drain to Source Voltage

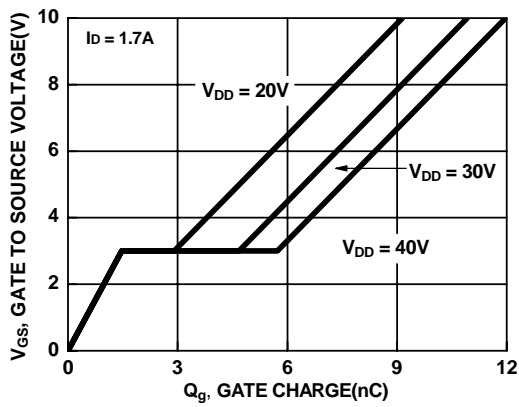








Figure 13. Gate Charge vs Gate to Source Voltage



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