NTMFS4108N

Power MOSFET

30 V, 35 A, Single N−Channel, SO−8 Flat Lead Package

Features

- Thermally and Electrically Enhanced Packaging Compatible with Standard SO−8 Package Footprint
- New Package Provides Capability of Inspection and Probe After Board Mounting
- Ultra Low $R_{DS(on)}$ (at 4.5 V_{GS}), Low Gate Resistance and Low Q_G
- Optimized for Low Side Synchronous Applications
- High Speed Switching Capability

Applications

- Notebook Computer Vcore Applications
- Network Applications
- DC−DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	22	A
		T_A = 85°C		16	
	t ≤ 10 s	T_A = 25°C		35	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	2.4	W
	t ≤ 10 s			6.25	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	13.5	A
		T_A = 85°C		10	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.91	W
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	100	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	203	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 150	°C
Continuous Source Current (Body Diode)			I_S	6.0	A
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 30 V, V_{GS} = 10 V, I_{PK} = 30 A, L = 1 mH, R_G = 25 Ω)			E_{AS}	450	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1″ sq. pad size (Cu area = 1.127″ sq. [1 oz] including traces).
2. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412″ sq.).

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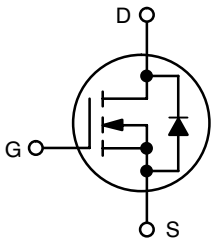
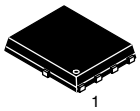
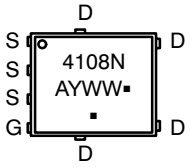
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	1.8 mΩ @ 10 V	35 A
	2.7 mΩ @ 4.5 V	





SO−8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



4108N = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4108NT1G	SO−8 FL (Pb−Free)	1500 Tape / Reel
NTMFS4108NT3G	SO−8 FL (Pb−Free)	5000 Tape / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	1.25	°C/W
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	53	
Junction−to−Ambient − t ≤ 10 s (Note 3)	$R_{\theta JA}$	20	
Junction−to−Ambient − Steady State (Note 4)	$R_{\theta JA}$	138	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			25	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				7.5		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 19 A			2.7	3.4	mΩ
		V_{GS} = 10 V, I_D = 21 A			1.8	2.2	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 10 A			25		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 15 V			6000		pF
Output Capacitance	C_{OSS}				1200		
Reverse Transfer Capacitance	C_{RSS}				700		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 24 V, I_D = 21 A			54		nC
Threshold Gate Charge	$Q_{G(TH)}$				11		
Gate−to−Source Charge	Q_{GS}				16		
Gate−to−Drain Charge	Q_{GD}				23		
Gate Resistance	R_G				0.7		Ω
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 6)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 1.0 A, R_G = 6.0 Ω			45		ns
Rise Time	t_r				60		
Turn−Off Delay Time	$t_{d(OFF)}$				70		
Fall Time	t_f				140		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 6.0 A	T_J = 25°C		0.72	1.1	V
			T_J = 125°C		0.65		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 6.0 A			41		ns
Charge Time	t_a				20		
Discharge Time	t_b				21		
Reverse Recovery Charge	Q_{RR}				45		nC

3. Surface−mounted on FR4 board using 1″ sq. pad size (Cu area = 1.127″ sq. [1 oz] including traces).
4. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412″ sq.).
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

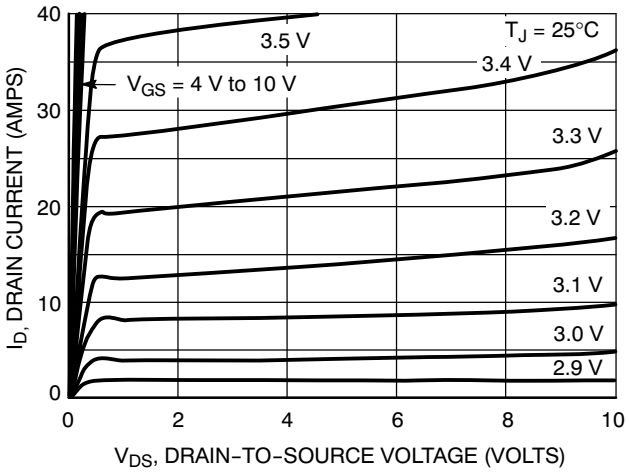


Figure 1. On−Region Characteristics

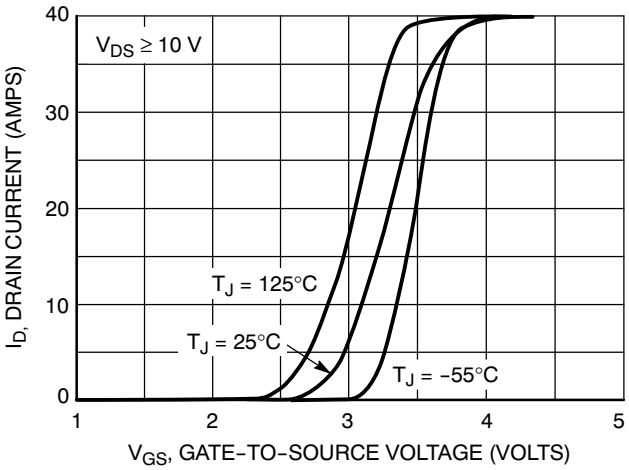


Figure 2. Transfer Characteristics

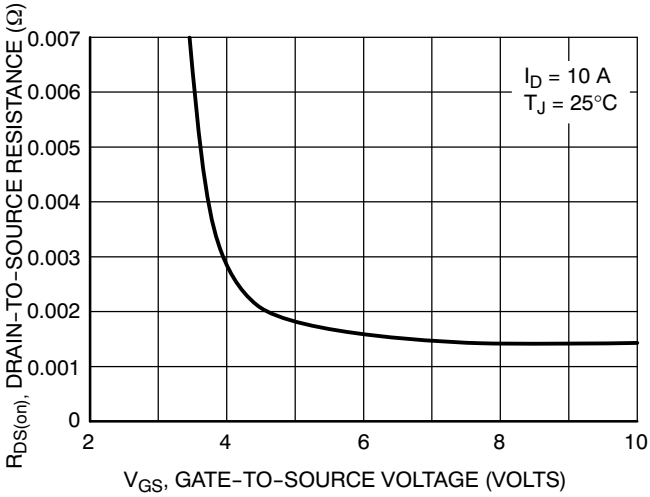


Figure 3. On−Resistance vs. Gate−to−Source Voltage

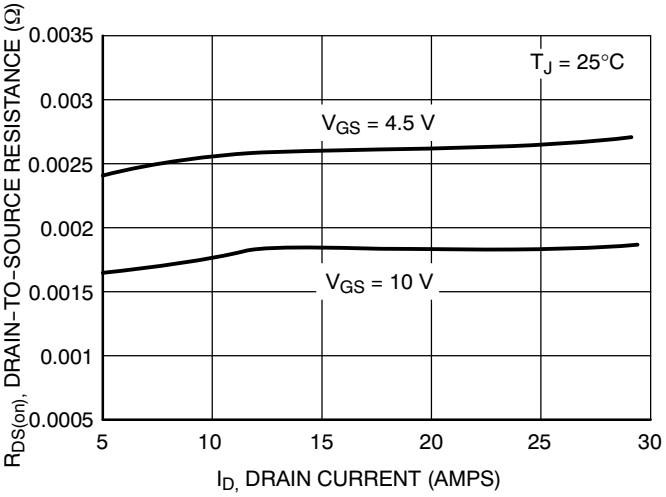


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

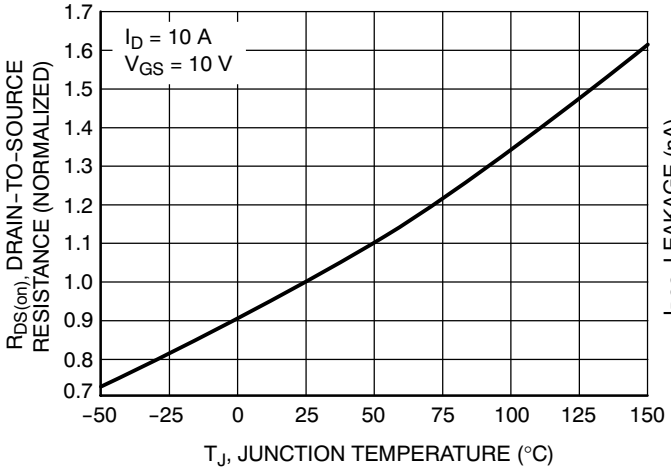


Figure 5. On−Resistance Variation with Temperature

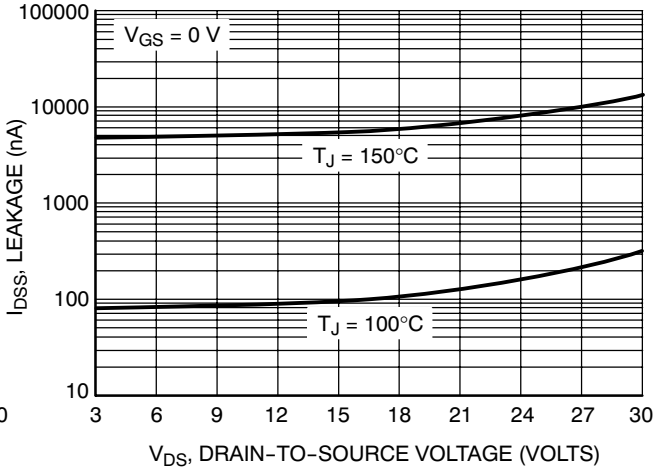


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

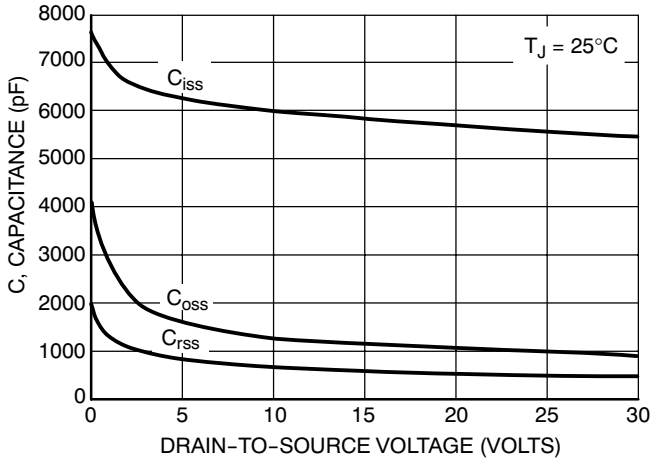


Figure 7. Capacitance Variation

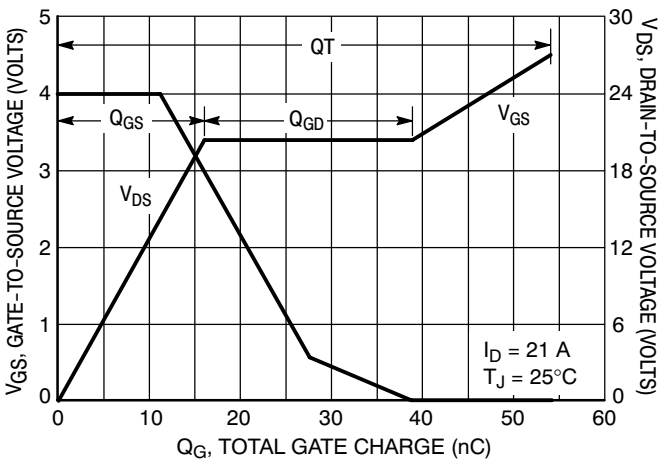


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

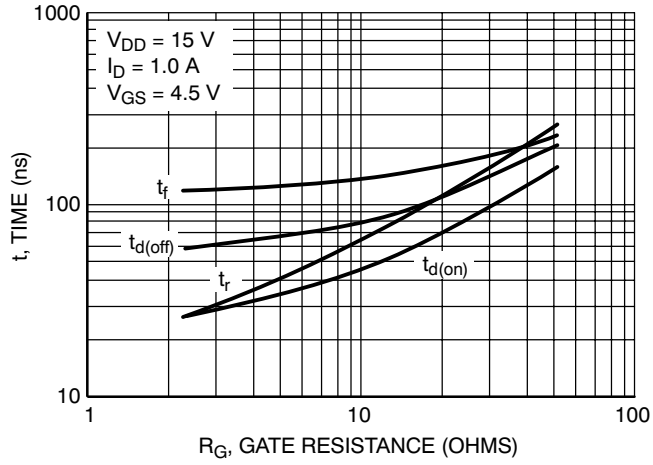


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

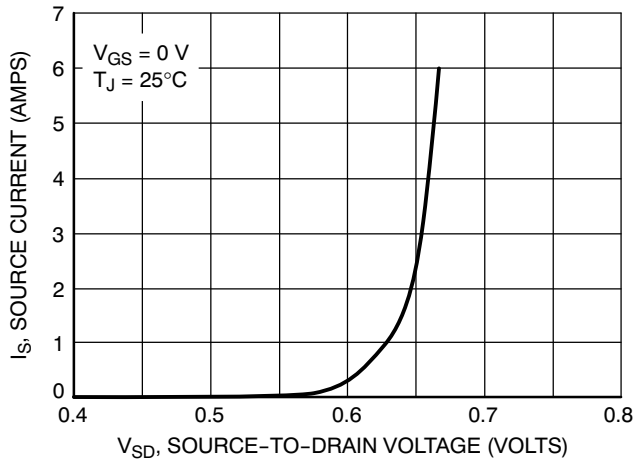


Figure 10. Diode Forward Voltage vs. Current

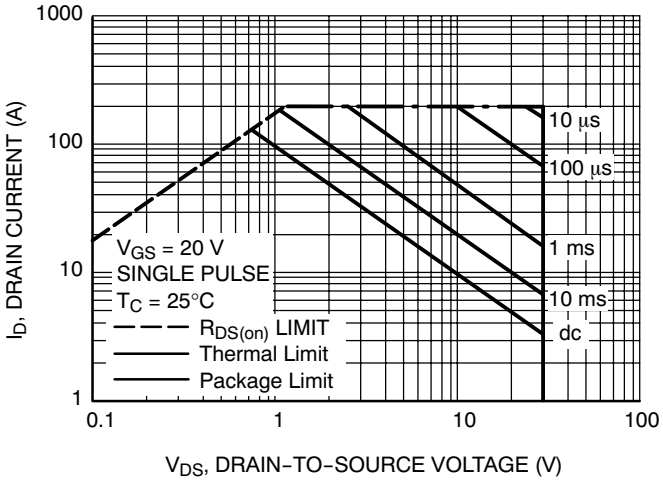
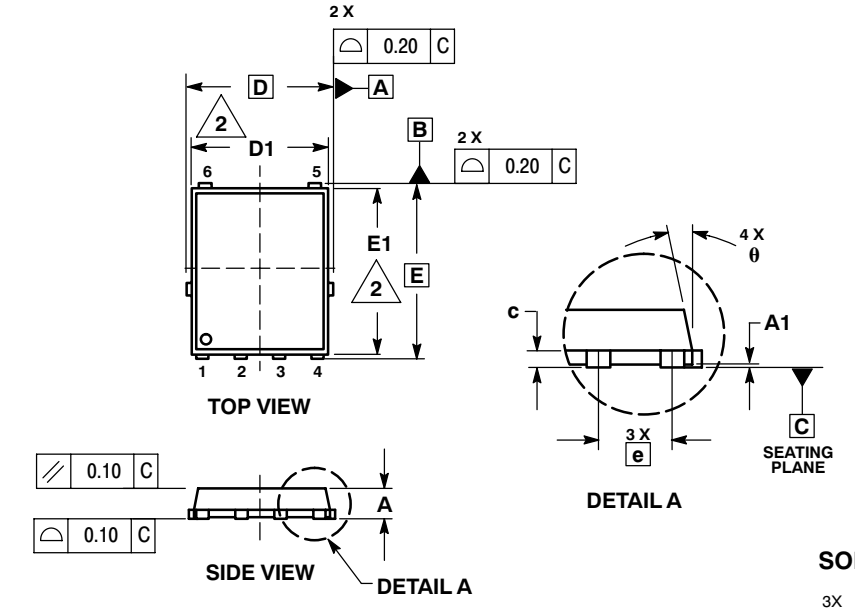


Figure 11. Maximum Rated Forward Biased Safe Operating Area

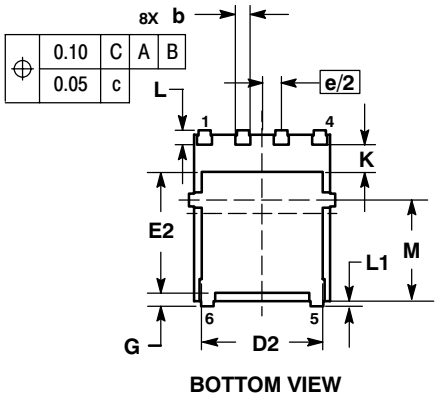
PACKAGE DIMENSIONS

DFN6 5x6, 1.27P (SO8 FL)
CASE 488AA−01
ISSUE C



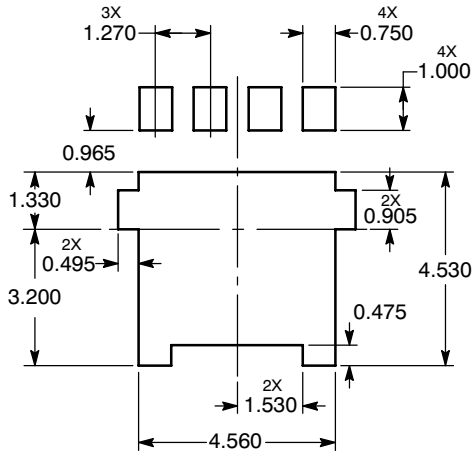
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D		5.15 BSC	
D1	4.50	4.90	5.10
D2	3.50	---	4.22
E		6.15 BSC	
E1	5.50	5.80	6.10
E2	3.45	---	4.30
e		1.27 BSC	
G	0.51	0.61	0.71
K	0.51	---	---
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	---	12 °



STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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