NEC

MOS FIELD EFFECT TRANSISTOR

μPA1792

SWITCHING
N- AND P-CHANNEL POWER MOS FET

DESCRIPTION

The μPA1792 is N- and P-channel MOS Field Effect Transistors designed for Motor Drive application of HDD and so on.

FEATURES

- Low on-state resistance

  N-channel $R_{DS(on)1}$ = 26 mΩ MAX. (V_{GS} = 10 V, I_D = 3.4 A)

  $R_{DS(on)2}$ = 36 mΩ MAX. (V_{GS} = 4.5 V, I_D = 3.4 A)

  $R_{DS(on)3}$ = 42 mΩ MAX. (V_{GS} = 4.0 V, I_D = 3.4 A)

  P-channel $R_{DS(on)1}$ = 36 mΩ MAX. (V_{GS} = –10 V, I_D = –2.9 A)

  $R_{DS(on)2}$ = 54 mΩ MAX. (V_{GS} = –4.5 V, I_D = –2.9 A)

  $R_{DS(on)3}$ = 65 mΩ MAX. (V_{GS} = –4.0 V, I_D = –2.9 A)

- Low input capacitance

  N-channel C_{iss} = 760 pF TYP.

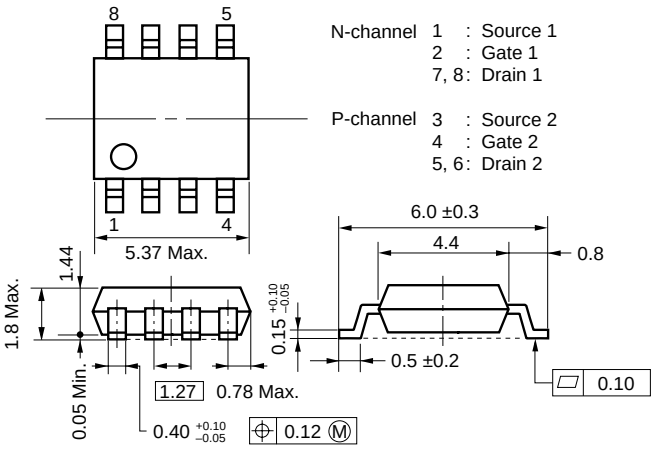
  P-channel C_{iss} = 900 pF TYP.

- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

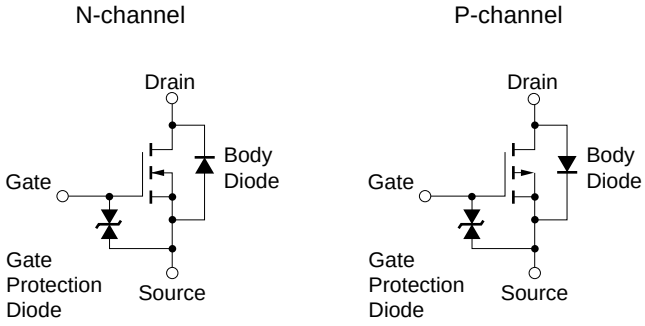
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1792G	Power SOP8

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Document No. G14557EJ3V0DS00 (3rd edition)
Date Published April 2003 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C. All terminals are connected.)

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	−30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	∓20	V
Drain Current (DC)	$I_{D(DC)}$	±6.8	∓5.8	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±27.2	∓23.2	A
Total Power Dissipation (1 unit) Note2	P_T	1.7		W
Total Power Dissipation (2 units) Note2	P_T	2.0		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 to +150		°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on ceramic substrate of 2000 mm^2 x 1.6 mm

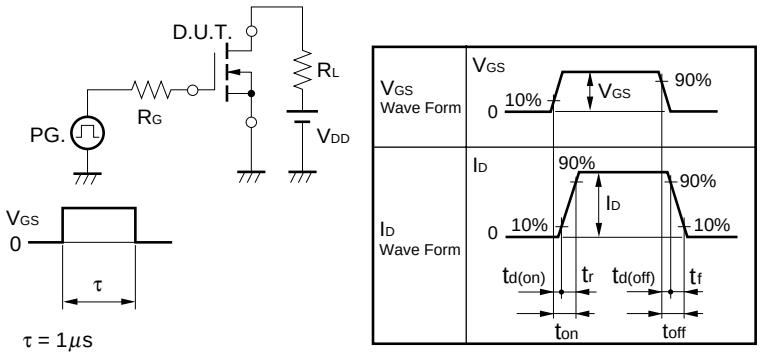
ELECTRICAL CHARACTERISTICS (T_A = 25°C. All terminals are connected.)

N-channel

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.1	2.5	V
Forward Transfer Admittance **Note**	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 3.4 A	3.0	7.5		S
Drain to Source On-state Resistance **Note**	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 3.4 A		20.5	26	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 3.4 A		27	36	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 3.4 A		31	42	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		760		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		250		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		95		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 3.4 A		20		ns
Rise Time	t_r	V_{GS} = 10 V		140		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		50		ns
Fall Time	t_f			30		ns
Total Gate Charge	Q_G	I_D = 6.8 A		14		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 24 V		2		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		5		nC
Body Diode Forward Voltage **Note**	$V_{F(S-D)}$	I_F = 6.8 A, V_{GS} = 0 V		0.86		V
Reverse Recovery Time	t_{rr}	I_F = 6.8 A, V_{GS} = 0 V		30		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		20		nC

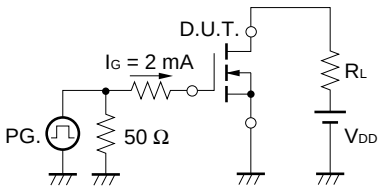
Note Pulse: PW ≤ 350 μs, Duty Cycle ≤ 2%

TEST CIRCUIT 1 SWITCHING TIME



τ = 1μs
Duty Cycle ≤ 1%

TEST CIRCUIT 2 GATE CHARGE

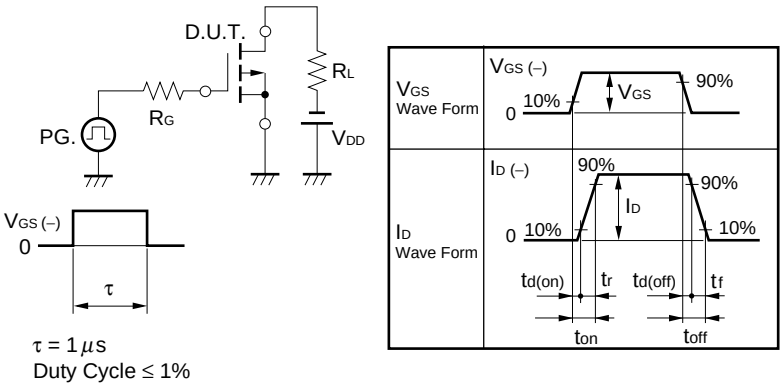


P-channel

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓16 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.5	–2.0	–2.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –2.9 A	3.5	8.0		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –2.9 A		30	36	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –2.9 A		43	54	mΩ
	$R_{DS(on)3}$	V_{GS} = –4.0 V, I_D = –2.9 A		49	65	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		900		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		300		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		120		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V, I_D = –2.9 A		23		ns
Rise Time	t_r	V_{GS} = –10 V		220		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		90		ns
Fall Time	t_f			70		ns
Total Gate Charge	Q_G	I_D = –5.8 A		17		nC
Gate to Source Charge	Q_{GS}	V_{DD} = –24 V		2.5		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = –10 V		4.0		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 5.8 A, V_{GS} = 0 V		0.85		V
Reverse Recovery Time	t_{rr}	I_F = 5.8 A, V_{GS} = 0 V		40		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		30		nC

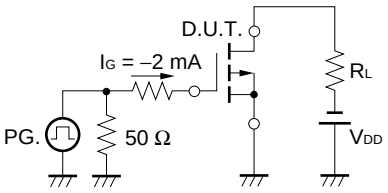
Note Pulse: PW ≤ 350 μs, Duty Cycle ≤ 2%

TEST CIRCUIT 1 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

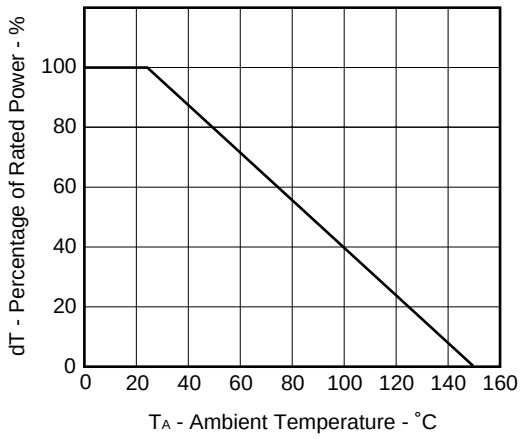
TEST CIRCUIT 2 GATE CHARGE



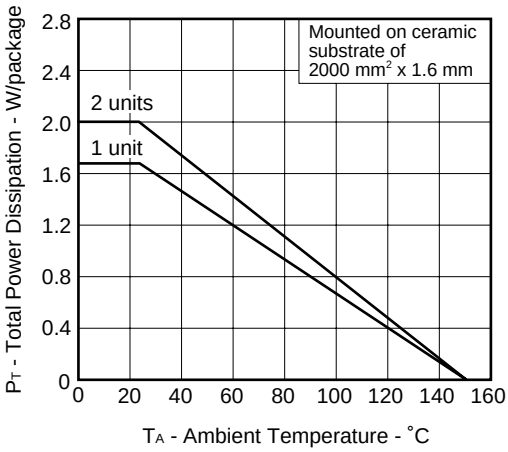
TYPICAL CHARACTERISTICS (T_A = 25°C)

(1) N-channel

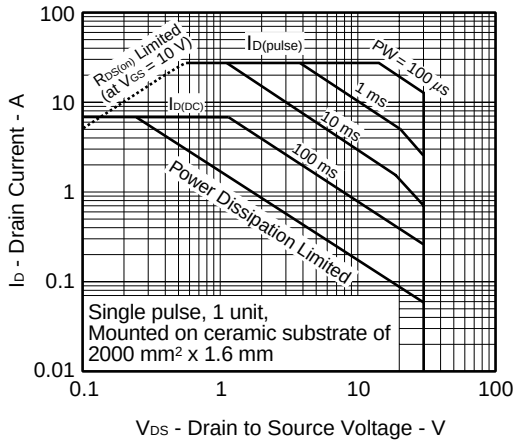
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



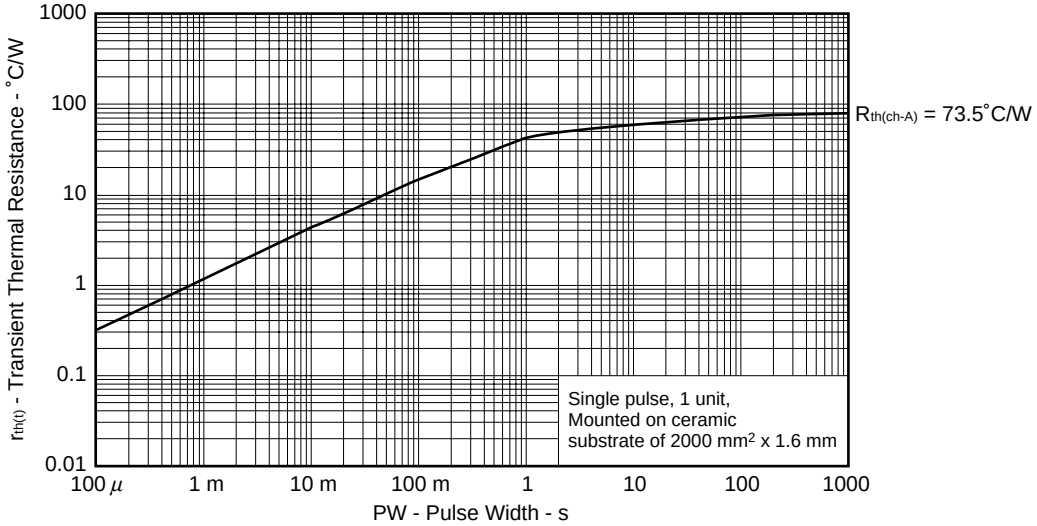
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



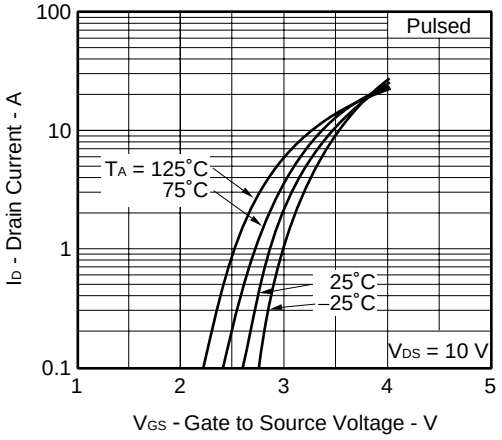
★ FORWARD BIAS SAFE OPERATING AREA



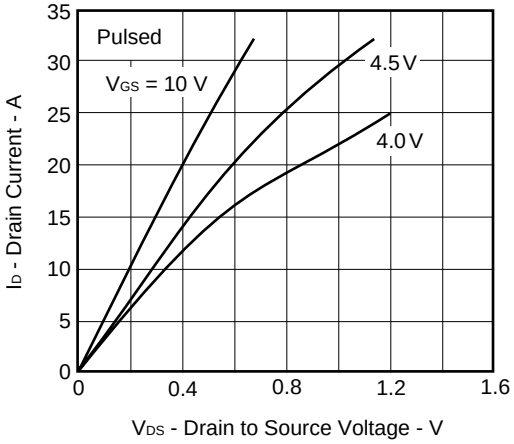
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



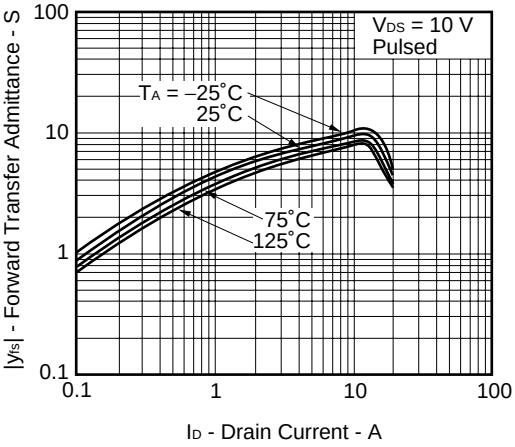
FORWARD TRANSFER CHARACTERISTICS



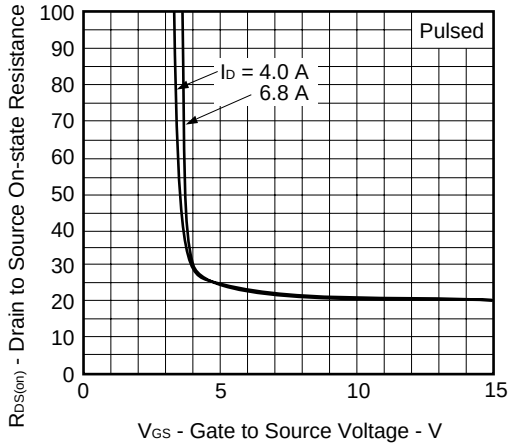
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



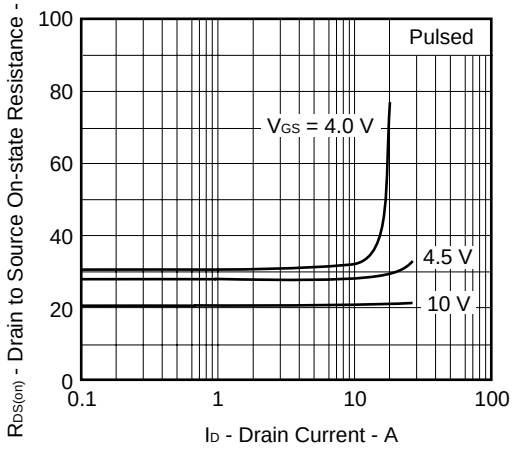
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



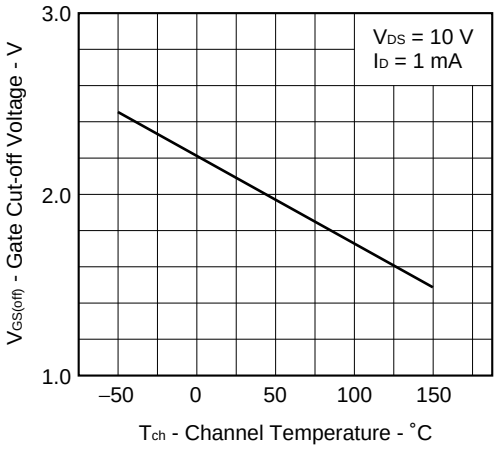
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



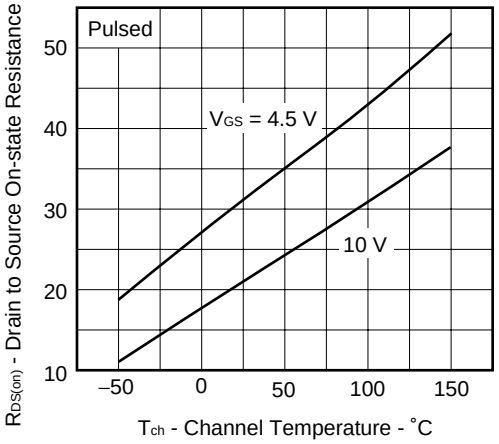
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



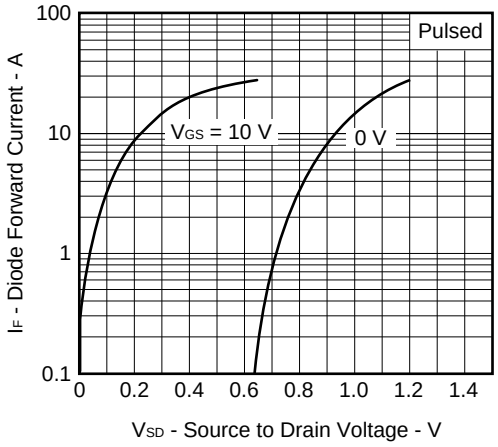
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



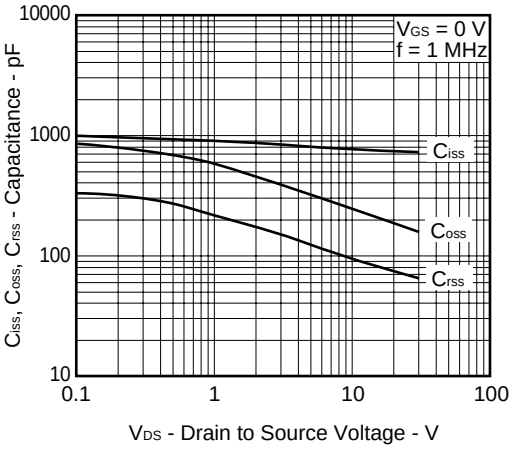
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



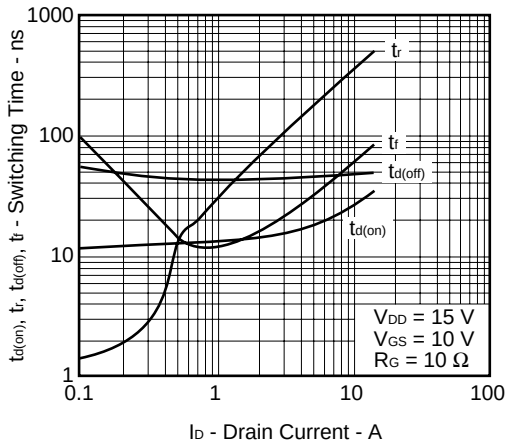
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



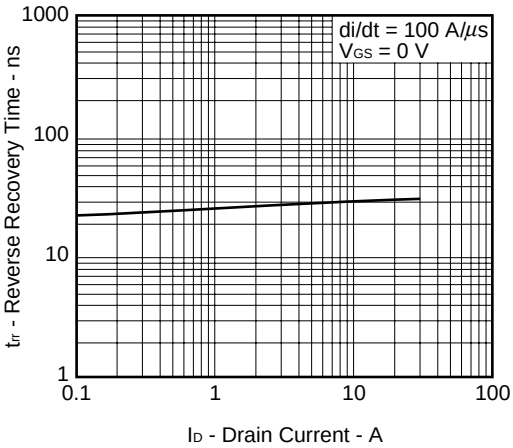
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



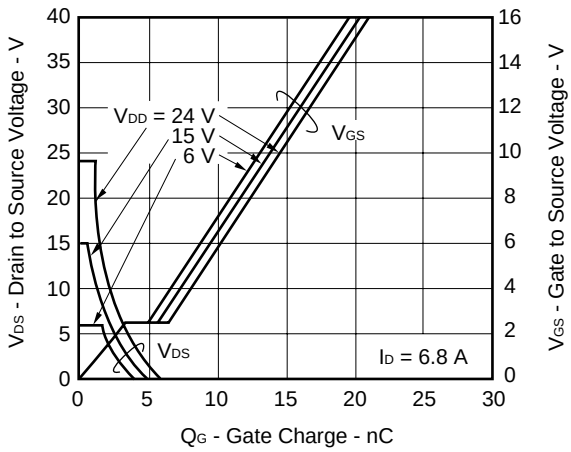
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT

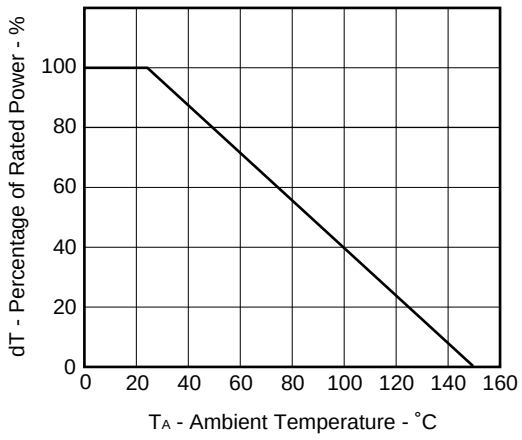


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

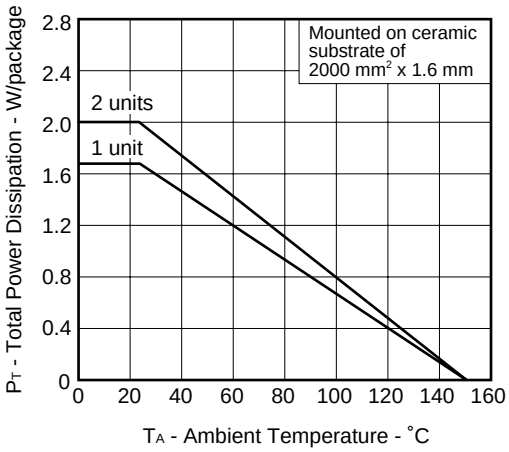


(2) P-channel

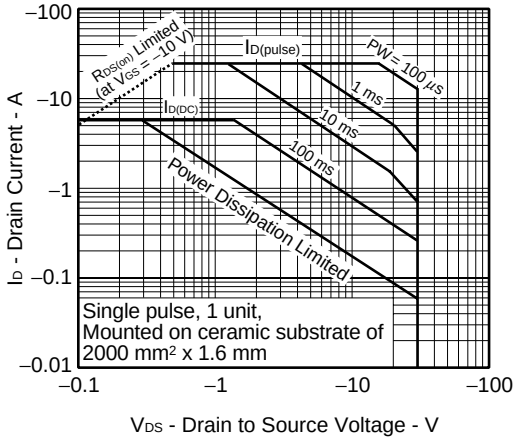
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



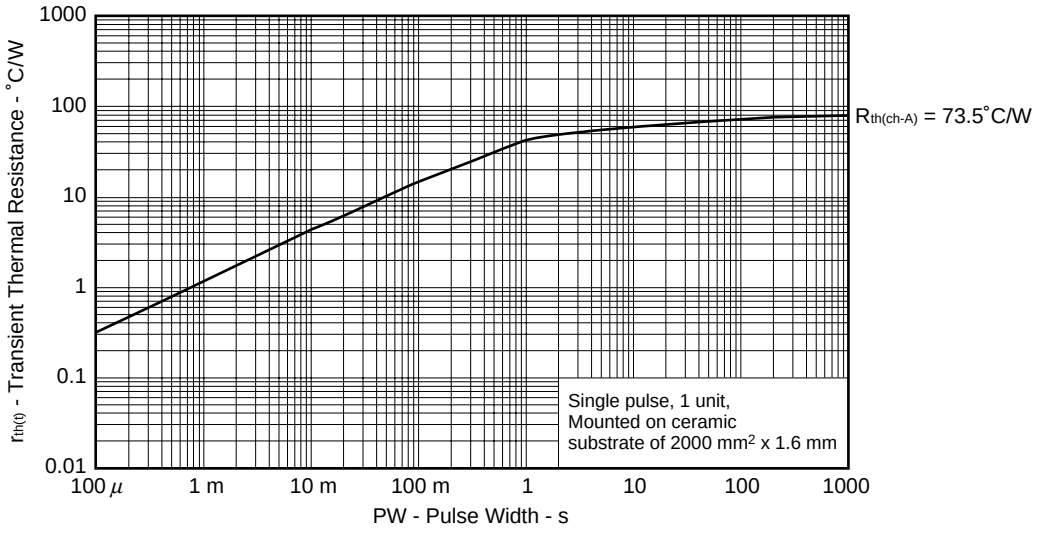
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



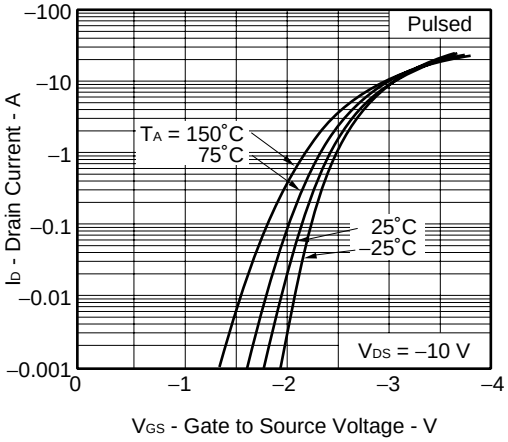
★ FORWARD BIAS SAFE OPERATING AREA



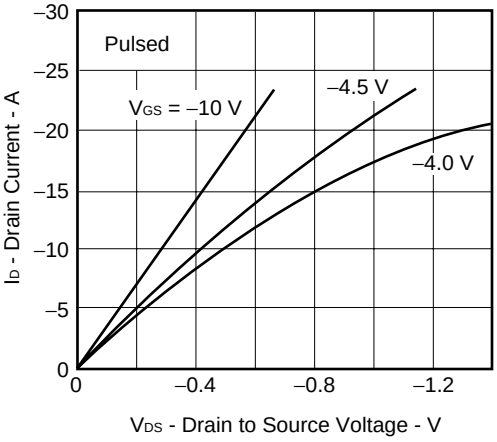
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



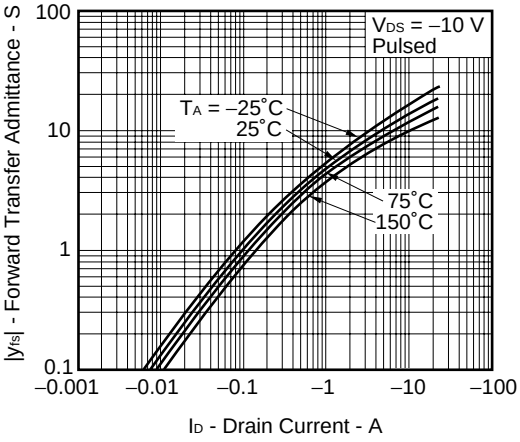
FORWARD TRANSFER CHARACTERISTICS



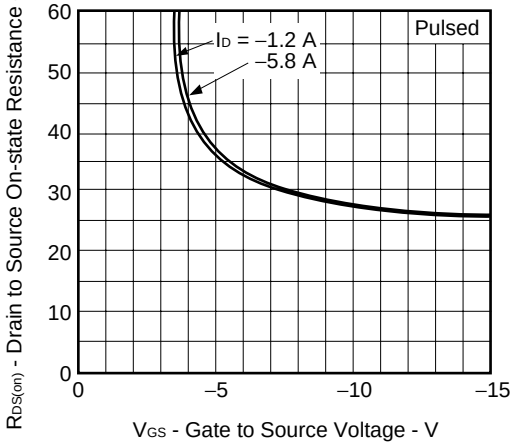
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



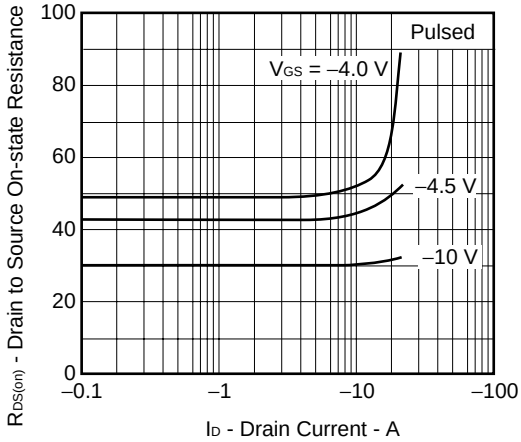
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



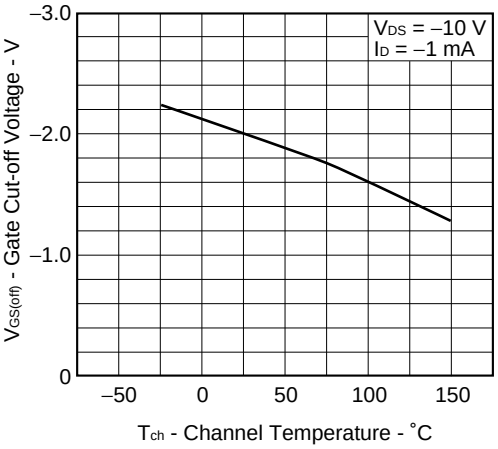
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



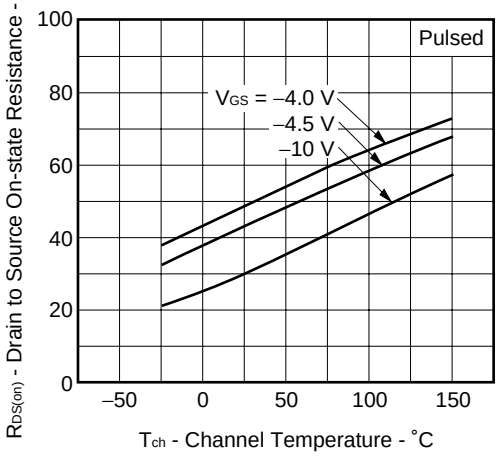
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



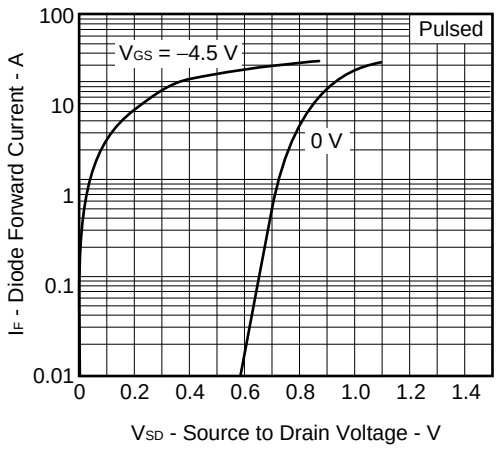
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



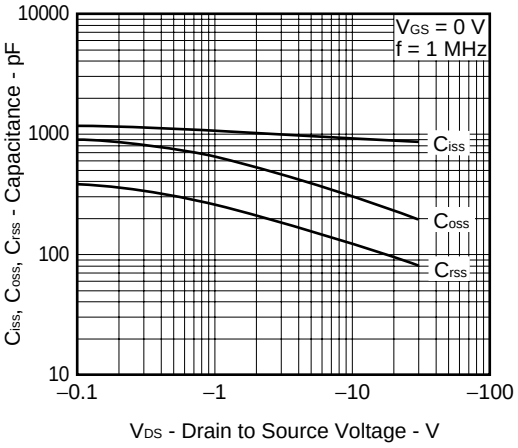
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



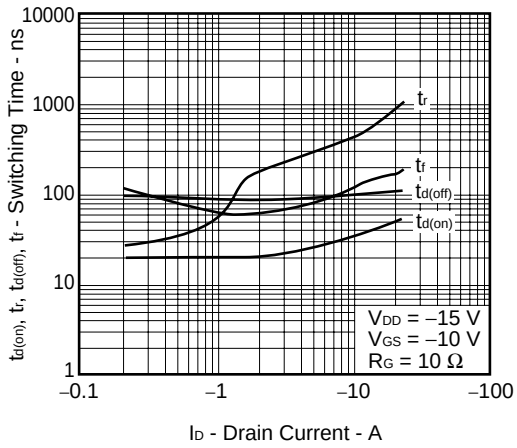
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



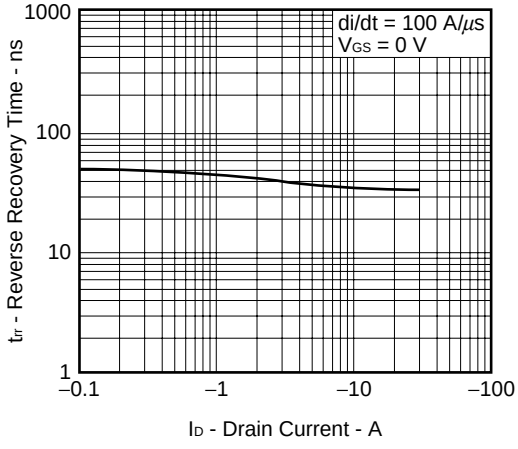
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



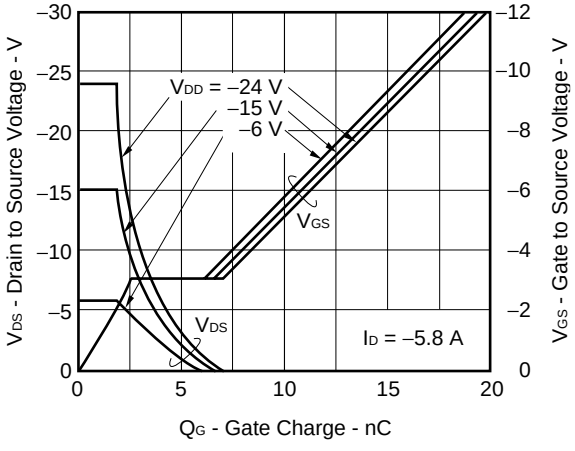
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



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M8E 02. 11-1