

NCV8664

Very Low I_q Low Dropout Linear Regulator

The NCV8664 is a precision 3.3 V and 5.0 V fixed output, low dropout integrated voltage regulator with an output current capability of 150 mA. Careful management of light load current consumption, combined with a low leakage process, achieve a typical quiescent current of 22 μ A.

NCV8664 is pin and functionally compatible with NCV4264 and NCV4264-2, and it could replace these parts when very low quiescent current is required.

The output voltage is accurate within $\pm 2.0\%$, and maximum dropout voltage is 600 mV at full rated load current.

It is internally protected against input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Features

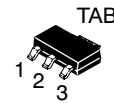
- 3.3 V, 5.0 V Fixed Output
- $\pm 2.0\%$ Output Accuracy, Over Full Temperature Range
- 30 μ A Maximum Quiescent Current at $I_{OUT} = 100 \mu$ A
- 600 mV Maximum Dropout Voltage at 150 mA Load Current
- Wide Input Voltage Operating Range of 4.5 V to 45 V
- Internal Fault Protection
 - ◆ -42 V Reverse Voltage
 - ◆ Short Circuit/Overcurrent
 - ◆ Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- AEC-Q100 Qualified
- EMC Compliant
- This is a Pb-Free Device



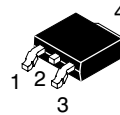
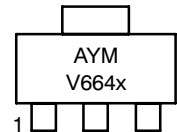
ON Semiconductor®

<http://onsemi.com>

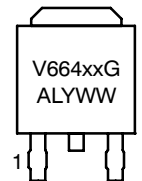
MARKING DIAGRAMS



SOT-223
ST SUFFIX
CASE 318E



DPAK
DT SUFFIX
CASE 369C



xx = Voltage Rating DPAK
(50 = 5.0 V Version)
(33 = 3.3 V Version)

x = Voltage Rating SOT223
(5 = 5.0 V Version)
(3 = 3.3 V Version)

A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
M = Date Code
G = Pb-Free Package

PIN CONNECTIONS

| PIN | FUNCTION |
|--------|-----------|
| 1 | V_{IN} |
| 2, TAB | GND |
| 3 | V_{OUT} |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

NCV8664

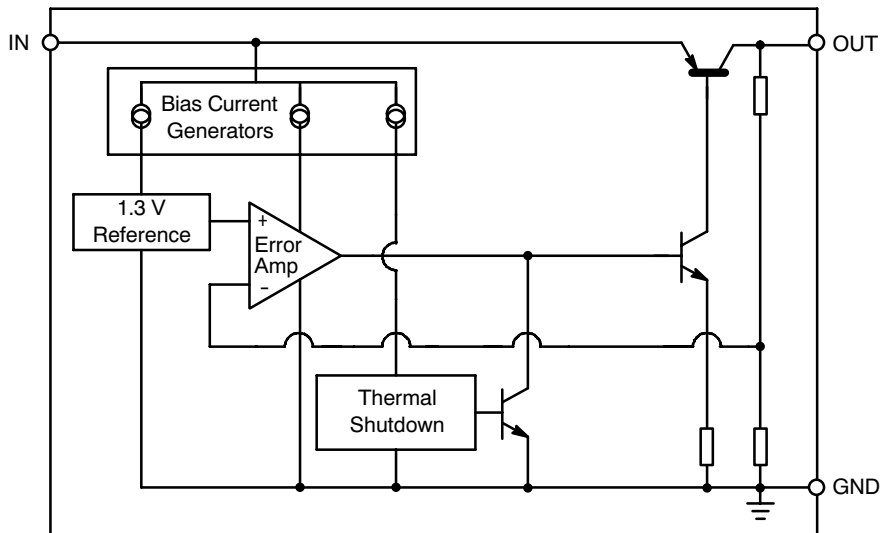


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

| Pin No. | Symbol | Function |
|---------|-----------|--|
| 1 | V_{IN} | Unregulated input voltage; 4.5 V to 45 V. |
| 2 | GND | Ground; substrate. |
| 3 | V_{OUT} | Regulated output voltage; collector of the internal PNP pass transistor. |
| TAB | GND | Ground; substrate and best thermal connection to the die. |

OPERATING RANGE

| Pin Symbol, Parameter | Symbol | Min | Max | Unit |
|---------------------------------------|----------|-----|------|------|
| V_{IN} , DC Input Operating Voltage | V_{IN} | 4.5 | +45 | V |
| Junction Temperature Operating Range | T_J | -40 | +150 | °C |

MAXIMUM RATINGS

| Rating | Symbol | Min | Max | Unit |
|---|--------------|------|------|------|
| V_{IN} , DC Voltage | V_{IN} | -42 | +45 | V |
| V_{OUT} , DC Voltage | V_{OUT} | -0.3 | +16 | V |
| Storage Temperature | T_{stg} | -55 | +150 | °C |
| ESD Capability, Human Body Model (Note 1) | V_{ESDHB} | 4000 | - | V |
| ESD Capability, Machine Model (Note 1) | V_{ESDMIM} | 200 | - | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- This device series incorporates ESD protection and is tested by the following methods:
 ESD HBM tested per AEC-Q100-002 (EIA/JESD22-A 114C)
 ESD MM tested per AEC-Q100-003 (EIA/JESD22-A 115C)

Thermal Resistance

| Parameter | Symbol | Condition | Min | Max | Unit |
|---------------------|-----------------|-----------|-----|--------------|------|
| Junction-to-Ambient | $R_{\theta JA}$ | DPAK | - | 101 (Note 2) | °C/W |
| Junction-to-Ambient | $R_{\theta JA}$ | SOT-223 | - | 99 (Note 2) | °C/W |
| Junction-to-Case | $R_{\theta JC}$ | DPAK | - | 9.0 | °C/W |
| Junction-to-Case | $R_{\theta JC}$ | SOT-223 | - | 17 | °C/W |

- 1 oz., 100 mm² copper area.

NCV8664

Lead Soldering Temperature and MSL

| Rating | Symbol | Min | Max | Unit |
|--|-------------------|--------|--------|--------------------|
| Lead Temperature Soldering Reflow (SMD Styles Only), Lead Free (Note 3) | T_{slid} | - | 265 pk | $^{\circ}\text{C}$ |
| Moisture Sensitivity Level SOT223 DPAK | MSL | 3 1 | - - | - |

3. Lead Free, 60 sec – 150 sec above 217 $^{\circ}\text{C}$, 40 sec max at peak.

ELECTRICAL CHARACTERISTICS ($V_{\text{IN}} = 13.5\text{ V}$, $T_{\text{J}} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, unless otherwise noted.)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---------|------------|----------------|---------------------------|
| Output Voltage 5.0 V Version | V_{OUT} | $0.1\text{ mA} \leq I_{\text{OUT}} \leq 150\text{ mA}$ (Note 4) $6.0\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$ | 4.900 | 5.000 | 5.100 | V |
| Output Voltage 3.3 V Version | V_{OUT} | $0.1\text{ mA} \leq I_{\text{OUT}} \leq 150\text{ mA}$ (Note 4) $4.5\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$ | 3.234 | 3.300 | 3.366 | V |
| Line Regulation 5.0 V Version | $\Delta V_{\text{OUT vs. } V_{\text{IN}}}$ | $I_{\text{OUT}} = 5.0\text{ mA}$ $6.0\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$ | -25 | 5.0 | +25 | mV |
| Line Regulation 3.3 V Version | $\Delta V_{\text{OUT vs. } V_{\text{IN}}}$ | $I_{\text{OUT}} = 5.0\text{ mA}$ $4.5\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$ | -25 | 5.0 | +25 | mV |
| Load Regulation | $\Delta V_{\text{OUT vs. } I_{\text{OUT}}}$ | $1.0\text{ mA} \leq I_{\text{OUT}} \leq 150\text{ mA}$ (Note 4) | -35 | 5.0 | +35 | mV |
| Dropout Voltage 5.0 V Version | $V_{\text{IN}} - V_{\text{OUT}}$ | $I_{\text{Q}} = 100\text{ mA}$ (Notes 4 & 5) $I_{\text{Q}} = 150\text{ mA}$ (Notes 4 & 5) | - - | 265 315 | 500 600 | mV |
| Dropout Voltage 3.3 V Version | $V_{\text{IN}} - V_{\text{OUT}}$ | $I_{\text{Q}} = 100\text{ mA}$ (Notes 4 & 7) $I_{\text{Q}} = 150\text{ mA}$ (Notes 4 & 7) | - - | - - | 1.266 1.266 | V |
| Quiescent Current | I_{q} | $I_{\text{OUT}} = 100\text{ }\mu\text{A}$ $T_{\text{J}} = 25^{\circ}\text{C}$ $T_{\text{J}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | - - | 21 22 | 29 30 | μA |
| Active Ground Current | $I_{\text{G(ON)}}$ | $I_{\text{OUT}} = 50\text{ mA}$ (Note 4) $I_{\text{OUT}} = 150\text{ mA}$ (Note 4) | - - | 1.3 8.0 | 3 15 | mA |
| Power Supply Rejection | PSRR | $V_{\text{RIPPLE}} = 0.5\text{ V}_{\text{P-P}}$, $F = 100\text{ Hz}$ | - | 67 | - | dB |
| Output Capacitor for Stability 5.0 V Version | C_{OUT} ESR | $I_{\text{OUT}} = 0.1\text{ mA}$ to 150 mA (Note 4) | 10 - | - - | - 9.0 | μF Ω |
| Output Capacitor for Stability 3.3 V Version | C_{OUT} ESR | $I_{\text{OUT}} = 0.1\text{ mA}$ to 150 mA (Note 4) | 22 - | - - | - 18 | μF Ω |

PROTECTION

| | | | | | | |
|-----------------------------|-----------------------|--|------------|--------|------------|--------------------|
| Current Limit | $I_{\text{OUT(LIM)}}$ | $V_{\text{OUT}} = 4.5\text{ V}$ (5.0 V Version) (Note 4) $V_{\text{OUT}} = 3.0\text{ V}$ (3.3 V Version) (Note 4) | 150 150 | - - | 500 500 | mA |
| Short Circuit Current Limit | $I_{\text{OUT(SC)}}$ | $V_{\text{OUT}} = 0\text{ V}$ (Note 4) | 100 | - | 500 | mA |
| Thermal Shutdown Threshold | T_{TSD} | (Note 6) | 150 | - | 200 | $^{\circ}\text{C}$ |

4. Use pulse loading to limit power dissipation.

5. Dropout voltage = $(V_{\text{IN}} - V_{\text{OUT}})$, measured when the output voltage has dropped 100 mV relative to the nominal value obtained with $V_{\text{IN}} = 13.5\text{ V}$.

6. Not tested in production. Limits are guaranteed by design.

7. $V_{\text{DO}} = V_{\text{IN}} - V_{\text{OUT}}$. For output voltage set to $< 4.5\text{ V}$, V_{DO} will be constrained by the minimum input voltage.

NCV8664

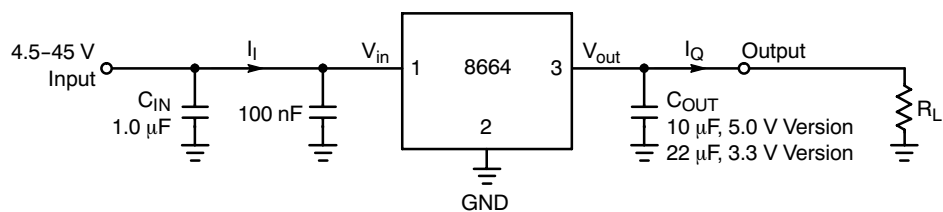


Figure 2. Measurement Circuit

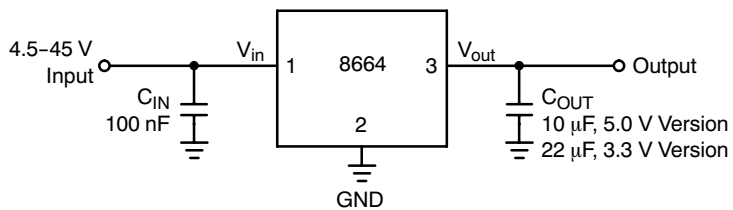


Figure 3. Applications Circuit

Typical Curves

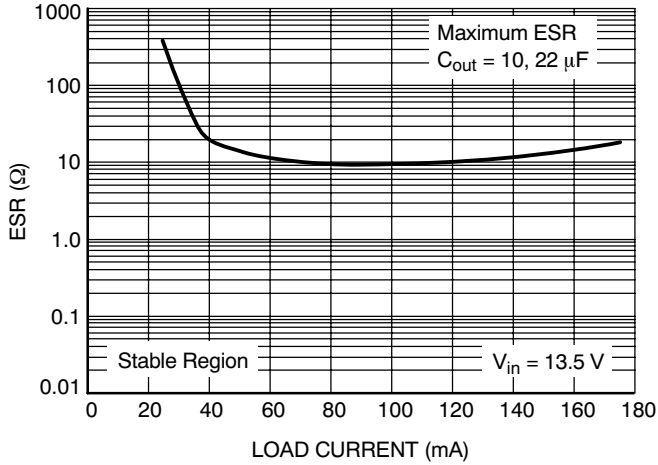


Figure 4. ESR Characterization, 5.0 V Version

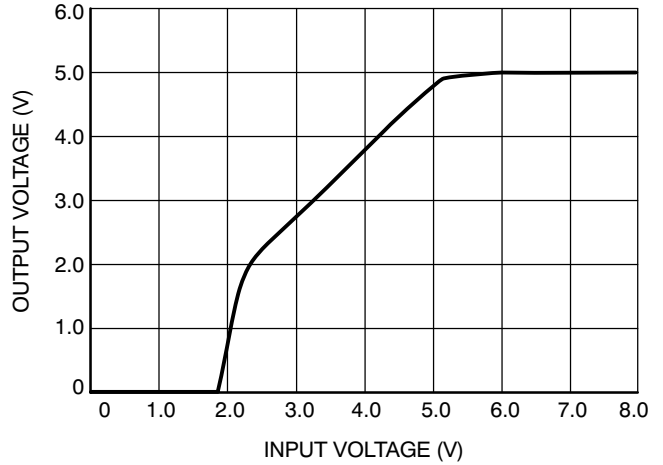


Figure 5. Output Voltage vs. Input Voltage, 5.0 V Version

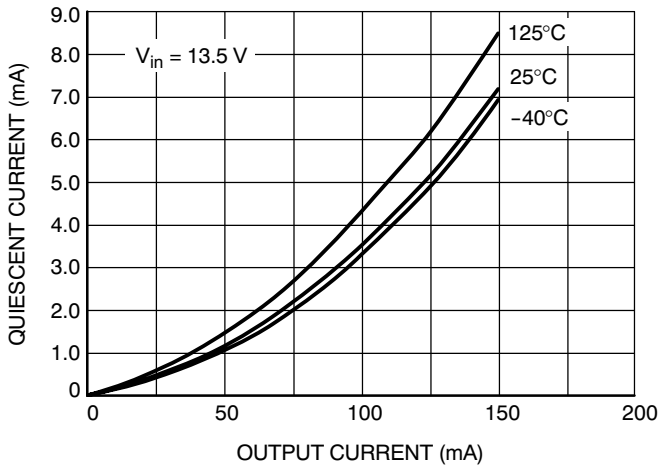


Figure 6. Current Consumption vs. Output Load, 5.0 V Version

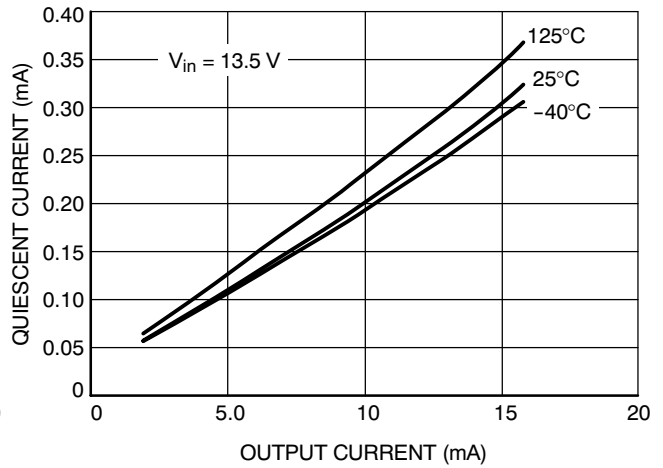


Figure 7. Current Consumption vs. Output Load (Low Load), 5.0 V Version

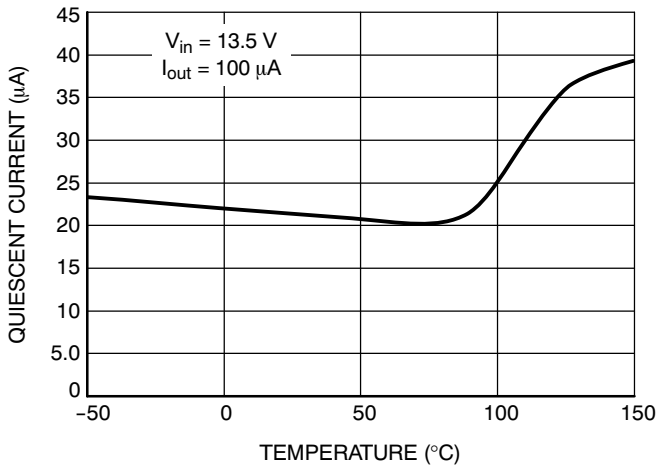


Figure 8. Quiescent Current vs. Temperature, 5.0 V Version

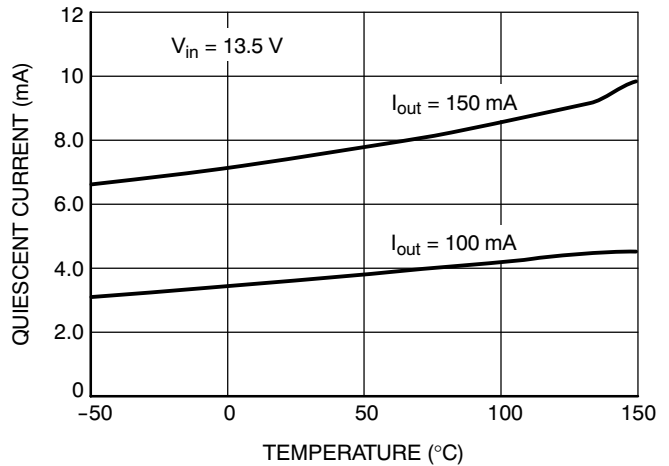


Figure 9. Quiescent Current vs. Temperature, 5.0 V Version

Typical Curves

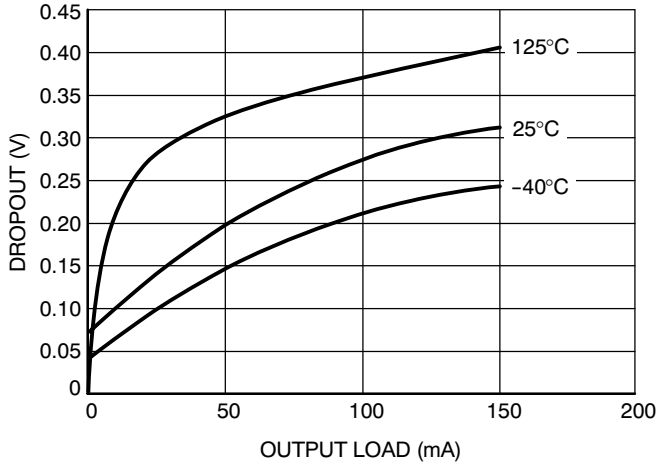


Figure 10. Dropout Voltage vs. Output Load, 5.0 V Version

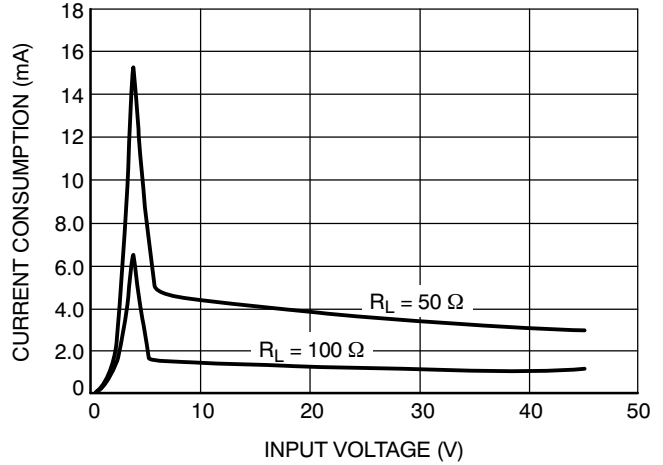


Figure 11. Current Consumption vs. Input Voltage, 5.0 V Version

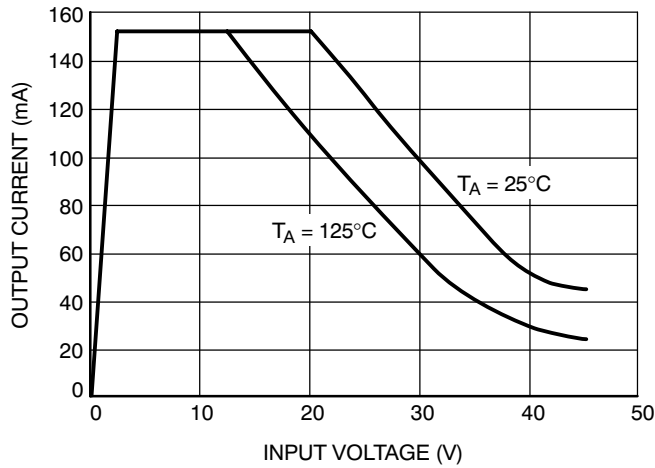


Figure 12. Output Current vs. Input Voltage, 5.0 V Version

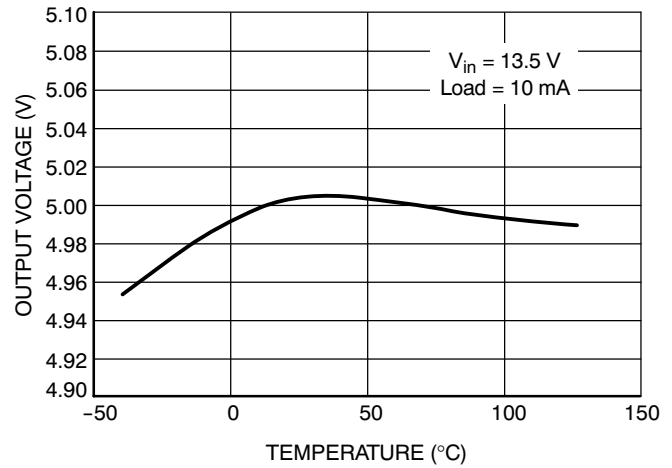


Figure 13. Output Voltage vs. Temperature, 5.0 V Version

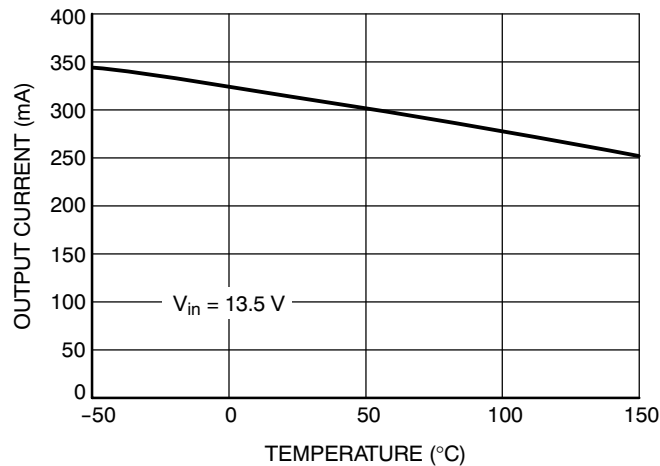


Figure 14. Current Limit vs. Temperature, 5.0 V Version

Typical Curves

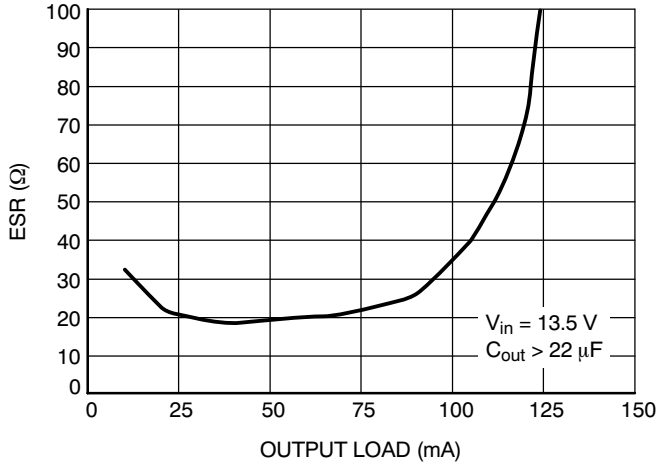


Figure 15. ESR Stability, 3.3 V Version

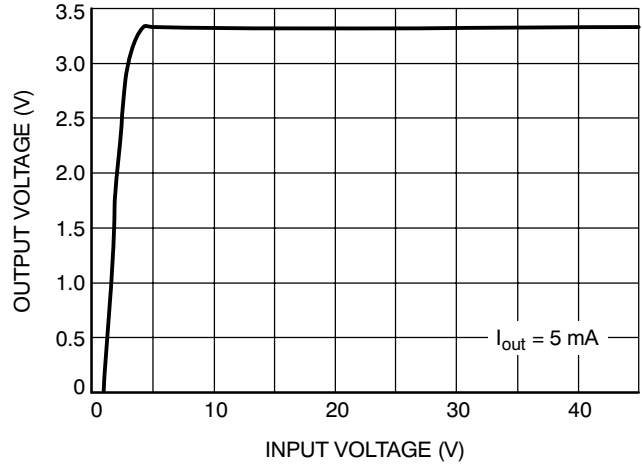


Figure 16. Output Voltage vs. Input Voltage, 3.3 V Version

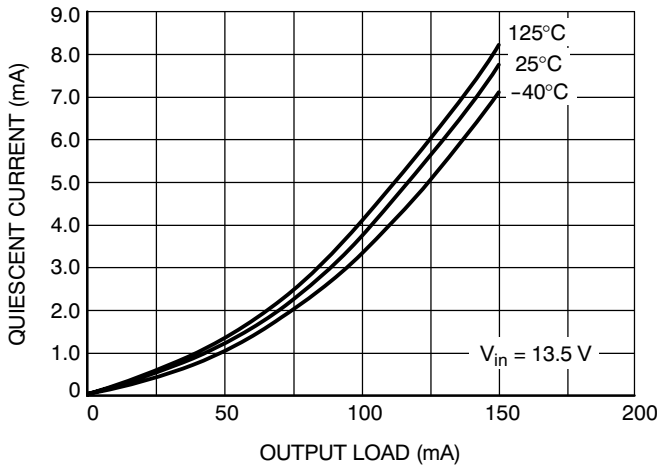


Figure 17. Current Consumption vs. Output Load, 3.3 V Version

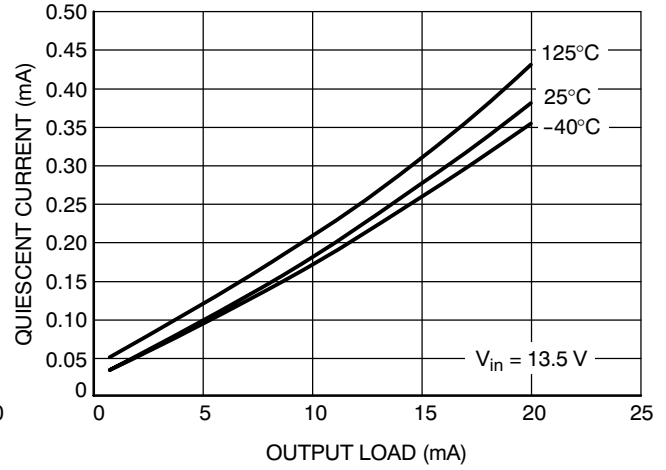


Figure 18. Current Consumption vs. Output Load (Low Load), 3.3 V Version

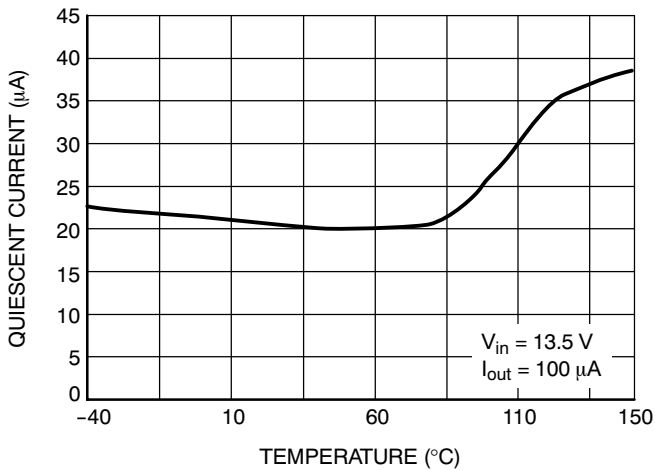


Figure 19. Quiescent Current vs. Temperature, 3.3 V Version

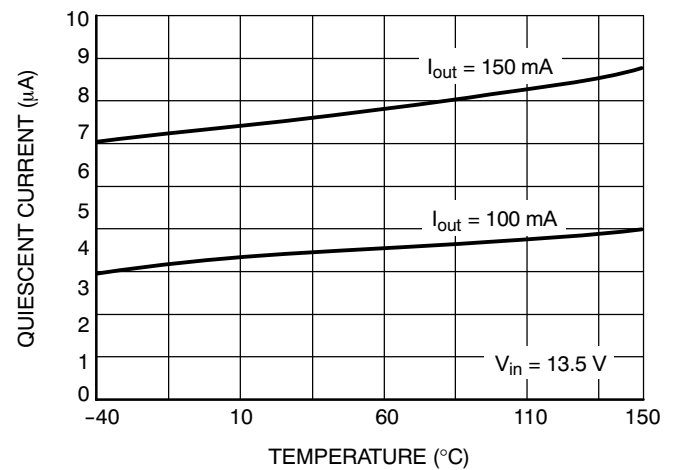


Figure 20. Quiescent Current vs. Temperature, 3.3 V Version

Typical Curves

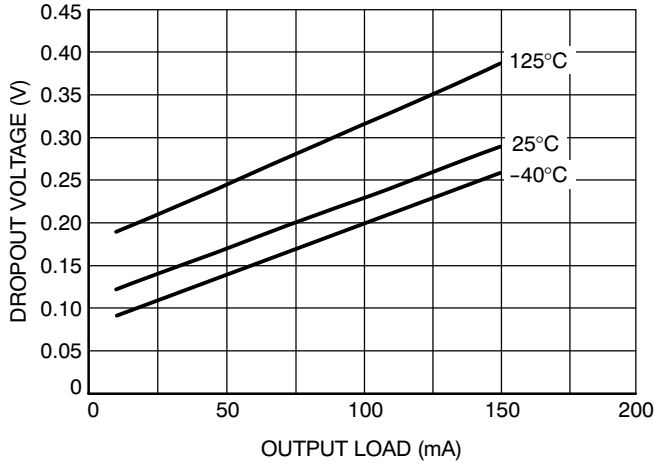


Figure 21. Dropout Voltage, 3.3 V Version

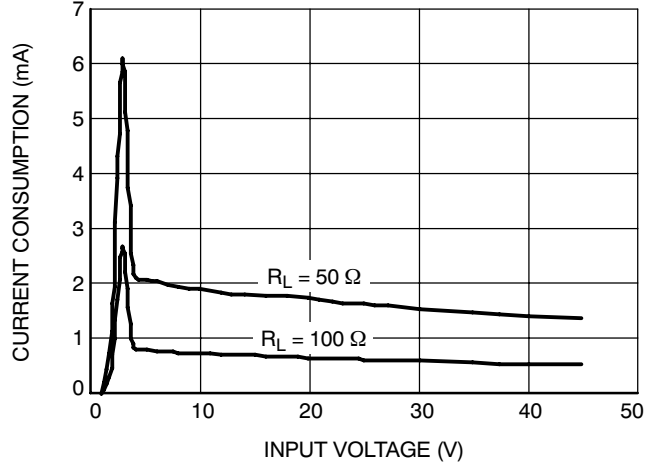


Figure 22. Current Consumption vs. Input Voltage, 3.3 V Version

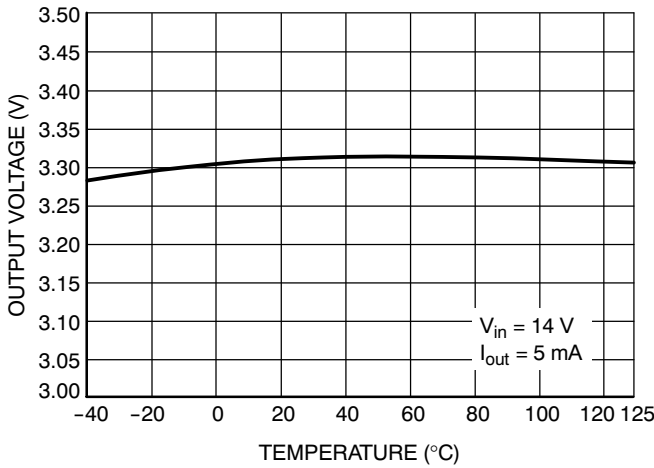


Figure 23. Output Voltage vs. Temperature, 3.3 V Version

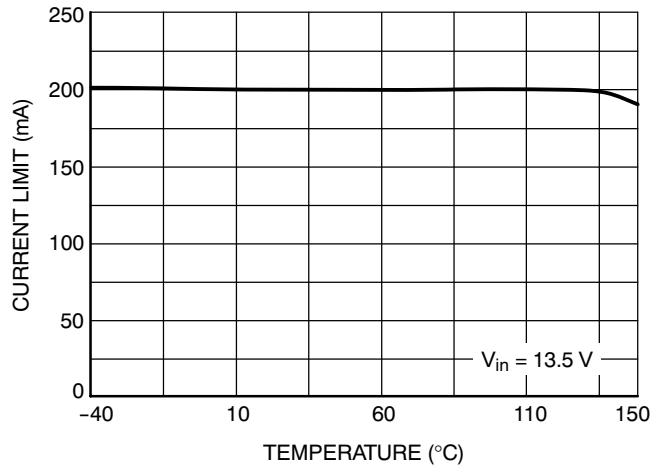


Figure 24. Short Circuit Current Limit vs. Temperature, 3.3 V Version

Circuit Description

The NCV8664 is a precision trimmed 3.3 V and 5.0 V fixed output regulator. Careful management of light load consumption combined with a low leakage process results in a typical quiescent current of 22 μA. The device has current capability of 150 mA, with 600 mV of dropout voltage at full rated load current. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference. The regulator is protected by both current limit and short circuit protection. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature-stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized. The NCV8664 is equipped with foldback current protection. This protection is designed to reduce the current limit during an overcurrent situation.

Regulator Stability Considerations

The input capacitor C_{IN} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{IN}. The output or compensation capacitor, C_{OUT} helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{OUT} shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values C_{OUT} ≥ 10 μF and ESR ≤ 9 Ω for 5.0 V version, and C_{OUT} ≥ 22 μF and ESR ≤ 18 Ω for 3.3 V version, within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}] \cdot I_{Q(max)} + V_{I(max)} \cdot I_q \quad (eq. 1)$$

Where:

V_{IN(max)} is the maximum input voltage,

V_{OUT(min)} is the minimum output voltage,

I_{Q(max)} is the maximum output current for the application, and I_q is the quiescent current the regulator consumes at I_{Q(max)}.

Once the value of P_{D(Max)} is known, the maximum permissible value of R_{θJA} can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}C - T_A}{P_D} \quad (eq. 2)$$

The value of R_{θJA} can then be compared with those in the package section of the data sheet. Those packages with R_{θJA}'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of R_{θJA}:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (eq. 3)$$

Where:

R_{θJC} = the junction-to-case thermal resistance,

R_{θCS} = the case-to-heat sink thermal resistance, and

R_{θSA} = the heat sink-to-ambient thermal resistance.

R_{θJA} appears in the package section of the data sheet.

Like R_{θJA}, it too is a function of package type. R_{θCS} and R_{θSA} are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.

NCV8664

EMC-Characteristics: Conducted Susceptibility

All EMC-Characteristics are based on limited samples and not part of production testing, according to 47A/658/CD IEC62132-4 (Direct Power Injection)

Direct Power Injection: 33 dBm forward power CW

Acceptance Criteria: Amplitude Dev. max 2% of Output Voltage

Test Conditions

Supply Voltage $V_{IN} = 12\text{ V}$
 Temperature $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$
 Load $R_L = 35\ \Omega$

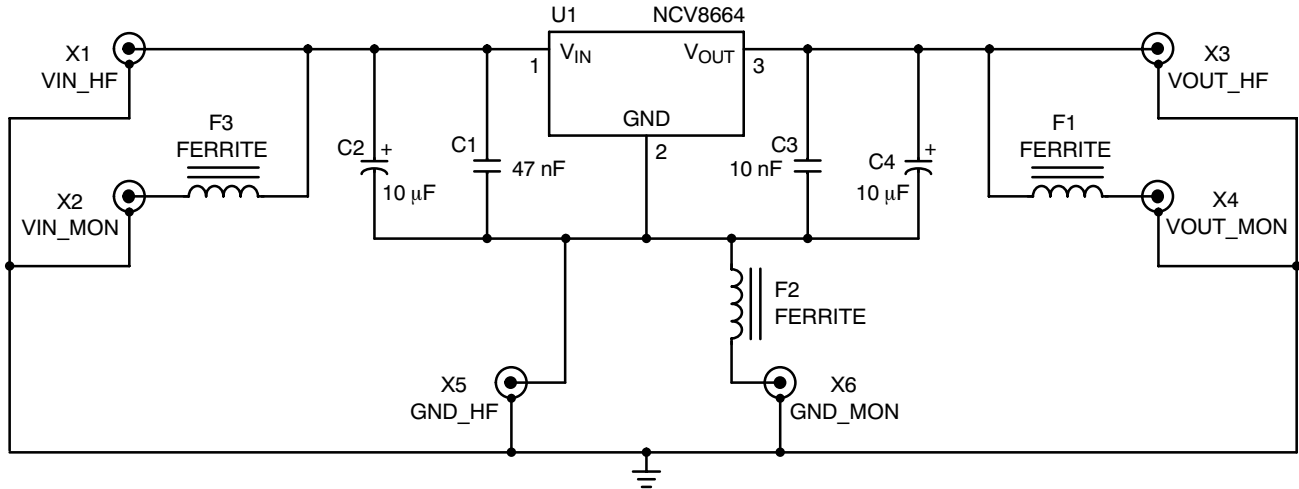


Figure 25. Test Circuit

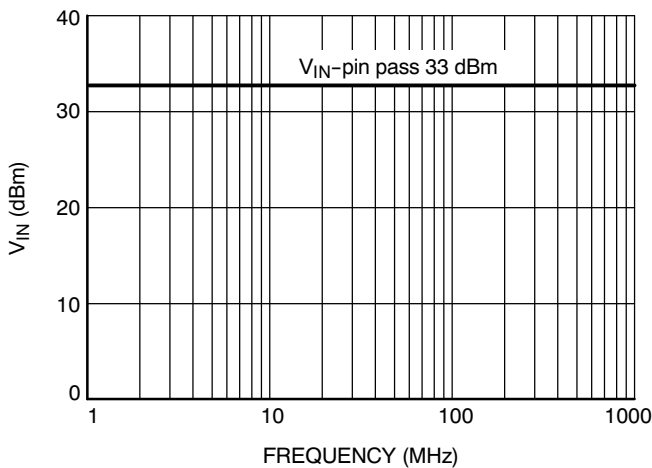


Figure 1. Typical V_{IN} -pin Susceptibility

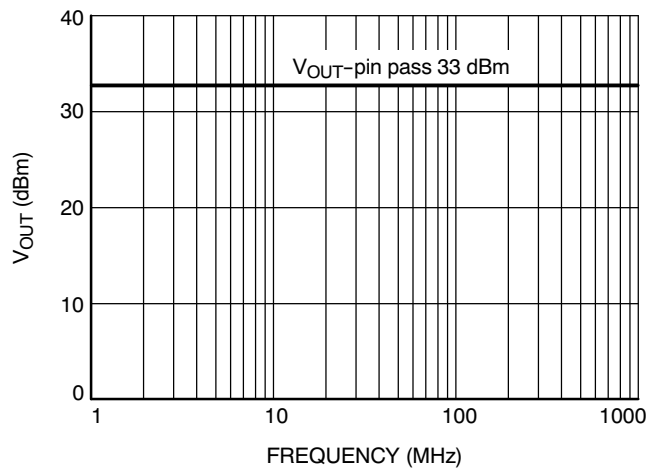


Figure 2. Typical V_{OUT} -pin Susceptibility

NCV8664

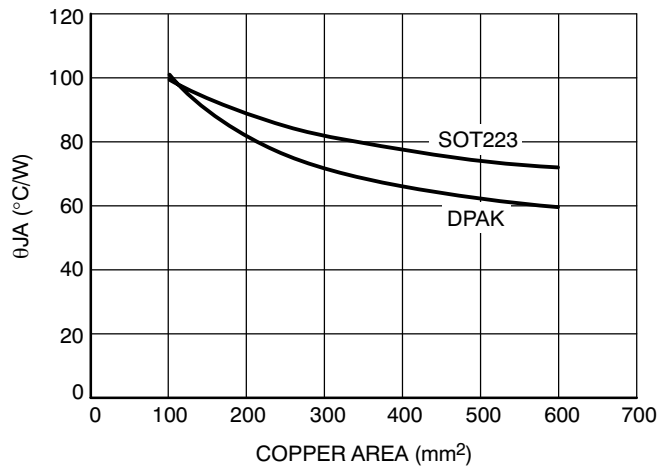


Figure 3. θ_{JA} vs. Copper Spreader Area

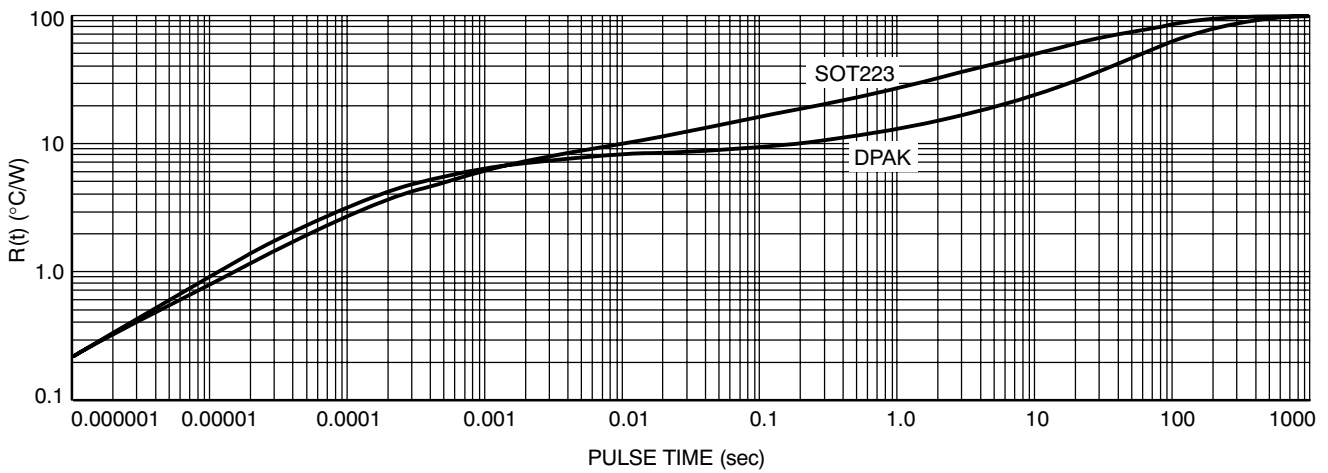


Figure 4. Single-Pulse Heating Curves

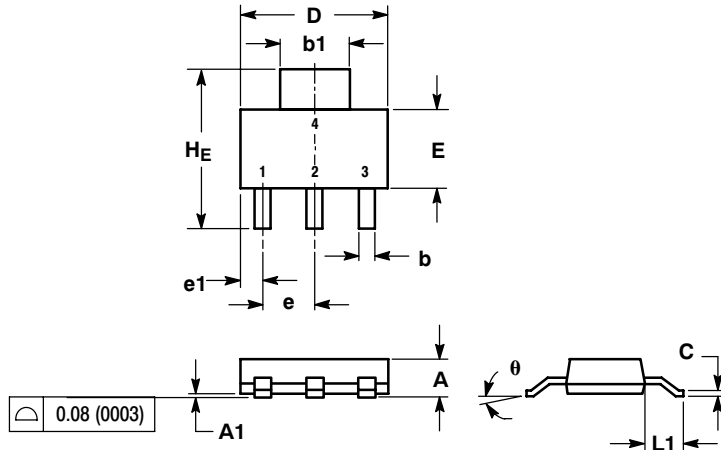
ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] |
|----------------|---------|---------|-----------------------|
| NCV8664DT50RKG | V66450G | DPAK | 2500/Tape & Reel |
| NCV8664DT33RKG | V66433G | DPAK | 2500/Tape & Reel |
| NCV8664ST50T3G | V6645 | SOT-223 | 4000/Tape & Reel |
| NCV8664ST33T3G | V6643 | SOT-223 | 4000/Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOT-223 (TO-261)
ST SUFFIX
CASE 318E-04
ISSUE L

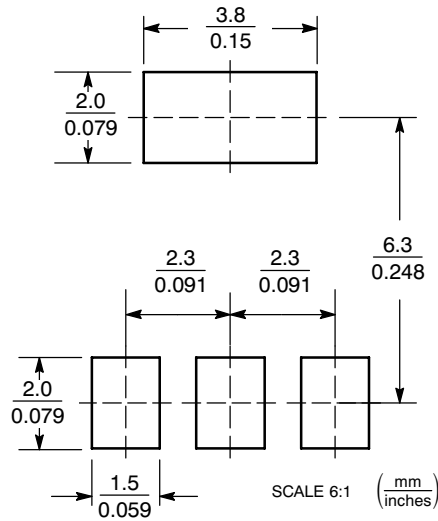


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|--------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.50 | 1.63 | 1.75 | 0.060 | 0.064 | 0.068 |
| A1 | 0.02 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.60 | 0.75 | 0.89 | 0.024 | 0.030 | 0.035 |
| b1 | 2.90 | 3.06 | 3.20 | 0.115 | 0.121 | 0.126 |
| c | 0.24 | 0.29 | 0.35 | 0.009 | 0.012 | 0.014 |
| D | 6.30 | 6.50 | 6.70 | 0.249 | 0.256 | 0.263 |
| E | 3.30 | 3.50 | 3.70 | 0.130 | 0.138 | 0.145 |
| e | 2.20 | 2.30 | 2.40 | 0.087 | 0.091 | 0.094 |
| e1 | 0.85 | 0.94 | 1.05 | 0.033 | 0.037 | 0.041 |
| L1 | 1.50 | 1.75 | 2.00 | 0.060 | 0.069 | 0.078 |
| HE | 6.70 | 7.00 | 7.30 | 0.264 | 0.276 | 0.287 |
| θ | 0° | - | 10° | 0° | - | 10° |

SOLDERING FOOTPRINT*

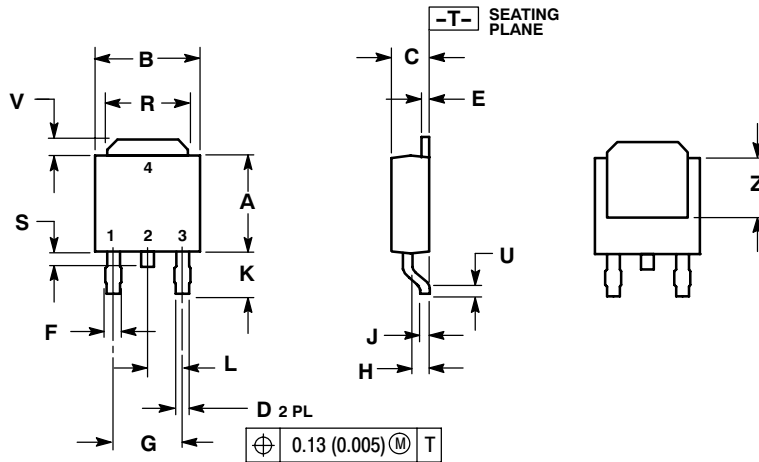


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCV8664

PACKAGE DIMENSIONS

DPAK (Single Gauge)
DT SUFFIX
CASE 369C
ISSUE O

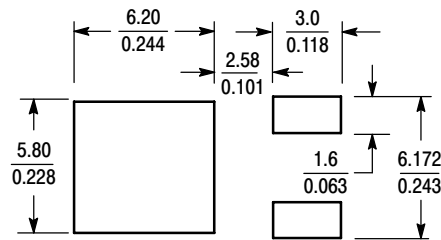


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.180 BSC | | 4.58 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.090 BSC | | 2.29 BSC | |
| R | 0.180 | 0.215 | 4.57 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| U | 0.020 | --- | 0.51 | --- |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

RECOMMENDED FOOTPRINT



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

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