SSD1298

Advance Information

240 RGB x 320 TFT LCD Controller Driver integrated Power Circuit, Gate and Source Driver with built-in RAM

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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1 GENERAL DESCRIPTION

SSD1298 is an all in one TFT LCD Controller Driver that integrated the RAM, power circuits, gate driver and source driver into a single chip. It can drive up to 262k color amorsphous TFT panel with resolution of 240 RGB x 320.

It also integrated the controller function and consists of 172,800 bytes (240 x 320 x 18 / 8) Graphic Display Data RAM (GDDRAM) such that it interfaced with common MPU through 8-/9-/16-/18-bit 6800-series / 8080-series compatible parallel interface or serial peripheral interface and stored the data in the GDDRAM. Auxiliary 18-/16-/6- bit video interface (VSYNC, HSYNC, DOTCLK, OE) are integrated into SSD1298 for animation image display.

SSD1298 embeds DC-DC Converter and Voltage generator to provide all necessary voltage required by the driver with minimum external components. A Common Voltage Generation Circuit is included to drive the TFT-display counter electrode. An Integrated Gamma Control Circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

SSD1298 can be operated down to 1.4V and provide different power save modes. It is suitable for any portable battery-driven applications requiring long operation period and compact size.

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2 FEATURES

- 240RGBx320 single chip controller driver IC for 262k color amorphous TFT LCD
- Power Supply
  - VDDIO = 1.4V – 3.6V (I/O Interface)
  - VCIR = 2.5V – 3.6V (Regulator power supply for logic circuit)
  - VCI = 2.5V – 3.6V (power supply for internal analog circuit)
- Output Voltages
  - Gate Driver:
    - VGH-GND = 9V ~ 18V
    - VGL-GND = -6 ~ -15V
    - VGH-VGL = 30Vp-p
  - Source Driver:
    - Maximum of VLCD63 = 6V
    - Typical Source Output Voltage variation: ±10 mV
  - VCOM drive:
    - VCOMH = 3.0V ~ 5.0V
    - VCOML = -1.0V ~ -3.0V
    - Maximum of VCOMA = 6V
- System Interface
  - 16-/18-bit RGB interface (OE, DOTCLK, HSYNC, VSYNC, DB[17:0]
  - High-speed interface by 8-/9-/16-/18-bit 6800-series / 8080-series parallel ports
  - Serial Peripheral Interface (SPI)
  - VSYNC interface (system interface + VSYNC)
  - WSYNC interface (system interface + WSYNC)
- Support low power consumption:
  - Low voltage supply
  - Low current sleep mode
  - 8-color display mode for power saving
  - Charge sharing function for step-up circuits
- High-speed RAM addressing functions
  - RAM write synchronization function
  - Window address function
  - Vertical scrolling function
  - Partial display mode
- Internal power supply circuit
  - Voltage generator
  - DC-DC converter up to 6x/-5x
- Built-in internal oscillator
- Internal GDDRAM capacity: 172800Byte
- Support Frame and Line inversion AC drive
- TFT storage capacitance: Cs on common
- Support source and gate scan direction control
- Programmable gamma correction curve
- Built-in Non Volatile Memory for VCOM calibration Display Size: 240 RGB x 320
- Support flexible arrangement of gate circuits on both sides of the glass substrate

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3 ORDERING INFORMATION

Table 3-1 – Ordering Information

Ordering Part Number	Source	Gate	Package Form	Reference
SSD1298Z	240 x 3 (720)	320	Gold Bump Die	

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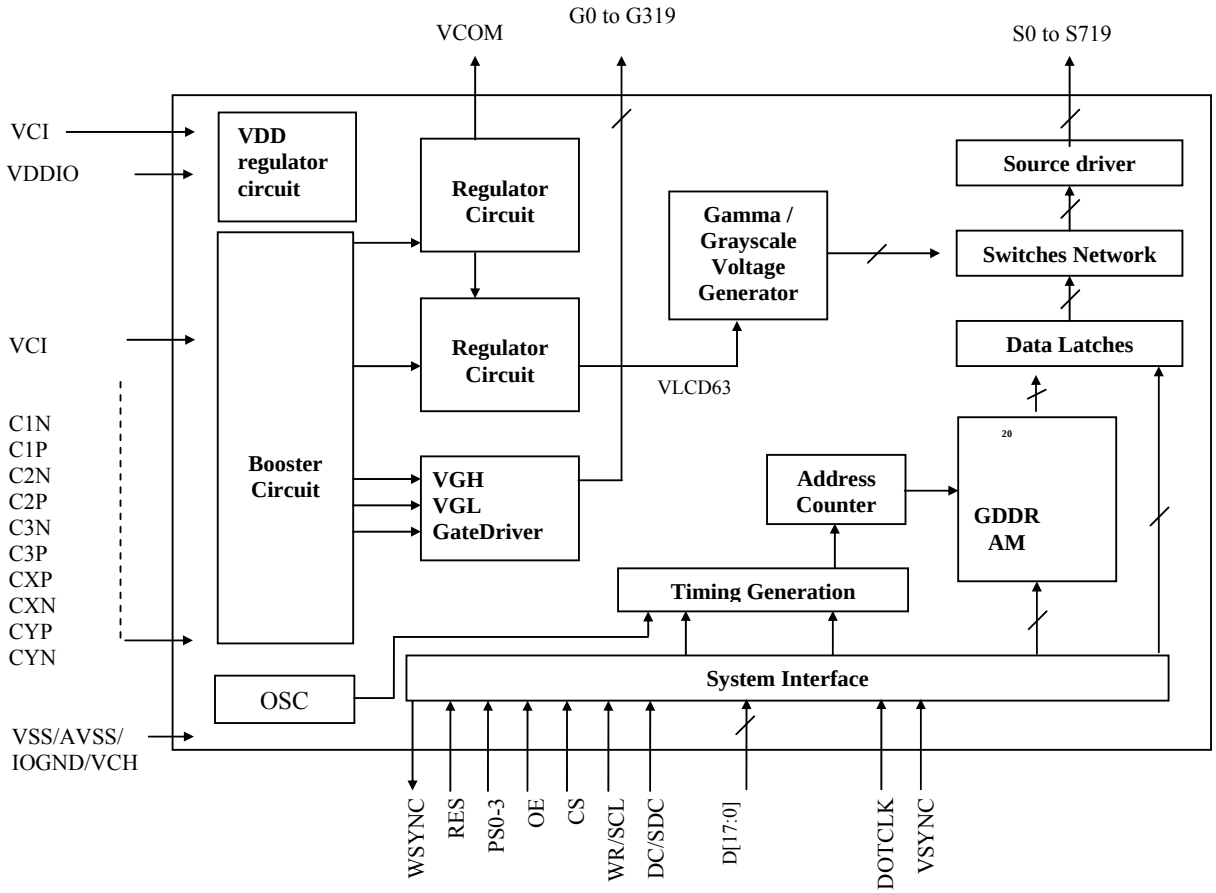
4 BLOCK DIAGRAM

Figure 4-1 - SSD1298 Block Diagram Description



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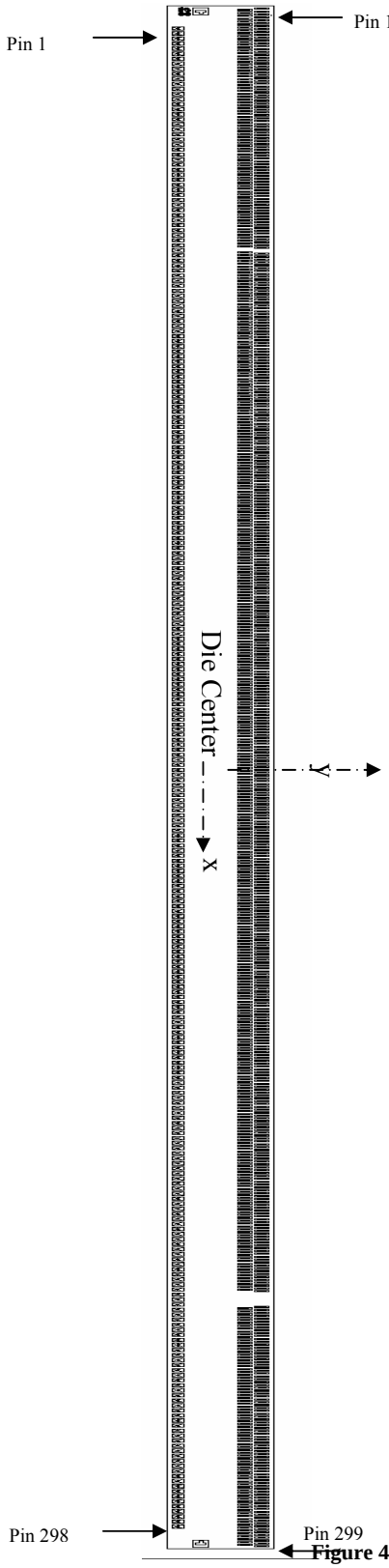
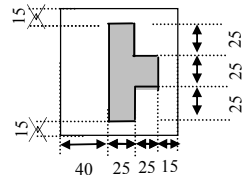
DIE PAD FLOOR PLAN



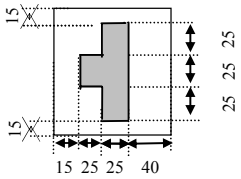
Note

(1) Diagram showing the die face up.
(2) Coordinates are referenced to center of the chip.
(3) Coordinate units and size of all alignment marks are in um.
(4) All alignment keys do not contain gold

Figure 4-3: Alignment Marks



Center: (-10633,-141.12)
Size: 105 x 105 μm²



Center: (10633,-141.12)
Size: 105 x 105 μm²

Figure 4-2: Output Pad Pitch (Pad 299 - 1354)

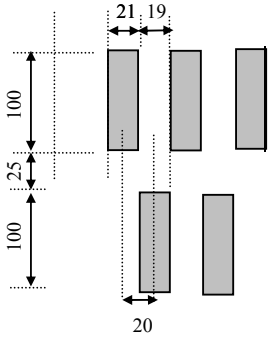


Table 4-1: Die Information

Die Size (no scribe)	21416 x 755 um²
Die Thickness	300 ± 25 um
Typical Bump Height	15 um
Bump Co-planarity (within die)	≤ 2 um
Bump Size 1	50 x 80 μm² (Pin 1 – 298)
Pad Pitch 1	70 μm
Bump Size 2	21 x 100 μm² (Pin 299 – 1354)
Pad Pitch 2	20 μm stagger

Figure 4-4 - SSD1298 Pad Arrangement (Bump face up)

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Table 4-2 - SSD1298 Bump Pad Coordinate (Bump Center)

Note: IC material temperature expansion factor is 2.6ppm, customer should take into account during panel design

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1	DUMMY	-10395.000	-305.620	51	D5	-6895.000	-305.620	101	VDDIO	-3395.000	-305.620
2	DUMMY	-10325.000	-305.620	52	D4	-6825.000	-305.620	102	VDDIO	-3325.000	-305.620
3	DUMMY	-10255.000	-305.620	53	D3	-6755.000	-305.620	103	VDDIO	-3255.000	-305.620
4	DUMMY	-10185.000	-305.620	54	D2	-6685.000	-305.620	104	VDDIO	-3185.000	-305.620
5	NC	-10115.000	-305.620	55	D1	-6615.000	-305.620	105	VCIR	-3115.000	-305.620
6	NC	-10045.000	-305.620	56	D0	-6545.000	-305.620	106	VCIR	-3045.000	-305.620
7	NC	-9975.000	-305.620	57	SDO	-6475.000	-305.620	107	VCIR	-2975.000	-305.620
8	VGH	-9905.000	-305.620	58	SDI	-6405.000	-305.620	108	VCIR	-2905.000	-305.620
9	VGH	-9835.000	-305.620	59	RD	-6335.000	-305.620	109	VCIR	-2835.000	-305.620
10	VGH	-9765.000	-305.620	60	WR	-6265.000	-305.620	110	VCIR	-2765.000	-305.620
11	VGH	-9695.000	-305.620	61	DC	-6195.000	-305.620	111	VCIR	-2695.000	-305.620
12	VGH	-9625.000	-305.620	62	CSB	-6125.000	-305.620	112	VCIR	-2625.000	-305.620
13	VSS	-9555.000	-305.620	63	NC	-6055.000	-305.620	113	VCORE	-2555.000	-305.620
14	VSS	-9485.000	-305.620	64	VDDIO	-5985.000	-305.620	114	VCORE	-2485.000	-305.620
15	VSS	-9415.000	-305.620	65	VDDIO	-5915.000	-305.620	115	VCORE	-2415.000	-305.620
16	DUMMY	-9345.000	-305.620	66	WSYNC	-5845.000	-305.620	116	VCORE	-2345.000	-305.620
17	DUMMY	-9275.000	-305.620	67	NC	-5775.000	-305.620	117	VCORE	-2275.000	-305.620
18	DUMMY	-9205.000	-305.620	68	NC	-5705.000	-305.620	118	VCORE	-2205.000	-305.620
19	DUMMY	-9135.000	-305.620	69	NC	-5635.000	-305.620	119	VCORE	-2135.000	-305.620
20	NC	-9065.000	-305.620	70	NC	-5565.000	-305.620	120	VCORE	-2065.000	-305.620
21	NC	-8995.000	-305.620	71	NC	-5495.000	-305.620	121	VCORE	-1995.000	-305.620
22	NC	-8925.000	-305.620	72	NC	-5425.000	-305.620	122	VREGC	-1925.000	-305.620
23	NC	-8855.000	-305.620	73	NC	-5355.000	-305.620	123	VREGC	-1855.000	-305.620
24	PS0	-8785.000	-305.620	74	NC	-5285.000	-305.620	124	VREGC	-1785.000	-305.620
25	PS1	-8715.000	-305.620	75	NC	-5215.000	-305.620	125	VREGC	-1715.000	-305.620
26	PS2	-8645.000	-305.620	76	DUMMY	-5145.000	-305.620	126	DUMMY	-1645.000	-305.620
27	PS3	-8575.000	-305.620	77	DUMMY	-5075.000	-305.620	127	DUMMY	-1575.000	-305.620
28	DUMMY	-8505.000	-305.620	78	NC	-5005.000	-305.620	128	DUMMY	-1505.000	-305.620
29	VDDIO	-8435.000	-305.620	79	NC	-4935.000	-305.620	129	DUMMY	-1435.000	-305.620
30	DUMMY	-8365.000	-305.620	80	NC	-4865.000	-305.620	130	DUMMY	-1365.000	-305.620
31	RESB	-8295.000	-305.620	81	DUMMY	-4795.000	-305.620	131	DUMMY	-1295.000	-305.620
32	VSYNC	-8225.000	-305.620	82	TESTA	-4725.000	-305.620	132	DUMMY	-1225.000	-305.620
33	HSYNC	-8155.000	-305.620	83	TESTB	-4655.000	-305.620	133	DUMMY	-1155.000	-305.620
34	DOTCLK	-8085.000	-305.620	84	TESTC	-4585.000	-305.620	134	VCHS	-1085.000	-305.620
35	OE	-8015.000	-305.620	85	NC	-4515.000	-305.620	135	VCHS	-1015.000	-305.620
36	D17	-7945.000	-305.620	86	DUMMY	-4445.000	-305.620	136	VCHS	-945.000	-305.620
37	D16	-7875.000	-305.620	87	NC	-4375.000	-305.620	137	VCHS	-875.000	-305.620
38	D15	-7805.000	-305.620	88	NC	-4305.000	-305.620	138	VCHS	-805.000	-305.620
39	D14	-7735.000	-305.620	89	NC	-4235.000	-305.620	139	VCHS	-735.000	-305.620
40	D13	-7665.000	-305.620	90	NC	-4165.000	-305.620	140	VCHS	-665.000	-305.620
41	D12	-7595.000	-305.620	91	IOGND	-4095.000	-305.620	141	VCHS	-595.000	-305.620
42	D11	-7525.000	-305.620	92	IOGND	-4025.000	-305.620	142	VCHS	-525.000	-305.620
43	D10	-7455.000	-305.620	93	IOGND	-3955.000	-305.620	143	VCHS	-455.000	-305.620
44	D9	-7385.000	-305.620	94	IOGND	-3885.000	-305.620	144	VCHS	-385.000	-305.620
45	D8	-7315.000	-305.620	95	IOGND	-3815.000	-305.620	145	AVSS	-315.000	-305.620
46	DUMMY	-7245.000	-305.620	96	IOGND	-3745.000	-305.620	146	AVSS	-245.000	-305.620
47	VSS	-7175.000	-305.620	97	IOGND	-3675.000	-305.620	147	AVSS	-175.000	-305.620
48	NC	-7105.000	-305.620	98	VDDIO	-3605.000	-305.620	148	AVSS	-105.000	-305.620
49	D7	-7035.000	-305.620	99	VDDIO	-3535.000	-305.620	149	AVSS	-35.000	-305.620
50	D6	-6965.000	-305.620	100	VDDIO	-3465.000	-305.620	150	AVSS	35.000	-305.620

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Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
151	VSS	105.000	-305.620	201	VCIX2G	3605.000	-305.620	251	VGL	7105.000	-305.620
152	VSS	175.000	-305.620	202	VCIX2G	3675.000	-305.620	252	VGL	7175.000	-305.620
153	VSS	245.000	-305.620	203	VCIX2	3745.000	-305.620	253	VGL	7245.000	-305.620
154	VSS	315.000	-305.620	204	VCIX2	3815.000	-305.620	254	VGL	7315.000	-305.620
155	VSS	385.000	-305.620	205	VCIX2	3885.000	-305.620	255	VGL	7385.000	-305.620
156	VSS	455.000	-305.620	206	VCIX2	3955.000	-305.620	256	VGL	7455.000	-305.620
157	VSS	525.000	-305.620	207	VCIX2	4025.000	-305.620	257	VGL	7525.000	-305.620
158	VSS	595.000	-305.620	208	VCIX2	4095.000	-305.620	258	VGL	7595.000	-305.620
159	VSS	665.000	-305.620	209	VCIX2	4165.000	-305.620	259	VGL	7665.000	-305.620
160	VSS	735.000	-305.620	210	VCI	4235.000	-305.620	260	DUMMY	7735.000	-305.620
161	DUMMY	805.000	-305.620	211	VCI	4305.000	-305.620	261	DUMMY	7805.000	-305.620
162	DUMMY	875.000	-305.620	212	VCI	4375.000	-305.620	262	DUMMY	7875.000	-305.620
163	DUMMY	945.000	-305.620	213	VCI	4445.000	-305.620	263	VGH	7945.000	-305.620
164	EXVR	1015.000	-305.620	214	VCI	4515.000	-305.620	264	VGH	8015.000	-305.620
165	DUMMY	1085.000	-305.620	215	VCI	4585.000	-305.620	265	VGH	8085.000	-305.620
166	DUMMY	1155.000	-305.620	216	VCI	4655.000	-305.620	266	VGH	8155.000	-305.620
167	DUMMY	1225.000	-305.620	217	VCI	4725.000	-305.620	267	VGH	8225.000	-305.620
168	DUMMY	1295.000	-305.620	218	VCIP	4795.000	-305.620	268	VGH	8295.000	-305.620
169	DUMMY	1365.000	-305.620	219	VCI	4865.000	-305.620	269	DUMMY	8365.000	-305.620
170	DUMMY	1435.000	-305.620	220	VCI	4935.000	-305.620	270	C3N	8435.000	-305.620
171	VCOM	1505.000	-305.620	221	VCI	5005.000	-305.620	271	C3N	8505.000	-305.620
172	VCOM	1575.000	-305.620	222	VCI	5075.000	-305.620	272	C3N	8575.000	-305.620
173	VCOM	1645.000	-305.620	223	VCI	5145.000	-305.620	273	DUMMY	8645.000	-305.620
174	VCOM	1715.000	-305.620	224	VCI	5215.000	-305.620	274	C3P	8715.000	-305.620
175	VCOM	1785.000	-305.620	225	VCI	5285.000	-305.620	275	C3P	8785.000	-305.620
176	VCOM	1855.000	-305.620	226	VCI	5355.000	-305.620	276	C3P	8855.000	-305.620
177	VCOMH	1925.000	-305.620	227	CYN	5425.000	-305.620	277	DUMMY	8925.000	-305.620
178	VCOMH	1995.000	-305.620	228	CYN	5495.000	-305.620	278	C1N	8995.000	-305.620
179	VCOMH	2065.000	-305.620	229	CYN	5565.000	-305.620	279	C1N	9065.000	-305.620
180	VCOMH	2135.000	-305.620	230	CYN	5635.000	-305.620	280	C1N	9135.000	-305.620
181	VCOMH	2205.000	-305.620	231	CYN	5705.000	-305.620	281	C1P	9205.000	-305.620
182	VCOMH	2275.000	-305.620	232	CYP	5775.000	-305.620	282	C1P	9275.000	-305.620
183	VCOML	2345.000	-305.620	233	CYP	5845.000	-305.620	283	C1P	9345.000	-305.620
184	VCOML	2415.000	-305.620	234	CYP	5915.000	-305.620	284	C2N	9415.000	-305.620
185	VCOML	2485.000	-305.620	235	CYP	5985.000	-305.620	285	C2N	9485.000	-305.620
186	VCOML	2555.000	-305.620	236	CYP	6055.000	-305.620	286	C2N	9555.000	-305.620
187	VCOML	2625.000	-305.620	237	CXN	6125.000	-305.620	287	C2P	9625.000	-305.620
188	VCOML	2695.000	-305.620	238	CXN	6195.000	-305.620	288	C2P	9695.000	-305.620
189	DUMMY	2765.000	-305.620	239	CXN	6265.000	-305.620	289	C2P	9765.000	-305.620
190	DUMMY	2835.000	-305.620	240	CXN	6335.000	-305.620	290	CDUM1N	9835.000	-305.620
191	VLCD63	2905.000	-305.620	241	CXN	6405.000	-305.620	291	CDUM1N	9905.000	-305.620
192	DUMMY	2975.000	-305.620	242	CXP	6475.000	-305.620	292	CDUM1N	9975.000	-305.620
193	DUMMY	3045.000	-305.620	243	CXP	6545.000	-305.620	293	CDUM1P	10045.000	-305.620
194	DUMMY	3115.000	-305.620	244	CXP	6615.000	-305.620	294	CDUM1P	10115.000	-305.620
195	VCOMR	3185.000	-305.620	245	CXP	6685.000	-305.620	295	CDUM1P	10185.000	-305.620
196	DUMMY	3255.000	-305.620	246	CXP	6755.000	-305.620	296	DUMMY	10255.000	-305.620
197	VCIM	3325.000	-305.620	247	DUMMY	6825.000	-305.620	297	DUMMY	10325.000	-305.620
198	VCIM	3395.000	-305.620	248	VGL	6895.000	-305.620	298	DUMMY	10395.000	-305.620
199	VCIM	3465.000	-305.620	249	VGL	6965.000	-305.620	299	DUMMY	10670.000	293.380
200	VCIX2G	3535.000	-305.620	250	VGL	7035.000	-305.620	300	DUMMY	10650.000	168.380

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Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
301	DUMMY	10630.000	293.380	351	G95	9630.000	293.380	401	G195	8630.000	293.380
302	DUMMY	10610.000	168.380	352	G97	9610.000	168.380	402	G197	8610.000	168.380
303	DUMMY	10590.000	293.380	353	G99	9590.000	293.380	403	G199	8590.000	293.380
304	G1	10570.000	168.380	354	G101	9570.000	168.380	404	G201	8570.000	168.380
305	G3	10550.000	293.380	355	G103	9550.000	293.380	405	G203	8550.000	293.380
306	G5	10530.000	168.380	356	G105	9530.000	168.380	406	G205	8530.000	168.380
307	G7	10510.000	293.380	357	G107	9510.000	293.380	407	G207	8510.000	293.380
308	G9	10490.000	168.380	358	G109	9490.000	168.380	408	G209	8490.000	168.380
309	G11	10470.000	293.380	359	G111	9470.000	293.380	409	G211	8470.000	293.380
310	G13	10450.000	168.380	360	G113	9450.000	168.380	410	G213	8450.000	168.380
311	G15	10430.000	293.380	361	G115	9430.000	293.380	411	G215	8430.000	293.380
312	G17	10410.000	168.380	362	G117	9410.000	168.380	412	G217	8410.000	168.380
313	G19	10390.000	293.380	363	G119	9390.000	293.380	413	G219	8390.000	293.380
314	G21	10370.000	168.380	364	G121	9370.000	168.380	414	G221	8370.000	168.380
315	G23	10350.000	293.380	365	G123	9350.000	293.380	415	G223	8350.000	293.380
316	G25	10330.000	168.380	366	G125	9330.000	168.380	416	G225	8330.000	168.380
317	G27	10310.000	293.380	367	G127	9310.000	293.380	417	G227	8310.000	293.380
318	G29	10290.000	168.380	368	G129	9290.000	168.380	418	G229	8290.000	168.380
319	G31	10270.000	293.380	369	G131	9270.000	293.380	419	G231	8270.000	293.380
320	G33	10250.000	168.380	370	G133	9250.000	168.380	420	G233	8250.000	168.380
321	G35	10230.000	293.380	371	G135	9230.000	293.380	421	G235	8230.000	293.380
322	G37	10210.000	168.380	372	G137	9210.000	168.380	422	G237	8210.000	168.380
323	G39	10190.000	293.380	373	G139	9190.000	293.380	423	G239	8190.000	293.380
324	G41	10170.000	168.380	374	G141	9170.000	168.380	424	G241	8170.000	168.380
325	G43	10150.000	293.380	375	G143	9150.000	293.380	425	G243	8150.000	293.380
326	G45	10130.000	168.380	376	G145	9130.000	168.380	426	G245	8130.000	168.380
327	G47	10110.000	293.380	377	G147	9110.000	293.380	427	G247	8110.000	293.380
328	G49	10090.000	168.380	378	G149	9090.000	168.380	428	G249	8090.000	168.380
329	G51	10070.000	293.380	379	G151	9070.000	293.380	429	G251	8070.000	293.380
330	G53	10050.000	168.380	380	G153	9050.000	168.380	430	G253	8050.000	168.380
331	G55	10030.000	293.380	381	G155	9030.000	293.380	431	G255	8030.000	293.380
332	G57	10010.000	168.380	382	G157	9010.000	168.380	432	G257	8010.000	168.380
333	G59	9990.000	293.380	383	G159	8990.000	293.380	433	G259	7990.000	293.380
334	G61	9970.000	168.380	384	G161	8970.000	168.380	434	G261	7970.000	168.380
335	G63	9950.000	293.380	385	G163	8950.000	293.380	435	G263	7950.000	293.380
336	G65	9930.000	168.380	386	G165	8930.000	168.380	436	G265	7930.000	168.380
337	G67	9910.000	293.380	387	G167	8910.000	293.380	437	G267	7910.000	293.380
338	G69	9890.000	168.380	388	G169	8890.000	168.380	438	G269	7890.000	168.380
339	G71	9870.000	293.380	389	G171	8870.000	293.380	439	G271	7870.000	293.380
340	G73	9850.000	168.380	390	G173	8850.000	168.380	440	G273	7850.000	168.380
341	G75	9830.000	293.380	391	G175	8830.000	293.380	441	G275	7830.000	293.380
342	G77	9810.000	168.380	392	G177	8810.000	168.380	442	G277	7810.000	168.380
343	G79	9790.000	293.380	393	G179	8790.000	293.380	443	G279	7790.000	293.380
344	G81	9770.000	168.380	394	G181	8770.000	168.380	444	G281	7770.000	168.380
345	G83	9750.000	293.380	395	G183	8750.000	293.380	445	G283	7750.000	293.380
346	G85	9730.000	168.380	396	G185	8730.000	168.380	446	G285	7730.000	168.380
347	G87	9710.000	293.380	397	G187	8710.000	293.380	447	G287	7710.000	293.380
348	G89	9690.000	168.380	398	G189	8690.000	168.380	448	G289	7690.000	168.380
349	G91	9670.000	293.380	399	G191	8670.000	293.380	449	G291	7670.000	293.380
350	G93	9650.000	168.380	400	G193	8650.000	168.380	450	G293	7650.000	168.380

Downloaded from Elcodis.com electronic components distributor

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
451	G295	7630.000	293.380	501	S685	6430.000	168.380	551	S635	5430.000	168.380
452	G297	7610.000	168.380	502	S684	6410.000	293.380	552	S634	5410.000	293.380
453	G299	7590.000	293.380	503	S683	6390.000	168.380	553	S633	5390.000	168.380
454	G301	7570.000	168.380	504	S682	6370.000	293.380	554	S632	5370.000	293.380
455	G303	7550.000	293.380	505	S681	6350.000	168.380	555	S631	5350.000	168.380
456	G305	7530.000	168.380	506	S680	6330.000	293.380	556	S630	5330.000	293.380
457	G307	7510.000	293.380	507	S679	6310.000	168.380	557	S629	5310.000	168.380
458	G309	7490.000	168.380	508	S678	6290.000	293.380	558	S628	5290.000	293.380
459	G311	7470.000	293.380	509	S677	6270.000	168.380	559	S627	5270.000	168.380
460	G313	7450.000	168.380	510	S676	6250.000	293.380	560	S626	5250.000	293.380
461	G315	7430.000	293.380	511	S675	6230.000	168.380	561	S625	5230.000	168.380
462	G317	7410.000	168.380	512	S674	6210.000	293.380	562	S624	5210.000	293.380
463	G319	7390.000	293.380	513	S673	6190.000	168.380	563	S623	5190.000	168.380
464	DUMMY	7370.000	168.380	514	S672	6170.000	293.380	564	S622	5170.000	293.380
465	DUMMY	7350.000	293.380	515	S671	6150.000	168.380	565	S621	5150.000	168.380
466	DUMMY	7130.000	293.380	516	S670	6130.000	293.380	566	S620	5130.000	293.380
467	S719	7110.000	168.380	517	S669	6110.000	168.380	567	S619	5110.000	168.380
468	S718	7090.000	293.380	518	S668	6090.000	293.380	568	S618	5090.000	293.380
469	S717	7070.000	168.380	519	S667	6070.000	168.380	569	S617	5070.000	168.380
470	S716	7050.000	293.380	520	S666	6050.000	293.380	570	S616	5050.000	293.380
471	S715	7030.000	168.380	521	S665	6030.000	168.380	571	S615	5030.000	168.380
472	S714	7010.000	293.380	522	S664	6010.000	293.380	572	S614	5010.000	293.380
473	S713	6990.000	168.380	523	S663	5990.000	168.380	573	S613	4990.000	168.380
474	S712	6970.000	293.380	524	S662	5970.000	293.380	574	S612	4970.000	293.380
475	S711	6950.000	168.380	525	S661	5950.000	168.380	575	S611	4950.000	168.380
476	S710	6930.000	293.380	526	S660	5930.000	293.380	576	S610	4930.000	293.380
477	S709	6910.000	168.380	527	S659	5910.000	168.380	577	S609	4910.000	168.380
478	S708	6890.000	293.380	528	S658	5890.000	293.380	578	S608	4890.000	293.380
479	S707	6870.000	168.380	529	S657	5870.000	168.380	579	S607	4870.000	168.380
480	S706	6850.000	293.380	530	S656	5850.000	293.380	580	S606	4850.000	293.380
481	S705	6830.000	168.380	531	S655	5830.000	168.380	581	S605	4830.000	168.380
482	S704	6810.000	293.380	532	S654	5810.000	293.380	582	S604	4810.000	293.380
483	S703	6790.000	168.380	533	S653	5790.000	168.380	583	S603	4790.000	168.380
484	S702	6770.000	293.380	534	S652	5770.000	293.380	584	S602	4770.000	293.380
485	S701	6750.000	168.380	535	S651	5750.000	168.380	585	S601	4750.000	168.380
486	S700	6730.000	293.380	536	S650	5730.000	293.380	586	S600	4730.000	293.380
487	S699	6710.000	168.380	537	S649	5710.000	168.380	587	S599	4710.000	168.380
488	S698	6690.000	293.380	538	S648	5690.000	293.380	588	S598	4690.000	293.380
489	S697	6670.000	168.380	539	S647	5670.000	168.380	589	S597	4670.000	168.380
490	S696	6650.000	293.380	540	S646	5650.000	293.380	590	S596	4650.000	293.380
491	S695	6630.000	168.380	541	S645	5630.000	168.380	591	S595	4630.000	168.380
492	S694	6610.000	293.380	542	S644	5610.000	293.380	592	S594	4610.000	293.380
493	S693	6590.000	168.380	543	S643	5590.000	168.380	593	S593	4590.000	168.380
494	S692	6570.000	293.380	544	S642	5570.000	293.380	594	S592	4570.000	293.380
495	S691	6550.000	168.380	545	S641	5550.000	168.380	595	S591	4550.000	168.380
496	S690	6530.000	293.380	546	S640	5530.000	293.380	596	S590	4530.000	293.380
497	S689	6510.000	168.380	547	S639	5510.000	168.380	597	S589	4510.000	168.380
498	S688	6490.000	293.380	548	S638	5490.000	293.380	598	S588	4490.000	293.380
499	S687	6470.000	168.380	549	S637	5470.000	168.380	599	S587	4470.000	168.380
500	S686	6450.000	293.380	550	S636	5450.000	293.380	600	S586	4450.000	293.380

Downloaded from Elcodis.com electronic components distributor

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
601	S585	4430.000	168.380	651	S535	3430.000	168.380	701	S485	2430.000	168.380
602	S584	4410.000	293.380	652	S534	3410.000	293.380	702	S484	2410.000	293.380
603	S583	4390.000	168.380	653	S533	3390.000	168.380	703	S483	2390.000	168.380
604	S582	4370.000	293.380	654	S532	3370.000	293.380	704	S482	2370.000	293.380
605	S581	4350.000	168.380	655	S531	3350.000	168.380	705	S481	2350.000	168.380
606	S580	4330.000	293.380	656	S530	3330.000	293.380	706	S480	2330.000	293.380
607	S579	4310.000	168.380	657	S529	3310.000	168.380	707	S479	2310.000	168.380
608	S578	4290.000	293.380	658	S528	3290.000	293.380	708	S478	2290.000	293.380
609	S577	4270.000	168.380	659	S527	3270.000	168.380	709	S477	2270.000	168.380
610	S576	4250.000	293.380	660	S526	3250.000	293.380	710	S476	2250.000	293.380
611	S575	4230.000	168.380	661	S525	3230.000	168.380	711	S475	2230.000	168.380
612	S574	4210.000	293.380	662	S524	3210.000	293.380	712	S474	2210.000	293.380
613	S573	4190.000	168.380	663	S523	3190.000	168.380	713	S473	2190.000	168.380
614	S572	4170.000	293.380	664	S522	3170.000	293.380	714	S472	2170.000	293.380
615	S571	4150.000	168.380	665	S521	3150.000	168.380	715	S471	2150.000	168.380
616	S570	4130.000	293.380	666	S520	3130.000	293.380	716	S470	2130.000	293.380
617	S569	4110.000	168.380	667	S519	3110.000	168.380	717	S469	2110.000	168.380
618	S568	4090.000	293.380	668	S518	3090.000	293.380	718	S468	2090.000	293.380
619	S567	4070.000	168.380	669	S517	3070.000	168.380	719	S467	2070.000	168.380
620	S566	4050.000	293.380	670	S516	3050.000	293.380	720	S466	2050.000	293.380
621	S565	4030.000	168.380	671	S515	3030.000	168.380	721	S465	2030.000	168.380
622	S564	4010.000	293.380	672	S514	3010.000	293.380	722	S464	2010.000	293.380
623	S563	3990.000	168.380	673	S513	2990.000	168.380	723	S463	1990.000	168.380
624	S562	3970.000	293.380	674	S512	2970.000	293.380	724	S462	1970.000	293.380
625	S561	3950.000	168.380	675	S511	2950.000	168.380	725	S461	1950.000	168.380
626	S560	3930.000	293.380	676	S510	2930.000	293.380	726	S460	1930.000	293.380
627	S559	3910.000	168.380	677	S509	2910.000	168.380	727	S459	1910.000	168.380
628	S558	3890.000	293.380	678	S508	2890.000	293.380	728	S458	1890.000	293.380
629	S557	3870.000	168.380	679	S507	2870.000	168.380	729	S457	1870.000	168.380
630	S556	3850.000	293.380	680	S506	2850.000	293.380	730	S456	1850.000	293.380
631	S555	3830.000	168.380	681	S505	2830.000	168.380	731	S455	1830.000	168.380
632	S554	3810.000	293.380	682	S504	2810.000	293.380	732	S454	1810.000	293.380
633	S553	3790.000	168.380	683	S503	2790.000	168.380	733	S453	1790.000	168.380
634	S552	3770.000	293.380	684	S502	2770.000	293.380	734	S452	1770.000	293.380
635	S551	3750.000	168.380	685	S501	2750.000	168.380	735	S451	1750.000	168.380
636	S550	3730.000	293.380	686	S500	2730.000	293.380	736	S450	1730.000	293.380
637	S549	3710.000	168.380	687	S499	2710.000	168.380	737	S449	1710.000	168.380
638	S548	3690.000	293.380	688	S498	2690.000	293.380	738	S448	1690.000	293.380
639	S547	3670.000	168.380	689	S497	2670.000	168.380	739	S447	1670.000	168.380
640	S546	3650.000	293.380	690	S496	2650.000	293.380	740	S446	1650.000	293.380
641	S545	3630.000	168.380	691	S495	2630.000	168.380	741	S445	1630.000	168.380
642	S544	3610.000	293.380	692	S494	2610.000	293.380	742	S444	1610.000	293.380
643	S543	3590.000	168.380	693	S493	2590.000	168.380	743	S443	1590.000	168.380
644	S542	3570.000	293.380	694	S492	2570.000	293.380	744	S442	1570.000	293.380
645	S541	3550.000	168.380	695	S491	2550.000	168.380	745	S441	1550.000	168.380
646	S540	3530.000	293.380	696	S490	2530.000	293.380	746	S440	1530.000	293.380
647	S539	3510.000	168.380	697	S489	2510.000	168.380	747	S439	1510.000	168.380
648	S538	3490.000	293.380	698	S488	2490.000	293.380	748	S438	1490.000	293.380
649	S537	3470.000	168.380	699	S487	2470.000	168.380	749	S437	1470.000	168.380
650	S536	3450.000	293.380	700	S486	2450.000	293.380	750	S436	1450.000	293.380

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Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
751	S435	1430.000	168.380	801	S385	430.000	168.380	851	S335	-570.000	168.380
752	S434	1410.000	293.380	802	S384	410.000	293.380	852	S334	-590.000	293.380
753	S433	1390.000	168.380	803	S383	390.000	168.380	853	S333	-610.000	168.380
754	S432	1370.000	293.380	804	S382	370.000	293.380	854	S332	-630.000	293.380
755	S431	1350.000	168.380	805	S381	350.000	168.380	855	S331	-650.000	168.380
756	S430	1330.000	293.380	806	S380	330.000	293.380	856	S330	-670.000	293.380
757	S429	1310.000	168.380	807	S379	310.000	168.380	857	S329	-690.000	168.380
758	S428	1290.000	293.380	808	S378	290.000	293.380	858	S328	-710.000	293.380
759	S427	1270.000	168.380	809	S377	270.000	168.380	859	S327	-730.000	168.380
760	S426	1250.000	293.380	810	S376	250.000	293.380	860	S326	-750.000	293.380
761	S425	1230.000	168.380	811	S375	230.000	168.380	861	S325	-770.000	168.380
762	S424	1210.000	293.380	812	S374	210.000	293.380	862	S324	-790.000	293.380
763	S423	1190.000	168.380	813	S373	190.000	168.380	863	S323	-810.000	168.380
764	S422	1170.000	293.380	814	S372	170.000	293.380	864	S322	-830.000	293.380
765	S421	1150.000	168.380	815	S371	150.000	168.380	865	S321	-850.000	168.380
766	S420	1130.000	293.380	816	S370	130.000	293.380	866	S320	-870.000	293.380
767	S419	1110.000	168.380	817	S369	110.000	168.380	867	S319	-890.000	168.380
768	S418	1090.000	293.380	818	S368	90.000	293.380	868	S318	-910.000	293.380
769	S417	1070.000	168.380	819	S367	70.000	168.380	869	S317	-930.000	168.380
770	S416	1050.000	293.380	820	S366	50.000	293.380	870	S316	-950.000	293.380
771	S415	1030.000	168.380	821	S365	30.000	168.380	871	S315	-970.000	168.380
772	S414	1010.000	293.380	822	S364	10.000	293.380	872	S314	-990.000	293.380
773	S413	990.000	168.380	823	S363	-10.000	168.380	873	S313	-1010.000	168.380
774	S412	970.000	293.380	824	S362	-30.000	293.380	874	S312	-1030.000	293.380
775	S411	950.000	168.380	825	S361	-50.000	168.380	875	S311	-1050.000	168.380
776	S410	930.000	293.380	826	S360	-70.000	293.380	876	S310	-1070.000	293.380
777	S409	910.000	168.380	827	S359	-90.000	168.380	877	S309	-1090.000	168.380
778	S408	890.000	293.380	828	S358	-110.000	293.380	878	S308	-1110.000	293.380
779	S407	870.000	168.380	829	S357	-130.000	168.380	879	S307	-1130.000	168.380
780	S406	850.000	293.380	830	S356	-150.000	293.380	880	S306	-1150.000	293.380
781	S405	830.000	168.380	831	S355	-170.000	168.380	881	S305	-1170.000	168.380
782	S404	810.000	293.380	832	S354	-190.000	293.380	882	S304	-1190.000	293.380
783	S403	790.000	168.380	833	S353	-210.000	168.380	883	S303	-1210.000	168.380
784	S402	770.000	293.380	834	S352	-230.000	293.380	884	S302	-1230.000	293.380
785	S401	750.000	168.380	835	S351	-250.000	168.380	885	S301	-1250.000	168.380
786	S400	730.000	293.380	836	S350	-270.000	293.380	886	S300	-1270.000	293.380
787	S399	710.000	168.380	837	S349	-290.000	168.380	887	S299	-1290.000	168.380
788	S398	690.000	293.380	838	S348	-310.000	293.380	888	S298	-1310.000	293.380
789	S397	670.000	168.380	839	S347	-330.000	168.380	889	S297	-1330.000	168.380
790	S396	650.000	293.380	840	S346	-350.000	293.380	890	S296	-1350.000	293.380
791	S395	630.000	168.380	841	S345	-370.000	168.380	891	S295	-1370.000	168.380
792	S394	610.000	293.380	842	S344	-390.000	293.380	892	S294	-1390.000	293.380
793	S393	590.000	168.380	843	S343	-410.000	168.380	893	S293	-1410.000	168.380
794	S392	570.000	293.380	844	S342	-430.000	293.380	894	S292	-1430.000	293.380
795	S391	550.000	168.380	845	S341	-450.000	168.380	895	S291	-1450.000	168.380
796	S390	530.000	293.380	846	S340	-470.000	293.380	896	S290	-1470.000	293.380
797	S389	510.000	168.380	847	S339	-490.000	168.380	897	S289	-1490.000	168.380
798	S388	490.000	293.380	848	S338	-510.000	293.380	898	S288	-1510.000	293.380
799	S387	470.000	168.380	849	S337	-530.000	168.380	899	S287	-1530.000	168.380
800	S386	450.000	293.380	850	S336	-550.000	293.380	900	S286	-1550.000	293.380

Downloaded from Elcodis.com electronic components distributor

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
901	S285	-1570.000	168.380	951	S235	-2570.000	168.380	1001	S185	-3570.000	168.380
902	S284	-1590.000	293.380	952	S234	-2590.000	293.380	1002	S184	-3590.000	293.380
903	S283	-1610.000	168.380	953	S233	-2610.000	168.380	1003	S183	-3610.000	168.380
904	S282	-1630.000	293.380	954	S232	-2630.000	293.380	1004	S182	-3630.000	293.380
905	S281	-1650.000	168.380	955	S231	-2650.000	168.380	1005	S181	-3650.000	168.380
906	S280	-1670.000	293.380	956	S230	-2670.000	293.380	1006	S180	-3670.000	293.380
907	S279	-1690.000	168.380	957	S229	-2690.000	168.380	1007	S179	-3690.000	168.380
908	S278	-1710.000	293.380	958	S228	-2710.000	293.380	1008	S178	-3710.000	293.380
909	S277	-1730.000	168.380	959	S227	-2730.000	168.380	1009	S177	-3730.000	168.380
910	S276	-1750.000	293.380	960	S226	-2750.000	293.380	1010	S176	-3750.000	293.380
911	S275	-1770.000	168.380	961	S225	-2770.000	168.380	1011	S175	-3770.000	168.380
912	S274	-1790.000	293.380	962	S224	-2790.000	293.380	1012	S174	-3790.000	293.380
913	S273	-1810.000	168.380	963	S223	-2810.000	168.380	1013	S173	-3810.000	168.380
914	S272	-1830.000	293.380	964	S222	-2830.000	293.380	1014	S172	-3830.000	293.380
915	S271	-1850.000	168.380	965	S221	-2850.000	168.380	1015	S171	-3850.000	168.380
916	S270	-1870.000	293.380	966	S220	-2870.000	293.380	1016	S170	-3870.000	293.380
917	S269	-1890.000	168.380	967	S219	-2890.000	168.380	1017	S169	-3890.000	168.380
918	S268	-1910.000	293.380	968	S218	-2910.000	293.380	1018	S168	-3910.000	293.380
919	S267	-1930.000	168.380	969	S217	-2930.000	168.380	1019	S167	-3930.000	168.380
920	S266	-1950.000	293.380	970	S216	-2950.000	293.380	1020	S166	-3950.000	293.380
921	S265	-1970.000	168.380	971	S215	-2970.000	168.380	1021	S165	-3970.000	168.380
922	S264	-1990.000	293.380	972	S214	-2990.000	293.380	1022	S164	-3990.000	293.380
923	S263	-2010.000	168.380	973	S213	-3010.000	168.380	1023	S163	-4010.000	168.380
924	S262	-2030.000	293.380	974	S212	-3030.000	293.380	1024	S162	-4030.000	293.380
925	S261	-2050.000	168.380	975	S211	-3050.000	168.380	1025	S161	-4050.000	168.380
926	S260	-2070.000	293.380	976	S210	-3070.000	293.380	1026	S160	-4070.000	293.380
927	S259	-2090.000	168.380	977	S209	-3090.000	168.380	1027	S159	-4090.000	168.380
928	S258	-2110.000	293.380	978	S208	-3110.000	293.380	1028	S158	-4110.000	293.380
929	S257	-2130.000	168.380	979	S207	-3130.000	168.380	1029	S157	-4130.000	168.380
930	S256	-2150.000	293.380	980	S206	-3150.000	293.380	1030	S156	-4150.000	293.380
931	S255	-2170.000	168.380	981	S205	-3170.000	168.380	1031	S155	-4170.000	168.380
932	S254	-2190.000	293.380	982	S204	-3190.000	293.380	1032	S154	-4190.000	293.380
933	S253	-2210.000	168.380	983	S203	-3210.000	168.380	1033	S153	-4210.000	168.380
934	S252	-2230.000	293.380	984	S202	-3230.000	293.380	1034	S152	-4230.000	293.380
935	S251	-2250.000	168.380	985	S201	-3250.000	168.380	1035	S151	-4250.000	168.380
936	S250	-2270.000	293.380	986	S200	-3270.000	293.380	1036	S150	-4270.000	293.380
937	S249	-2290.000	168.380	987	S199	-3290.000	168.380	1037	S149	-4290.000	168.380
938	S248	-2310.000	293.380	988	S198	-3310.000	293.380	1038	S148	-4310.000	293.380
939	S247	-2330.000	168.380	989	S197	-3330.000	168.380	1039	S147	-4330.000	168.380
940	S246	-2350.000	293.380	990	S196	-3350.000	293.380	1040	S146	-4350.000	293.380
941	S245	-2370.000	168.380	991	S195	-3370.000	168.380	1041	S145	-4370.000	168.380
942	S244	-2390.000	293.380	992	S194	-3390.000	293.380	1042	S144	-4390.000	293.380
943	S243	-2410.000	168.380	993	S193	-3410.000	168.380	1043	S143	-4410.000	168.380
944	S242	-2430.000	293.380	994	S192	-3430.000	293.380	1044	S142	-4430.000	293.380
945	S241	-2450.000	168.380	995	S191	-3450.000	168.380	1045	S141	-4450.000	168.380
946	S240	-2470.000	293.380	996	S190	-3470.000	293.380	1046	S140	-4470.000	293.380
947	S239	-2490.000	168.380	997	S189	-3490.000	168.380	1047	S139	-4490.000	168.380
948	S238	-2510.000	293.380	998	S188	-3510.000	293.380	1048	S138	-4510.000	293.380
949	S237	-2530.000	168.380	999	S187	-3530.000	168.380	1049	S137	-4530.000	168.380
950	S236	-2550.000	293.380	1000	S186	-3550.000	293.380	1050	S136	-4550.000	293.380

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Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1051	S135	-4570.000	168.380	1101	S85	-5570.000	168.380	1151	S35	-6570.000	168.380
1052	S134	-4590.000	293.380	1102	S84	-5590.000	293.380	1152	S34	-6590.000	293.380
1053	S133	-4610.000	168.380	1103	S83	-5610.000	168.380	1153	S33	-6610.000	168.380
1054	S132	-4630.000	293.380	1104	S82	-5630.000	293.380	1154	S32	-6630.000	293.380
1055	S131	-4650.000	168.380	1105	S81	-5650.000	168.380	1155	S31	-6650.000	168.380
1056	S130	-4670.000	293.380	1106	S80	-5670.000	293.380	1156	S30	-6670.000	293.380
1057	S129	-4690.000	168.380	1107	S79	-5690.000	168.380	1157	S29	-6690.000	168.380
1058	S128	-4710.000	293.380	1108	S78	-5710.000	293.380	1158	S28	-6710.000	293.380
1059	S127	-4730.000	168.380	1109	S77	-5730.000	168.380	1159	S27	-6730.000	168.380
1060	S126	-4750.000	293.380	1110	S76	-5750.000	293.380	1160	S26	-6750.000	293.380
1061	S125	-4770.000	168.380	1111	S75	-5770.000	168.380	1161	S25	-6770.000	168.380
1062	S124	-4790.000	293.380	1112	S74	-5790.000	293.380	1162	S24	-6790.000	293.380
1063	S123	-4810.000	168.380	1113	S73	-5810.000	168.380	1163	S23	-6810.000	168.380
1064	S122	-4830.000	293.380	1114	S72	-5830.000	293.380	1164	S22	-6830.000	293.380
1065	S121	-4850.000	168.380	1115	S71	-5850.000	168.380	1165	S21	-6850.000	168.380
1066	S120	-4870.000	293.380	1116	S70	-5870.000	293.380	1166	S20	-6870.000	293.380
1067	S119	-4890.000	168.380	1117	S69	-5890.000	168.380	1167	S19	-6890.000	168.380
1068	S118	-4910.000	293.380	1118	S68	-5910.000	293.380	1168	S18	-6910.000	293.380
1069	S117	-4930.000	168.380	1119	S67	-5930.000	168.380	1169	S17	-6930.000	168.380
1070	S116	-4950.000	293.380	1120	S66	-5950.000	293.380	1170	S16	-6950.000	293.380
1071	S115	-4970.000	168.380	1121	S65	-5970.000	168.380	1171	S15	-6970.000	168.380
1072	S114	-4990.000	293.380	1122	S64	-5990.000	293.380	1172	S14	-6990.000	293.380
1073	S113	-5010.000	168.380	1123	S63	-6010.000	168.380	1173	S13	-7010.000	168.380
1074	S112	-5030.000	293.380	1124	S62	-6030.000	293.380	1174	S12	-7030.000	293.380
1075	S111	-5050.000	168.380	1125	S61	-6050.000	168.380	1175	S11	-7050.000	168.380
1076	S110	-5070.000	293.380	1126	S60	-6070.000	293.380	1176	S10	-7070.000	293.380
1077	S109	-5090.000	168.380	1127	S59	-6090.000	168.380	1177	S9	-7090.000	168.380
1078	S108	-5110.000	293.380	1128	S58	-6110.000	293.380	1178	S8	-7110.000	293.380
1079	S107	-5130.000	168.380	1129	S57	-6130.000	168.380	1179	S7	-7130.000	168.380
1080	S106	-5150.000	293.380	1130	S56	-6150.000	293.380	1180	S6	-7150.000	293.380
1081	S105	-5170.000	168.380	1131	S55	-6170.000	168.380	1181	S5	-7170.000	168.380
1082	S104	-5190.000	293.380	1132	S54	-6190.000	293.380	1182	S4	-7190.000	293.380
1083	S103	-5210.000	168.380	1133	S53	-6210.000	168.380	1183	S3	-7210.000	168.380
1084	S102	-5230.000	293.380	1134	S52	-6230.000	293.380	1184	S2	-7230.000	293.380
1085	S101	-5250.000	168.380	1135	S51	-6250.000	168.380	1185	S1	-7250.000	168.380
1086	S100	-5270.000	293.380	1136	S50	-6270.000	293.380	1186	S0	-7270.000	293.380
1087	S99	-5290.000	168.380	1137	S49	-6290.000	168.380	1187	DUMMY	-7290.000	168.380
1088	S98	-5310.000	293.380	1138	S48	-6310.000	293.380	1188	DUMMY	-7350.000	293.380
1089	S97	-5330.000	168.380	1139	S47	-6330.000	168.380	1189	DUMMY	-7370.000	168.380
1090	S96	-5350.000	293.380	1140	S46	-6350.000	293.380	1190	G318	-7390.000	293.380
1091	S95	-5370.000	168.380	1141	S45	-6370.000	168.380	1191	G316	-7410.000	168.380
1092	S94	-5390.000	293.380	1142	S44	-6390.000	293.380	1192	G314	-7430.000	293.380
1093	S93	-5410.000	168.380	1143	S43	-6410.000	168.380	1193	G312	-7450.000	168.380
1094	S92	-5430.000	293.380	1144	S42	-6430.000	293.380	1194	G310	-7470.000	293.380
1095	S91	-5450.000	168.380	1145	S41	-6450.000	168.380	1195	G308	-7490.000	168.380
1096	S90	-5470.000	293.380	1146	S40	-6470.000	293.380	1196	G306	-7510.000	293.380
1097	S89	-5490.000	168.380	1147	S39	-6490.000	168.380	1197	G304	-7530.000	168.380
1098	S88	-5510.000	293.380	1148	S38	-6510.000	293.380	1198	G302	-7550.000	293.380
1099	S87	-5530.000	168.380	1149	S37	-6530.000	168.380	1199	G300	-7570.000	168.380
1100	S86	-5550.000	293.380	1150	S36	-6550.000	293.380	1200	G298	-7590.000	293.380

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Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1201	G296	-7610.000	168.380	1253	G192	-8650.000	168.380	1305	G88	-9690.000	168.380
1202	G294	-7630.000	293.380	1254	G190	-8670.000	293.380	1306	G86	-9710.000	293.380
1203	G292	-7650.000	168.380	1255	G188	-8690.000	168.380	1307	G84	-9730.000	168.380
1204	G290	-7670.000	293.380	1256	G186	-8710.000	293.380	1308	G82	-9750.000	293.380
1205	G288	-7690.000	168.380	1257	G184	-8730.000	168.380	1309	G80	-9770.000	168.380
1206	G286	-7710.000	293.380	1258	G182	-8750.000	293.380	1310	G78	-9790.000	293.380
1207	G284	-7730.000	168.380	1259	G180	-8770.000	168.380	1311	G76	-9810.000	168.380
1208	G282	-7750.000	293.380	1260	G178	-8790.000	293.380	1312	G74	-9830.000	293.380
1209	G280	-7770.000	168.380	1261	G176	-8810.000	168.380	1313	G72	-9850.000	168.380
1210	G278	-7790.000	293.380	1262	G174	-8830.000	293.380	1314	G70	-9870.000	293.380
1211	G276	-7810.000	168.380	1263	G172	-8850.000	168.380	1315	G68	-9890.000	168.380
1212	G274	-7830.000	293.380	1264	G170	-8870.000	293.380	1316	G66	-9910.000	293.380
1213	G272	-7850.000	168.380	1265	G168	-8890.000	168.380	1317	G64	-9930.000	168.380
1214	G270	-7870.000	293.380	1266	G166	-8910.000	293.380	1318	G62	-9950.000	293.380
1215	G268	-7890.000	168.380	1267	G164	-8930.000	168.380	1319	G60	-9970.000	168.380
1216	G266	-7910.000	293.380	1268	G162	-8950.000	293.380	1320	G58	-9990.000	293.380
1217	G264	-7930.000	168.380	1269	G160	-8970.000	168.380	1321	G56	-10010.000	168.380
1218	G262	-7950.000	293.380	1270	G158	-8990.000	293.380	1322	G54	-10030.000	293.380
1219	G260	-7970.000	168.380	1271	G156	-9010.000	168.380	1323	G52	-10050.000	168.380
1220	G258	-7990.000	293.380	1272	G154	-9030.000	293.380	1324	G50	-10070.000	293.380
1221	G256	-8010.000	168.380	1273	G152	-9050.000	168.380	1325	G48	-10090.000	168.380
1222	G254	-8030.000	293.380	1274	G150	-9070.000	293.380	1326	G46	-10110.000	293.380
1223	G252	-8050.000	168.380	1275	G148	-9090.000	168.380	1327	G44	-10130.000	168.380
1224	G250	-8070.000	293.380	1276	G146	-9110.000	293.380	1328	G42	-10150.000	293.380
1225	G248	-8090.000	168.380	1277	G144	-9130.000	168.380	1329	G40	-10170.000	168.380
1226	G246	-8110.000	293.380	1278	G142	-9150.000	293.380	1330	G38	-10190.000	293.380
1227	G244	-8130.000	168.380	1279	G140	-9170.000	168.380	1331	G36	-10210.000	168.380
1228	G242	-8150.000	293.380	1280	G138	-9190.000	293.380	1332	G34	-10230.000	293.380
1229	G240	-8170.000	168.380	1281	G136	-9210.000	168.380	1333	G32	-10250.000	168.380
1230	G238	-8190.000	293.380	1282	G134	-9230.000	293.380	1334	G30	-10270.000	293.380
1231	G236	-8210.000	168.380	1283	G132	-9250.000	168.380	1335	G28	-10290.000	168.380
1232	G234	-8230.000	293.380	1284	G130	-9270.000	293.380	1336	G26	-10310.000	293.380
1233	G232	-8250.000	168.380	1285	G128	-9290.000	168.380	1337	G24	-10330.000	168.380
1234	G230	-8270.000	293.380	1286	G126	-9310.000	293.380	1338	G22	-10350.000	293.380
1235	G228	-8290.000	168.380	1287	G124	-9330.000	168.380	1339	G20	-10370.000	168.380
1236	G226	-8310.000	293.380	1288	G122	-9350.000	293.380	1340	G18	-10390.000	293.380
1237	G224	-8330.000	168.380	1289	G120	-9370.000	168.380	1341	G16	-10410.000	168.380
1238	G222	-8350.000	293.380	1290	G118	-9390.000	293.380	1342	G14	-10430.000	293.380
1239	G220	-8370.000	168.380	1291	G116	-9410.000	168.380	1343	G12	-10450.000	168.380
1240	G218	-8390.000	293.380	1292	G114	-9430.000	293.380	1344	G10	-10470.000	293.380
1241	G216	-8410.000	168.380	1293	G112	-9450.000	168.380	1345	G8	-10490.000	168.380
1242	G214	-8430.000	293.380	1294	G110	-9470.000	293.380	1346	G6	-10510.000	293.380
1243	G212	-8450.000	168.380	1295	G108	-9490.000	168.380	1347	G4	-10530.000	168.380
1244	G210	-8470.000	293.380	1296	G106	-9510.000	293.380	1348	G2	-10550.000	293.380
1245	G208	-8490.000	168.380	1297	G104	-9530.000	168.380	1349	G0	-10570.000	168.380
1246	G206	-8510.000	293.380	1298	G102	-9550.000	293.380	1350	DUMMY	-10590.000	293.380
1247	G204	-8530.000	168.380	1299	G100	-9570.000	168.380	1351	DUMMY	-10610.000	168.380
1248	G202	-8550.000	293.380	1300	G98	-9590.000	293.380	1352	DUMMY	-10630.000	293.380
1249	G200	-8570.000	168.380	1301	G96	-9610.000	168.380	1353	DUMMY	-10650.000	168.380
1250	G198	-8590.000	293.380	1302	G94	-9630.000	293.380	1354	DUMMY	-10670.000	293.380
1251	G196	-8610.000	168.380	1303	G92	-9650.000	168.380				
1252	G194	-8630.000	293.380	1304	G90	-9670.000	293.380				

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5 PIN DESCRIPTION

Remark:

I = Input;
O = Output;
IO = Bi-directional;
P = Power;
VCC = System VDD;
GND = System VSS;

Table 5-1: Power Supply Pins

Pin Name	Type	Connect to	Function	Description	When not in use
VSS	P	GND	Ground of the Power Supply	System ground pin of the IC.	-
AVSS		GND		Grounding for analog circuit.	-
IOGND		GND		Grounding for logic circuit.	
VCHS		AVSS		Grounding for booster circuit.	-
VCI	P	Power Supply	Power Supply for Analog Circuits	Booster input voltage pin. - Connect to voltage source between 2.5V to 3.6V	-
VCIP		VCI		Voltage supply pin for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. - Connect to same source of VCI	-
VCIM	O	Stabilizing capacitor	Booster voltages	Negative voltage of VCI.	-
VCIX2		Stabilizing capacitor		Equals to 2x VCI	-
VCIX2J	P	VCIX2 on FPC	Voltage for analog	They are the power supply used by on chip analog blocks and VGH/VGL DC-DC.	-
VCIX2G		VCIX2 on FPC			-
VCOMR	I	External voltage source or Open	External Reference	This pin provides voltage reference for internal voltage regulator when register VDV[4:0] of Power Control 4 set to “01111”. - Connect to an external voltage source for reference	Open
VCOMH	O	Stabilizing capacitor	Voltages for VCOM Signal	This pin indicates a HIGH level of VCOM generated in driving the VCOM alternation.	-
VCOML		Stabilizing capacitor		This pin indicates a LOW level of VCOM generated in driving the VCOM alternation.	-
VLCD63	O	Stabilizing capacitor	LCD Driving Voltages	This pin is the maximum source driver voltage.	-
VGH		Stabilizing capacitor		A positive power output pin for gate driver and for MTP programming	-
VGL		Stabilizing capacitor		A negative power output pin for gate driver.	-
EXVR	I	GND	External Reference	External reference of internal gamma resistor - Connect to VSS	-
CXP	I	Booster capacitor	Booster and Stabilization Capacitors	- Connect a capacitor to CXN	-
CXN				- Connect a capacitor to CXP	-
CYP		Booster capacitor		- Connect a capacitor to CYN	-
CYN				- Connect a capacitor to CYP	-
C1P		Booster capacitor		- Connect a capacitor to C1N	-
C1N				- Connect a capacitor to C1P	-
C2P		Booster capacitor		- Connect a capacitor to C2N	-
C2N				- Connect a capacitor to C2P	-
C3P		Booster capacitor		- Connect a capacitor to C3N	-
C3N				- Connect a capacitor to C3P	-
CDUM1P		Stabilizing capacitor	Stabilization Capacitors	- Connect a capacitor to CDUM1N	

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Pin Name	Type	Connect to	Function	Description	When not in use
					Open
CDUM1N		Stabilizing capacitor		- Connect a capacitor to CDUM1P	Open
VCORE	P	Stabilizing capacitor	Power for Core Logic	Vdd for core use. Connect a capacitor for stabilization	-
VREGC	P	VCORE	Regulator output for logic circuits	Regulator output for VCORE use.	-
VDDIO	P	Power Supply	Power for interface logic pins	Voltage input pin for logic I/O, connect to system VDD. - Connect to voltage source between 1.4V to 3.6V	-
VCIR	P	Power Supply	Power for interface logic pins	Internal regular input for logic supply : VCIR=2.5V-3.3V	-

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Table 5-2 - Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
DC	I	MPU	Logic Control	Data or command	V_{DDIO} or V_{ss}
CSB		MPU		Chip select pin for 6800/8080/SPI interface	-
RD		MPU		6800-system : E (enable signal) 8080-system : RD (read strobe signal) Serial mode : Not used and should be connected to V_{DDIO} or V_{ss}	V_{DDIO} or V_{ss}
WR		MPU		68-system : RW (indicates read cycle when High, write cycle when Low) 80-system : WR (write strobe signal) Serial mode : SCL (serial clock input)	V_{DDIO} or V_{ss}
D0-D17	IO	MPU	Data bus	For parallel mode, 8/9/16/18 bit interface. Please refer to Section 13 Interface Mapping for definition. Unused pins should connect to V_{SS}.	V_{SS}
WSYNC	O	MPU	Logic Control	Ram Write Synchronization output	Open
OE	I	MPU	Display Timing Signals	Display enable pin from controller. Data will be treated as dummy regardless the OE status during front/back porch setting at registers R16 and R17.	Vss
DOTCLK	I	MPU		Dot-clock signal and oscillator source. A non-stop external clock must be provided to that pin even at front or black porch non-display period.	Vss
HSYNC	I	MPU		Line Synchronization input	V_{SS}
VSYNC	I	MPU		Frame/Ram Write Synchronization input	V_{SS}
RESB	I	MPU	System Reset	System reset pin. - An active low pulse at this pin will reset the IC, Connect to V_{DDIO} in normal operation	-
SDI	I	MPU	Serial interface	Data input pin in serial interface	V_{SS}
SDO	O	MPU		Data output pin in serial interface	Open

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Table 5-3: Mode Selection Pins

<table>
<tr><th>Name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>PS[3:0]</td><td>I</td><td>V_{DDIO} or V_{SS}</td><td>Interface Selection</td><td>
<table>
<tr><th>PS3</th><th>PS2</th><th>PS1</th><th>PS0</th><th>Interface Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>16-bit 6800 parallel interface</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8-bit 6800 parallel interface</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>16-bit 8080 parallel interface</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>9-bit generic D[8:0] (262k colour) + 3-wire SPI If 65K color, D3 shorts to D8 internally</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit generic (262k colour) + 3-wire SPI</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit generic (262k colour) + 3-wire SPI</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>6-bit generic D[8:3] (262k colour) + 3-wire SPI</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>18-bits 6800 parallel interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9-bits 6800 parallel interface</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>18-bit 8080 parallel interface</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>9-bit 8080 parallel interface</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>3-wire SPI</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-wire SPI</td></tr>
</table>
</td><td>-</td></tr>
</table>

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Table 5-4: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
VCOM	O	LCD	LCD Driving Signals	A power supply for the TFT-display common electrode.	Open
G0-G319		LCD		Gate driver output pins. These pins output V_{GH}, V_{GL} or V_{GOFFH} level.	Open
S0-S719		LCD		Source driver output pins. S(3n) : display Red if BGR = LOW, Blue if BGR = HIGH. S(3n+1) : display Green. S(3n+2) : display Blue if BGR = LOW, Red if BGR = HIGH.	Open

Table 5-5: Miscellaneous Pins

Name	Type	Connect to	Function	Description	When not in use
NC	-	-	-	These pins must be left open and cannot be connected together	Open
DUMMY	-	-	-	Floating pins and no connection inside the IC. These pins should be open.	Open
TESTA	IO	FPC	IC Testing Signal	Test pin of the internal circuit. - Leave this pin open and insert test point in FPC	Open
TESTB		FPC		Test pin of the internal circuit. - Leave this pin open and insert test point in FPC	Open
TESTC		FPC		Test pin of the internal circuit. - Leave this pin open and insert test point in FPC	Open

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6 BLOCK FUNCTION DESCRIPTION

6.1 System Interface

The System Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series high speed parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS3, PS2, PS1 and PS0 pins. Please refer to the pin descriptions on page 19.

a) MPU Parallel 6800-series Interface

The parallel Interface consists of 18 bi-directional data pins D[17:0], $R/\overline{W}$, $D/\overline{C}$, E and $\overline{CS}$. $R/\overline{W}$ input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. $R/\overline{W}$ input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of $D/\overline{C}$ input. The E input serves as data latch signal (clock) when high provided that $\overline{CS}$ is low. Please refer to Parallel Interface Timing Diagram of 6800-series microprocessors. In order to match the operating frequency of the GDDRAM with that of the MCU, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

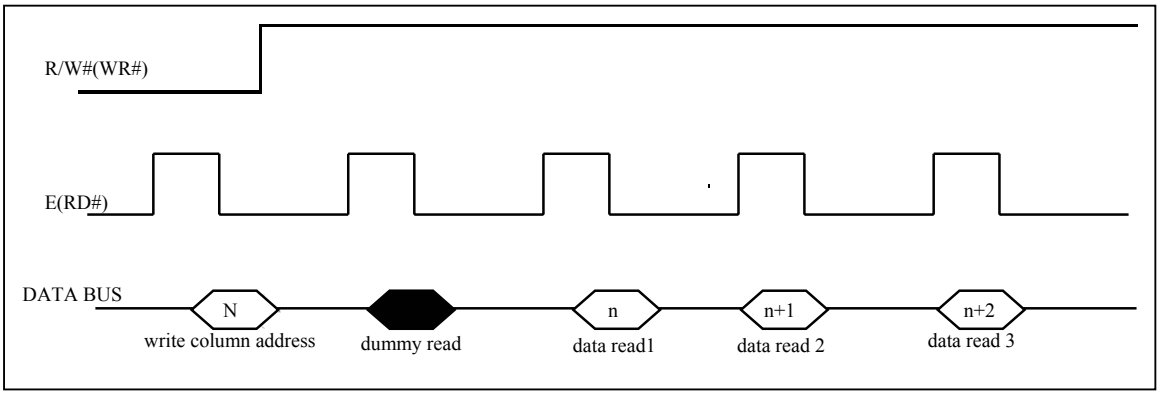

Figure 6-1 – Read Display Data

b) MPU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins D[17:0], RD, WR, DC and CSB. RD input serves as data read latch signal (clock) when low provided that CSB is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by DC. WR input serves as data write latch signal (clock) when low provided that CSB is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by DC. A dummy read is also required before the first actual display data read for 8080-series interface. Please refer Figure 7-1.

c) 3-lines Serial Peripheral Interface

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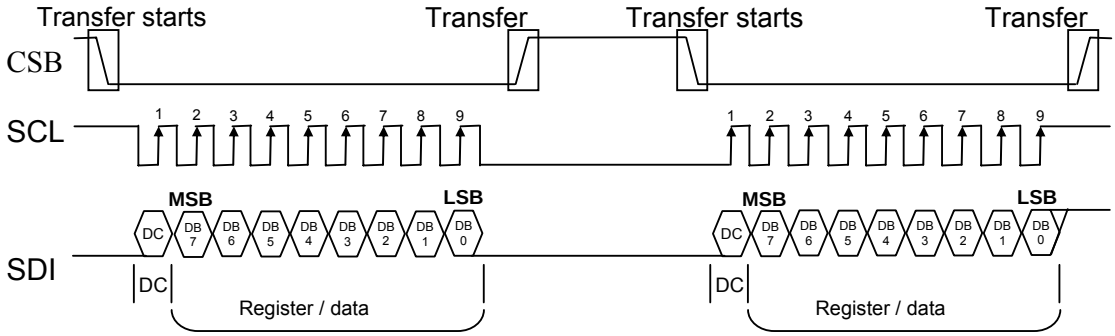
The operation is similar to 4-lines serial peripheral interface while DC is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0).

	6800 – series Parallel Interface	8080 – series Parallel Interface	MCU Serial Interface
Data Read	18/16/9/8-bits	18/16/9/8-bits	Yes
Data Write	18/16/9/8-bits	18/16/9/8-bits	8-bits
Command Read	Status only	Status only	No
Command Write	Yes	Yes	8-bits

Table 6-1 - Data bus selection modes

Figure 6-2: 3-wire SPI interface (9 bits)



d) 4-wire Serial Peripheral Interface (8 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (CSB), serial transfer clock line (SCL), serial input data (SDI). The serial data transfer starts at the falling edge of CSB input and ends at the rising edge of CSB.SDC determinate the data of SDI which is register or data.

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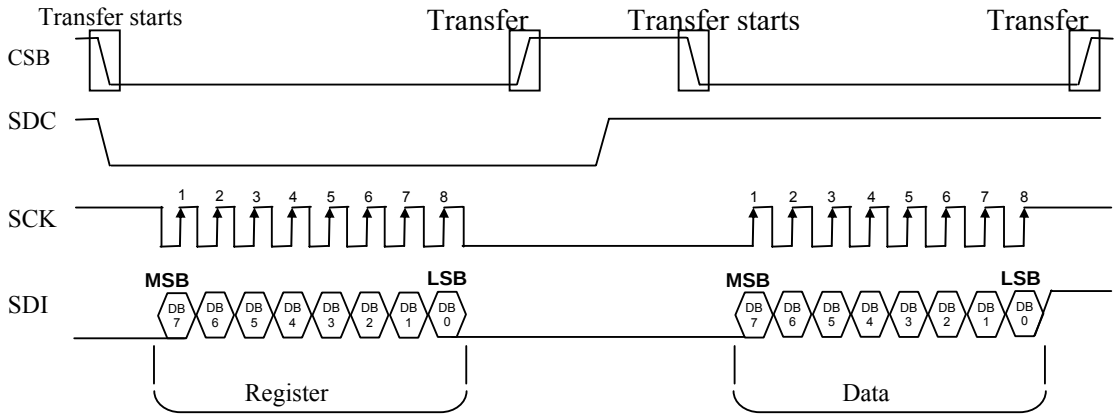
Figure 6-3: 4-wire SPI interface (8 bits)



6.2 RGB Interface

SSD1298 supports RGB interface. RGB interface unit consists of D[17:0], HSYNC, VSYNC, DOTCLK and OE signals for display moving pictures. When the RGB interface is selected, the display operation is synchronized with external control signals (HSYNC, VSYNC and DOTCLK). Data is written in synchronization with the control signals when DEN is enabled for write operation in order to avoid flicker or tearing effect while updating display data.

6.3 Address Counter (AC)

The address counter (AC) assigns address to the GDDRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

6.4 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 240 RGB x 320 x 18 / 8 = 172,800 bytes. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command “Data Output/Scan direction” for detail description.

Four pages of display data forms a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command “Set area Scroll” and “Set Scroll Start”.

6.5 Gamma/Grayscale Voltage Generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma adjustment resister. 262,144 possible colors can be displayed when 1 pixel = 18 bit. For details, see the gamma adjustment register.

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6.6 Booster and Regulator Circuit

These two functional blocks generate the voltage of VGH, VGL, VCOM levels and VLCD0~63 which are necessary for operating a TFT LCD.

6.7 Timing Generator

The timing generator generates a timing signal for the operation of internal circuit such as the internal RAM accessing, date output timing etc.

6.8 Oscillation Circuit (OSC)

This module is an on-chip low power RC oscillator circuitry. The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the display timing generator.

6.9 Data Latches

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

6.10 Liquid Crystal Driver Circuit

SSD1298 consists of a 720-output source driver (S0-S719) and a 320-output gate driver (G0-G319). The display image data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the RL bit and the shift direction of gate output from the gate driver can be changed by setting the TB bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the TB bit to select the operimal scan mode for the module.

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7 COMMAND TABLE

Table 7-1 - Command Table

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R00h	Oscillation Start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	GD	BGR	SM	TB	MUX8	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
	(3B3Fh)			0	0	1	1	1	0	1	1	0	0	1	1	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	All GAMAS[2:0] setting 8 color (6A64h)			0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
	(5308h)			0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0004h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
R0Fh	Gate scan start position	0	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R10h	Sleep mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R11h	Entry mode	0	1	VS mode	DFM1	DFM0	0	Denmode	WMode	Nosync	DMode	TY1	TY0	ID1	ID0	AM	0	0	0
	(6830h)			0	1	1	0	0	1	1	0	0	0	1	1	0	0	0	0
R15h	Entry mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	INVDOT	INVDEN	INVHS	INVVS
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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(continued)

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R22h	RAM data write	0	1	Data[17:0] mapping depends on the interface setting															
	RAM data read	1	1																
R23h	RAM write data mask (1)	0	1	WMR5	WMR4	WMR3	WMR2	WMR1	WMR0	0	0	WMG5	WMG4	WMG3	WMG2	WMG1	WMG0	0	0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R24h	RAM write data mask (2)	0	1	0	0	0	0	0	0	0	0	WMB5	WMB4	WMB3	WMB2	WMB1	WMB0	0	0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R25h	Frame Frequency	0	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
	(8000h)			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R28h	VCOM OTP (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R29h	VCOM OTP (80C0h)	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R41h	Vertical scroll control (1)	0	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R42h	Vertical scroll control (2)	0	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R44h	Horizontal RAM address position	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	(EF00h)			1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
R45h	Vertical RAM address start position	0	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	Vertical RAM address end position	0	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R48h	First window start	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	First window end	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R4Ah	Second window start	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	Second window end	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R4Eh	Set GDDRAM X address counter	0	1	0	0	0	0	0	0	0	0	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	Set GDDRAM Y address counter	0	1	0	0	0	0	0	0	0	YAD8	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: In R01h, bits REV, BGR, TB, RL, CM will override the corresponding hardware pins settings.
Setting R28h as 0x0006 is required before setting R25h and R29h registers.

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8 COMMAND DESCRIPTION

Index (IR)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index instruction specifies the RAM control indexes (R00h to RFFh). It sets the register number in the range of 00000000 to 11111111 in binary form. But do not access to Index register and instruction bits which do not have it's own index register.

Device Code Read (R00h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1

If this register is read forcibly, 8999h is read.

Oscillator (R00h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OSCEN: The oscillator will be turned on when OSCEN = 1, off when OSCEN = 0.

Driver Output Control (R01h) (POR = 3B3Fh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RL	REV	GD	BGR	SM	TB	MUX8	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		0	0	1	1	1	0	1	1	0	0	1	1	1	1	1	1

REV: Displays all character and graphics display sections with reversal when REV = "1". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data	Source Output level	
		Vcom = "L"	Vcom = "H"
0	00000H : 3FFFFH	V63 : V0	V0 : V63
1	00000H : 3FFFFH	V0 : V63	V63 : V0

GD: Selects the 1st output Gate

GD = '0', G0 is 1st output Gate, Gate sequence G0, G1, G2, G3, …, G318, G319

GD = '1', G1 is 1st output Gate, Gate sequence G1, G0, G3, G2, …, G319, G318

BGR: Selects the order from RGB to BGR in writing 18-bit pixel data in the GDDRAM.

When BGR = "0" <R><G><B> color is assigned from S0.

When BGR = "1" <B><G><R> color is assigned from S0.

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SM: Change scanning order of gate driver.

SM	Gate scan squence (GD='0')
0	G0, G1, G2, G3……G219 (left and right gate interlaced)
1	G0, G2, ……G318, G1, G3, ……G319

See "Scan mode setting" on next page.

TB: Selects the output shift direction of the gate driver.
When TB = 1, G0 shifts to G319.
When TB = 0, G319 shifts to G0.

RL: Selects the output shift direction of the source driver.
When RL = "1", S0 shifts to S719 and <R><G><B> color is assigned from S0.
When RL = "0", S719 shifts to S0 and <R><G><B> color is assigned from S719.
Set RL bit and BGR bit when changing the dot order of R, G and B. RL setting will be ignored when display with RAM (Dmode[1:0] = 00).

MUX[8:0]: Specify number of lines for the LCD driver. MUX[8:0] settings cannot exceed 319.
Remark: When using the partial display, the output for non-display area will be minimum voltage.

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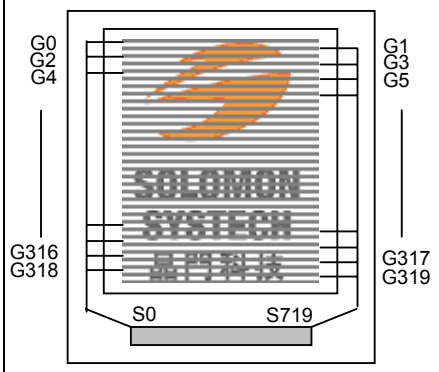
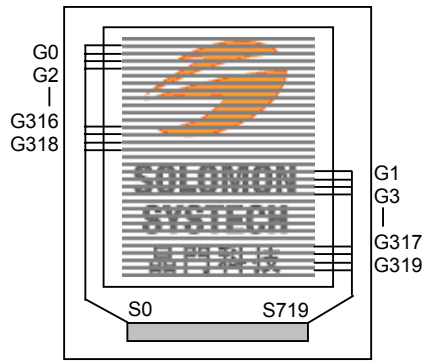
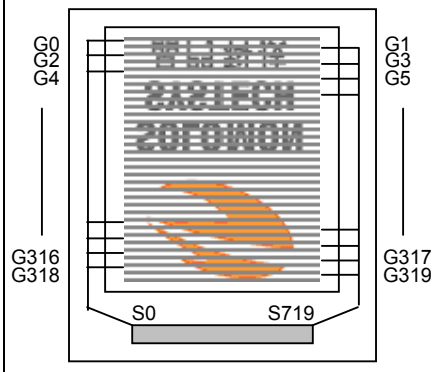
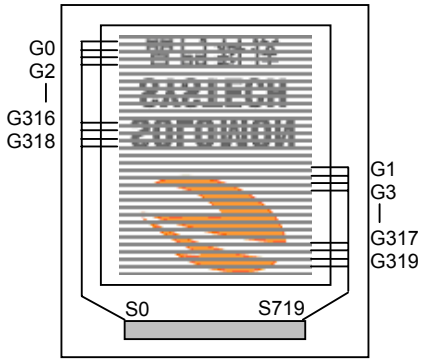
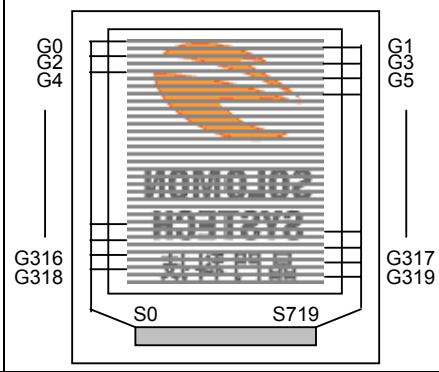
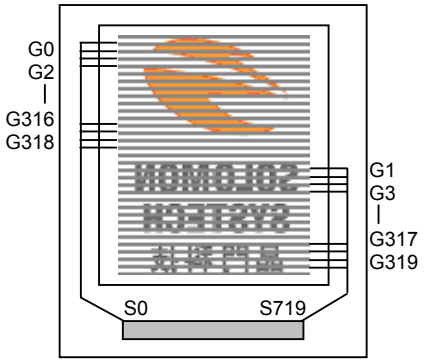
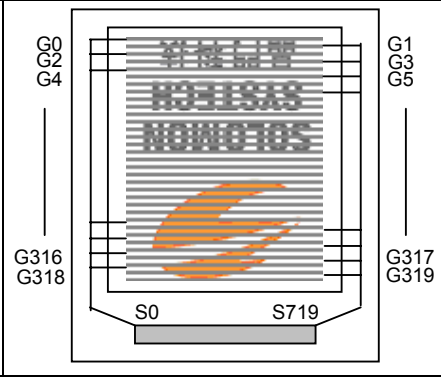
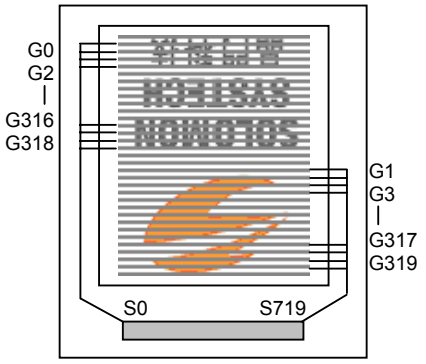
GD=’0’, G0 is the 1st gate output channel, gate output sequence is G0, G1, G2, G3, …, G318, G319.

	SM = 0	SM = 1
TB = 1 **RL = 1**		
TB = 0 **RL = 1**		
TB = 1 **RL = 0**		
TB = 0 **RL = 0**		

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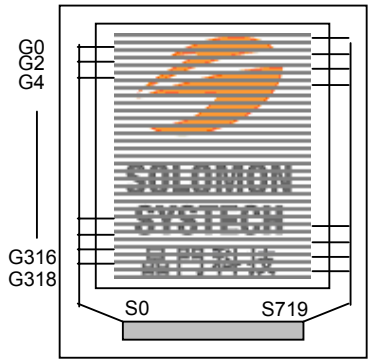
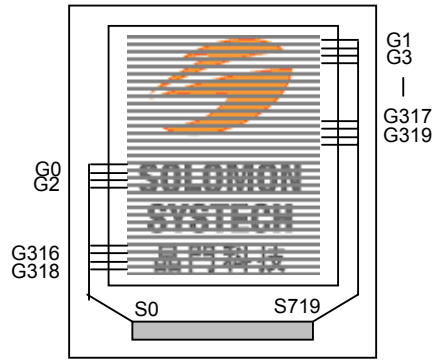
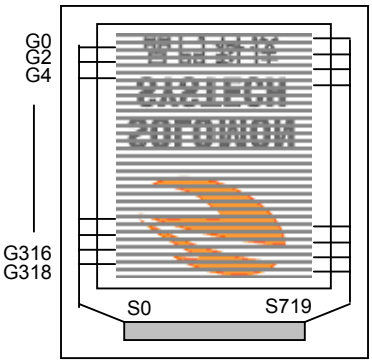
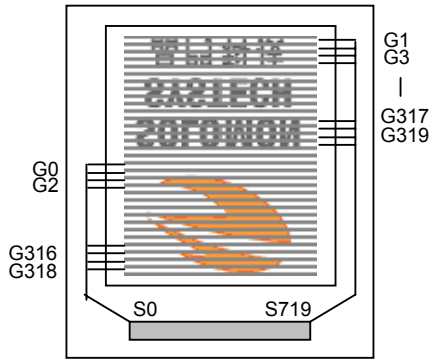
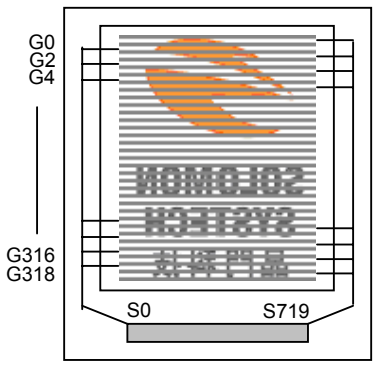
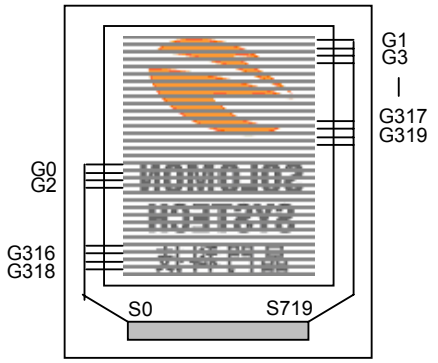
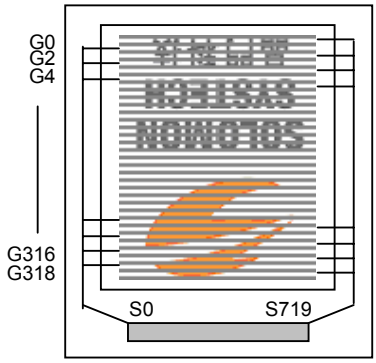
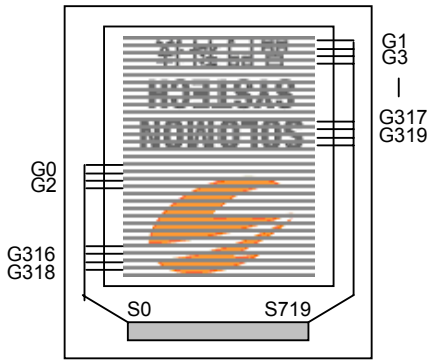
GD='1', G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, …, G319, G318.

	SM = 0	SM = 1
TB = 1 **RL = 1**		
TB = 0 **RL = 1**		
TB = 1 **RL = 0**		
TB = 0 **RL = 0**		

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LCD-Driving-Waveform Control (R02h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

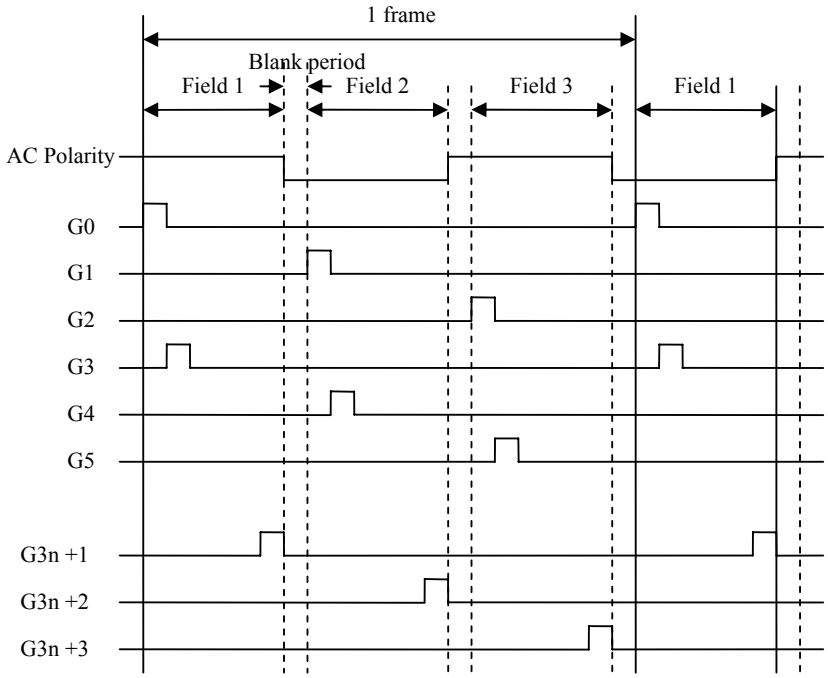
FLD: Set display in interlace drive mode to protect from flicker. It splits one frame into 3 fields and drive.
When FLD = 1, it is 3 field driving, which also limit VBP = 1.
When FLD = 0, it is normal driving.

The following figure shows the gate selection when the 3-field invension is enabled and the output waveform of the 3-field interlaced driving.

Table 8-1 - 3-field interlace driving

TB = 1			TB = 0		
Gate	FLD = 0	FLD = 1	Gate	FLD = 0	FLD = 1
G0	X		G319	X	
G1	X		G318	X	
G2	X	X	G317	X	X
G3	X		G316	X	
G4	X		G315	X	
	X	X		X	X
	X			X	
	X			x	
G317	X		G2	X	
G318	X		G1	X	
G319	X	X	G0	X	X

Figure 8-1 - gate output timing in 3-field interlacing driving



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B/C: Select the liquid crystal drive waveform VCOM.

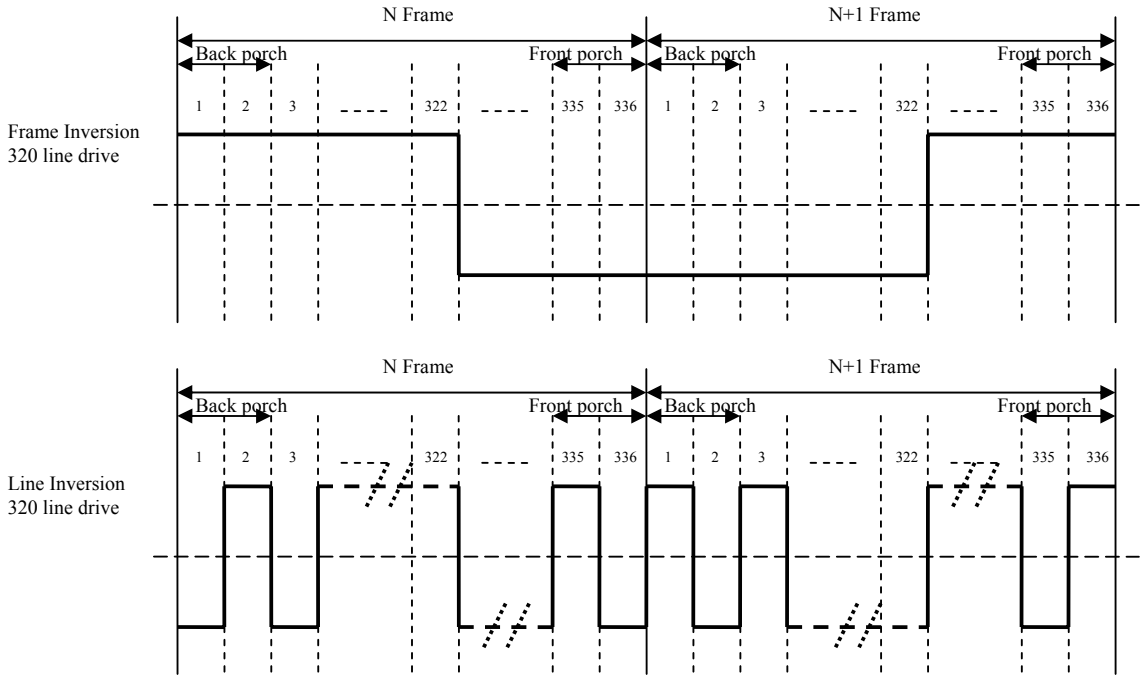
When B/C = 0, frame inversion of the LCD driving signal is enabled.

When B/C = 1, a N-line inversion waveform is generated and alternates in a N-line equals to NW[7:0]+1.

EOR: When B/C = 1 and EOR = 1, the odd/even frame-select signals and the N-line inversion signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the lines of the LCD driven and the N-lines.

NW[7:0]: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). N-line is equal to NW[7:0]+1.

Figure 8-2 - Line Inversion AC Driver



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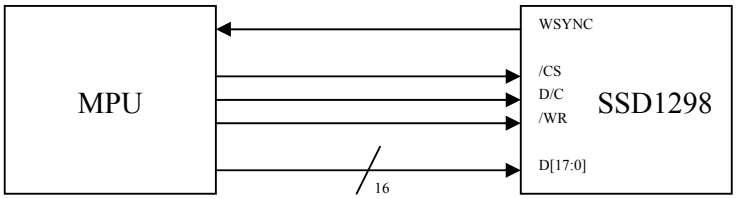
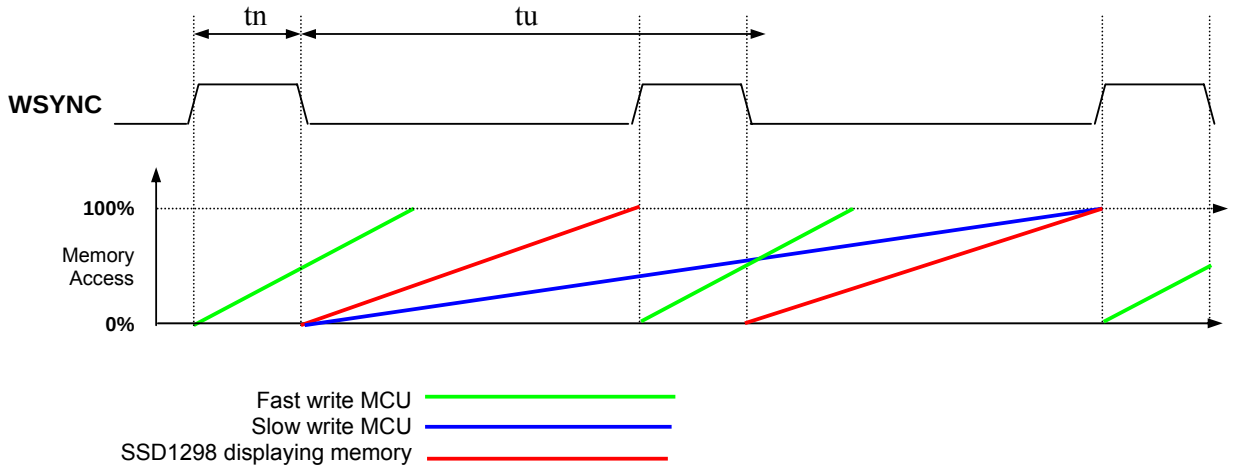
ENWS: When ENWS = 1, it enables WSYNC output pin. Mode1 or Mode2 is selected by WSMD. When ENWS = 0(POR), it disables WSYNC feature, the WSYNC output pin will be high-impedance.

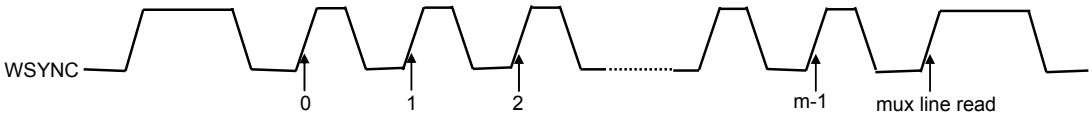


WSMD = 0 is **mode1**, the waveform of WSYNC output will be:



tn is the time when there is No Update of LCD screen from on-chip ram content.
tu is the time when the LCD screen is updating based on on-chip ram content.
e.g. fosc = 510KHz, for 320mux, tn = 282us (6 lines), tu =15.06ms (320 lines)

WSMD = 1 is **mode2**, the waveform of WSYNC output will be:



For fast write MCU: MCU should start to write new frame of ram data just after rising edge of long WSYNC pulse and should be finished well before the rising edge of the next long WSYNC pulse.
e.g. 5MHz 8 bit parallel write cycle for 18 bit color depth, or 3MHz 8 bit parallel write cycle for 16 bit color depth.

For slow write MCU (Half the write speed of fast write): MCU should start to write new frame ram data after the rising edge of the first short WSYNC pulse and must be finished within 2 frames time.
e.g. 2.5MHz 8 bit parallel write cycle for 18 bit color depth.
* Usually, **mode2** is for slower MCU, while **mode1** is for fast MCU.

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Power control 1 (R03h) (POR = 6864h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
POR		0	1	1	0	1	0	0	0	0	1	1	0	0	1	0	0

DCT[3:0]: Set the step-up cycle of the step-up circuit for 8-color mode (CM = V_{DDIO}). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline × 24
0	0	0	1	Fline × 16
0	0	1	0	Fline × 12
0	0	1	1	Fline × 8
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2
1	0	0	1	Fline × 1
1	0	1	0	fosc / 4
1	0	1	1	fosc / 6
1	1	0	0	fosc / 8
1	1	0	1	fosc / 10
1	1	1	0	fosc / 12
1	1	1	1	fosc / 16

* Fline = Line frequency
fosc = Internal oscillator frequency (~510KHz)

BT[2:0]: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used.

BT2	BT1	BT0	V_{GH} output	V_{GL} output	V_{GH} booster ratio	V_{GL} booster ratio
0	0	0	3 x V_{CIX2}	-(V_{GH}) + V_{CI}	+6	-5
0	0	1	3 x V_{CIX2}	-(V_{GH}) + V_{CIX2}	+6	-4
0	1	0	3 x V_{CIX2}	-(V_{CIX2})	+6	-2
0	1	1	2 x V_{CIX2} + V_{CI}	-(V_{GH})	+5	-5
1	0	0	2 x V_{CIX2} + V_{CI}	-(V_{GH}) + V_{CI}	+5	-4
1	0	1	2 x V_{CIX2} + V_{CI}	-(V_{GH}) + V_{Cix2}	+5	-3
1	1	0	2 x V_{CIX2}	-(V_{GH})	+4	-4
1	1	1	2 x V_{CIX2}	-(V_{GH}) + V_{CI}	+4	-3

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DC[3:0]: Set the step-up cycle of the step-up circuit for 262k-color mode (CM = V_{SS}). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline × 24
0	0	0	1	Fline × 16
0	0	1	0	Fline × 12
0	0	1	1	Fline × 8
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2
1	0	0	1	Fline × 1
1	0	1	0	fosc / 4
1	0	1	1	fosc / 6
1	1	0	0	fosc / 8
1	1	0	1	fosc / 10
1	1	1	0	fosc / 12
1	1	1	1	fosc / 16

* Fline = Line frequency
  fosc = Internal oscillator frequency (~510KHz)

AP[2:0]: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

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Display Control (R07h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PT[1:0]: Normalize the source outputs when non-displayed area of the partial display is driven.

VLE[2:1]: When VLE1 = 1 or VLE2 = 1, a vertical scroll is performed in the 1st screen by taking data VL17-0 in R41h register. When VLE1 = 1 and VLE2 = 1, a vertical scroll is performed in the 1st and 2nd screen by VL1[8:0] and VL2[8:0] respectively.

SPT: When SPT = "1", the 2-division LCD drive is performed.

CM: 8-color mode setting.
When CM = 1, 8-color mode is selected.
When CM = 0, 8-color mode is disable.

GON: Gate off level becomes VGH when GON = "0".

DTE: When GON = "1" and DTE = "0", all gate outputs become VGL. When GON = "1" and DTE = "1", selected gate wire becomes VGH, and non-selected gate wires become VGL.

D[1:0]: Display is on when D1 = "1" and off when D1 = "0". When off, the display data remains in the GDDRAM, and can be displayed instantly by setting D1 = "1". When D1= "0", the display is off with all of the source outputs set to the GND level. Because of this, the driver can control the charging current for the LCD with AC driving. When D[1:0] = "01", the internal display is performed although the display is off. When D[1:0] = "00", the internal display operation halts and the display is off. Control the display on/off while control GON and DTE.

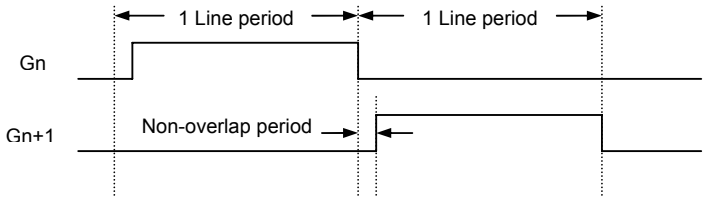
GON	DTE	D1	D0	Internal Display Operation	Source output	Gate output
0	0	0	0	Halt	GND	V_{GH}
0	0	0	1	Operation	GND	V_{GH}
1	0	0	1	Operation	GND	V_{GOFFL}
1	0	1	1	Operation	Grayscale level output	V_{GOFFL}
1	1	1	1	Operation	Grayscale level output	Selected gate line: V_{GH} Non-selected gate line: V_{GOFFL}

Frame Cycle Control (R0Bh) (POR = 5308h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
POR		0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0

NO[1:0]: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	reserved
0	1	1 clock cycle (POR)
1	0	2 clock cycle
1	1	3 clock cycle



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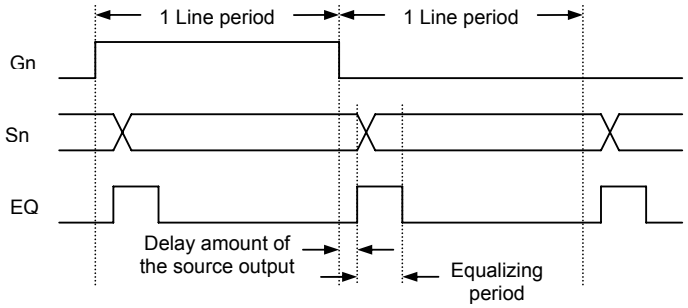
SDT[1:0]: Set delay amount from the gate output signal falling edge of the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	0 clock cycle
0	1	1 clock cycle (POR)
1	0	2 clock cycle
1	1	3 clock cycle

EQ[2:0]: Sets the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	2 clock cycle
0	1	0	3 clock cycle
0	1	1	4 clock cycle
1	0	0	5 clock cycle
1	0	1	6 clock cycle
1	1	0	7 clock cycle
1	1	1	8 clock cycle



DIV[1:0]: Set the division ratio of clocks for internal operation. Internal operations are driven by clocks which frequency is divided according to the DIV1-0 setting.

DIV1	DIV0	Division Ratio
0	0	1
0	1	2
1	0	4
1	1	8

* fosc = internal oscillator frequency, ~510kHz

SDIV: When SDIV = 1, DIV1-0 value will be count. When SDIV = 0, DIV1-0 value will be auto determined.

SRTN: When SRTN =1, RTN3-0 value will be count. When SRTN = 0, RTN3-0 value will be auto determined.

RTN[3:0]: Set the no. of clocks in each line. The total number will be the decimal value of RTN3-0 plus 16. e.g. if RTN3-0 = "1010h", the total number of clocks in each line = 10 +16 = 26 clocks.

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Frame frequency calculation

For DMode[1:0] = '00'

$$Frame\_frequency = \frac{Fosc}{div \times (rtn + 16) \times (mux + vbp + vfp + 3)}$$

where *Fosc* = internal oscillator frequency
div = Division ratio determined by DIV[1:0]
rtn = RTN[3:0]
mux = MUX[8:0]
vbp = VBP[7:0]
vfp = VFT[7:0]

for default values of SSD1298
Fosc = ~510KHz, DIV[1:0] = '00', RTN[3:0] = 8, MUX[8:0] = 319, VBP[7:0] = 3, VFP[7:0] = 1,

Frame frequency = $\frac{510K}{1 \times (8+16) \times (319+3+1+3)} = \frac{510K}{1 \times 24 \times 326} = 65Hz$

Power Control 2 (R0Ch) (POR = 0004h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

VRC[2:0]: Adjust VCIX2 output voltage. The adjusted level is indicated in the chart below VRC2-0 setting.

VRC2	VRC1	VRC0	VCIX2 voltage
0	0	0	5.1V
0	0	1	5.3V
0	1	0	5.5V
0	1	1	5.7V
1	0	0	5.9V
1	0	1	6.1V
1	1	0	Reserve
1	1	1	Reserve

Note: The above setting is valid when VCI has high enough voltage supply for boosting up the required voltage.
The above setting is assumed 100% booster efficiency. Please refer to DC Characteristics for detail.

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Power Control 3 (R0Dh) (POR = 0009h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
POR*		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

VRH[3:0]: Set amplitude magnification of V_{LCD63}. These bits amplify the V_{LCD63} voltage 1.78 to 3.00. times the Vref voltage set by VRH[3:0].

VRH3	VRH2	VRH1	VRH0	V_{LCD63} Voltage
0	0	0	0	Vref x 2.810
0	0	0	1	Vref x 2.900
0	0	1	0	Vref x 3.000
0	0	1	1	Vref x 1.780
0	1	0	0	Vref x 1.850
0	1	0	1	Vref x 1.930
0	1	1	0	Vref x 2.020
0	1	1	1	Vref x 2.090
1	0	0	0	Vref x 2.165
1	0	0	1	Vref x 2.245
1	0	1	0	Vref x 2.335
1	0	1	1	Vref x 2.400
1	1	0	0	Vref x 2.500
1	1	0	1	Vref x 2.570
1	1	1	0	Vref x 2.645
1	1	1	1	Vref x 2.725

*****Vref is the internal reference voltage equals to 2.0V.

Power Control 4 (R0Eh) (POR = 3200h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
POR*		0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

VcomG: When VcomG = "1", it is possible to set output voltage of VcomL to any level, and the instruction (VDV4-0) becomes available. When VcomG = "0", VcomL output is fixed to Hi-z level, VCIM output for VcomL power supply stops, and the instruction (VDV4-0) becomes unavailable. Set VcomG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV[4:0]: Set the alternating amplitudes of Vcom at the Vcom alternating drive. These bits amplify 0.6 to 1.23 times the VLCD63 voltage. When VcomG = "0", the settings become invalid. External voltage at VcomR is referenced when VDV = "01111".

VCOML = 0.9475*VCOMH - VCOMA

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom Amplitude
0	0	0	0	0	VLCD63 x 0.60
0	0	0	0	1	VLCD63 x 0.63
0	0	0	1	0	VLCD63 x 0.66
		: : :			: Step = 0.03 :
0	1	1	0	1	VLCD63 x 0.99
0	1	1	1	0	VLCD63 x 1.02
0	1	1	1	1	Reference from external variable resistor
1	0	0	0	0	VLCD63 x 1.05
1	0	0	0	1	VLCD63 x 1.08
		: : :			: Step = 0.03 :
1	0	1	0	1	VLCD63 x 1.20
1	0	1	1	0	VLCD63 x 1.23
1	0	1	1	1	Reserved
1	1	*	*	*	Reserved

Note: Vcom amplitude < 6V

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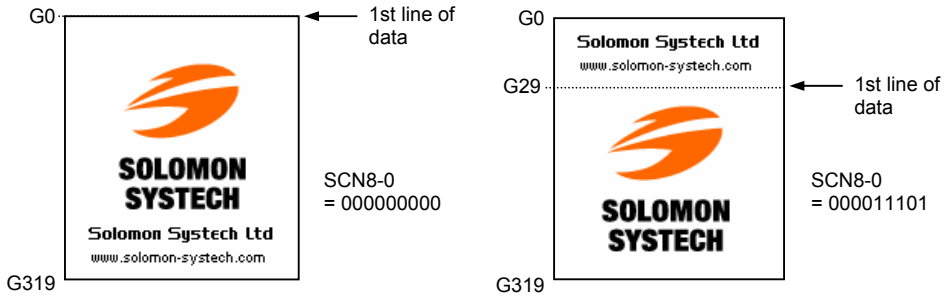
Gate Scan Position (R0Fh) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[8:0]: Set the scanning starting position of the gate driver. The valid range is from 0 to 319.



Sleep mode (R10h) (POR = 0001h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

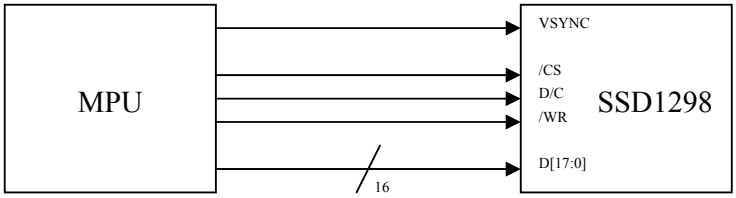
SLP: Sleep mode enable bit. In the sleep mode, the internal display operations are halted except the R-C oscillator to reduce current consumption. No change in the GDDRAM data or instructions during the sleep mode is made, although it is retained.

When SLP = 1, the driver enters into the sleep mode.
When SLP = 0, the driver leaves the sleep mode.

Entry Mode (R11h) (POR = 6230h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VSMode	DFM1	DFM0	0	DenMode	Wmode	Nosync	Dmode	TY1	TY0	ID1	ID0	AM	0	0	0
POR		0	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0

VSMode: When VSMode = 1 at DMode[1:0] = "00", the frame frequency will be dependent on VSYNC.



In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display oerpation speed + buffer), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the SSD1298 rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display. Therefore, the SSD1298 can write data via VSYNC interface in high speed with low power consumption.

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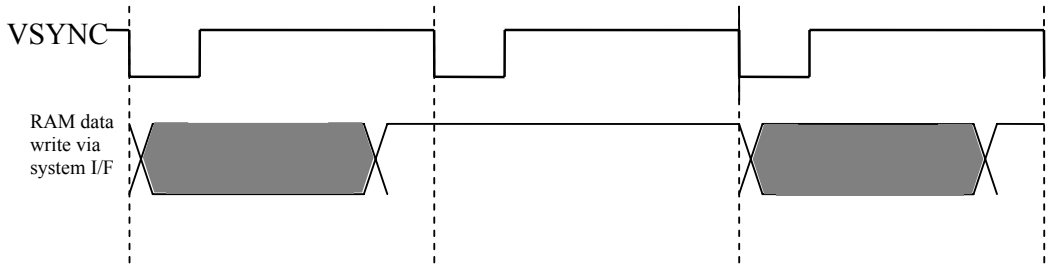

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$Fosc[Hz] = Frame\_frequency * (mux + vfp + vbp + 3) * (rtn + 16) * (div)$$

$$RAMWriteSpeed(min)[Hz] > \frac{240 * mux}{(vbp + mux - marginss) * (rtn + 16) * \frac{1}{fosc}}$$

where *Fosc* = internal oscillator frequency
div = Division ratio determined by DIV[1:0]
rtn = RTN[3:0]
mux = MUX[8:0]
vbp = VBP[7:0]
vfp = VFT[7:0]

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

DFM[1:0]: Set the color display mode.

DFM1	DFM0	Color mode
1	1	65k color (POR)
1	0	262k color

DenMode:

DenMode=1 : RGB interface ignore HSYNC, VSYNC pin and HBP, VBP
DenMode=0 : RGB interface control by HSYNC, VSYNC pin and HBP, VBP

When DenMode=1, Generic mode will write each input rgb pixel into RAM buffer, the window of ram buffer to be written defined by command R44h (define X of window)m R45h (define Y start),R46 (define Y end), whenever the input RGB dimension is larger than the defined ram window, it wont have any effect.

WMode:

WMode=1 : Write RAM from Generic RGB data (POR, if PS:00xx)
WMode=0 : Write RAM from SPI interface

Nosync:

Nosync=1 : Dmode change immediately
Nosync=0 : Dmode change Sync with on chip frame start

Dmode:

Dmode=1 : Display engine will be clocked by on chip oscillator and ignore DOTCLK pin
Dmode=0 : Display engine will be clocked by DOTCLK pin and onchip oscillator will be off (POR, if PS:00xx)

TY[1:0]: In 262k color mode, 16 bit parallel interface, there are three types of methods in writing data into the ram, Type A, B and C are described as below.

TY1	TY0	Writing mode
0	0	Type A
0	1	Type B

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1	0	Type C

			Hardware pins																
Interface	**Color mode**	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
16 bit	**262k Type A**	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	G4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x	
		3rd	G5	G4	G3	G2	G1	G0	x	x		B5	G4	B3	B2	B1	B0	x	x	
	262k Type B	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	x	x	x	x	x	x	x	x		B5	G4	B3	B2	B1	B0	x	x	
	262k Type C	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	G4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	

Remark : x Don't care bits

Not connected pins

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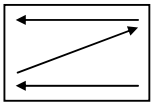
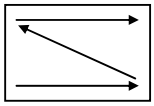
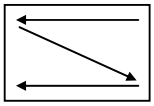
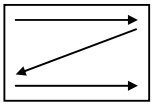
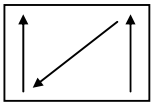
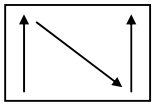
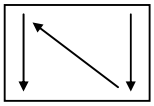
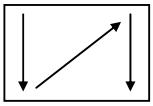
ID[1:0]: The address counter is automatically incremented by 1, after data are written to the GDDRAM when ID[1:0] = "1". The address counter is automatically decremented by 1, after data are written to the GDDRAM when ID[1:0] = "0". The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data are written to the GDDRAM is set with AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the GDDRAM. When AM = "0", the address counter is updated in the horizontal direction. When AM = "1", the address counter is updated in the vertical direction. When window addresses are selected, data are written to the GDDRAM area specified by the window addresses in the manner specified with ID1-0 and AM bits.

	ID[1:0]="00" Horizontal: decrement Vertical: decrement	ID[1:0]="01" Horizontal: increment Vertical: decrement	ID[1:0]="10" Horizontal: decrement Vertical: increment	ID[1:0]="11" Horizontal: increment Vertical: increment
AM="0" Horizontal	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh
AM="1" Vertical	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh

Generic Interface Control (R15h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	INVDOT	INVDEN	INVHS	INVVS
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

INVDOT: sets the signal polarity of DOTCLK pin. When INVDOT = 0, data is latched at positive edge of DOTCLK. When INVDOT = 1, data is latched at negative edge of DOTCLK.

INVDEN: sets the signal polarity of DEN pin. When INVDEN = 0, DEN is active high. When INVDEN = 1, DEN is active low.

INVHS: sets the signal polarity of HSYNC pin. When INVHS = 0, HSYNC is active low. When INVHS = 1, HSYNC is active high.

INVVS: sets the signal polarity of VSYNC pin. When INVVS = 0, VSYNC is active low. When INVVS = 1, VSYNC is active high.

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Power Control 5 (R1Eh) (POR = 0029h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
POR*		0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1

nOTP: nOTP equals to "0" after power on reset and VcomH voltage equals to programmed OTP value. When nOTP set to "1", setting of VCM[5:0] becomes valid and voltage of VcomH can be adjusted.

VCM[5:0]: Set the VcomH voltage if nOTP = "1". These bits amplify the VcomH voltage 0.35 to 0.99 times the VLCD63 voltage. Default value is "101001" when power on reset.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VcomH
0	0	0	0	0	0	VLCD63 x 0.35
0	0	0	0	0	1	VLCD63 x 0.36
:	:	:	:	:	:	: Step = 0.01 :
1	1	1	1	1	0	VLCD63 x 0.98
1	1	1	1	1	1	VLCD63 x 0.99

Write Data to GRAM (R22h)

R/W	DC	D[17:0]
W	1	WD[17:0] mapping depends on the interface setting

WD[17:0]: Transforms all the GDDRAM data into 18-bit, and writes the data. Format for transforming data into 18-bit depends on the interface used. SSD1298 selects the grayscale level according to the GDDRAM data. After writing data to GDDRAM, address is automatically updated according to AM bit and ID bit. Access to GDDRAM during stand-by mode is not available.

Read Data from GRAM (R22h)

R/W	DC	D[17:0]
R	1	RD[17:0] mapping depends on the interface setting

RD[17:0]: Read 18-bit data from the GDDRAM. When the data is read to the microcomputer, the first-word read immediately after the GDDRAM address setting is latched from the GDDRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal. When bit processing, such as a logical operation, is performed, only one read can be processed since the latched data in the first word is used.

Frame Frequency Control (R25h) (POR = 8000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
POR*		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OSC[3:0]: Set the frame frequency by OSC[3:0]

OSC[3:0]	Internal Oscillator Frequency (Hz)	Corresponding Frame Freq (Hz) (other registers are at POR value)
0000	390K	50
0010	430K	55
0101	470K	60
1000	510K	65
1010	548K	70
1100	587K	75
1110	626K	80

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Vcom OTP (R28h – R29h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R28h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R29h	W	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

When OTP is access, these registers must be set accordantly.

OTP programming sequence

<table>
<tr><th>Step</th><th>Operation</th></tr>
<tr><td>1</td><td>Power up the module at VCI = 2.7V, VDDIO = 1.8V.
Turn on the display as normal to 65k/262k color mode (displaying a test pattern if any).</td></tr>
<tr><td>2</td><td>Set nOTP to “1” (R1Eh) and optimizes VcomH by adjusting VCM[5:0] (R1Eh).</td></tr>
<tr><td>3</td><td>Power down the whole module.</td></tr>
<tr><td>4</td><td>Connect a supply to the module at VCI = 2.7V, VDDIO = 1.8V</td></tr>
<tr><td>5</td><td>Write below commands for OTP initialization and wait for 200ms for activate the OTP :
<table>
<tr><th>Index</th><th>Value</th></tr>
<tr><td>R00h</td><td>0x0001</td></tr>
<tr><td>R28h</td><td>0x0006</td></tr>
<tr><td>R29h</td><td>0x80C0</td></tr>
</table>
Connect a 14.5V supply to VGH through a current limiting resistor, see figure below.</td></tr>
<tr><td>6</td><td>Write the optimized value found in Step 2 to VCM[5:0] (R1Eh) and set nOTP to “1”.</td></tr>
<tr><td>7</td><td>Fire the OTP by write HEX code “000Ah” to register R28h.</td></tr>
<tr><td>8</td><td>Wait 500ms.</td></tr>
<tr><td>9</td><td>OTP complete. Power down the whole module and remove 14.5V supply.</td></tr>
</table>

Note: nOTP must set to “0” to activate the OTP effect.

Precaution:

1. All capacitors on OTP machine should be discharged completely before placing the LCD module.
2. The OTP programming voltage should not be applied when placing and removing the LCD module.
3. The OTP programming voltage should not be applied before VDDIO/VCI.
4. After OTP is finished, the capacitors at VGH and VCIX2 must be discharged completely before removing the LCD module.

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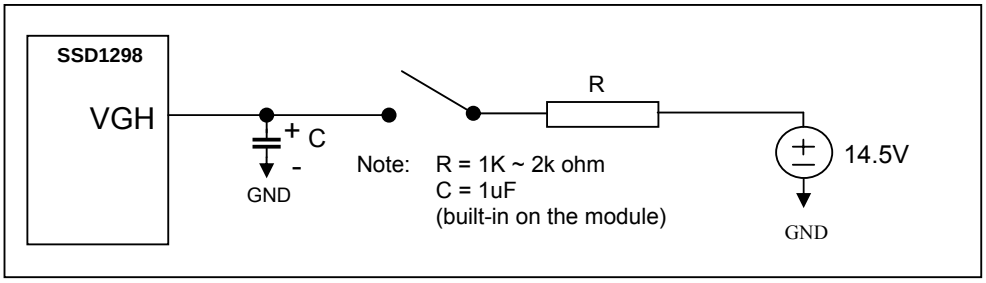
Figure 8-3 – OTP circuitry



Gamma Control (R30h to R3Bh)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30h	W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Note: please refer to table 5 for POR values.

PKP[52:00]: Gamma micro adjustment register for the positive polarity output

PRP[12:00]: Gradient adjustment register for the positive polarity output

VRP[14:00]: Adjustment register for amplification adjustment of the positive polarity output

PKN[52:00]: Gamma micro adjustment register for the negative polarity output

PRN[12:00]: Gradient adjustment register for the negative polarity output

VRN[14:00]: Adjustment register for the amplification adjustment of the negative polarity output.
(For details, see the Section 11 Gamma Adjustment Function).

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Vertical Scroll Control (R41h-R42h) (POR =0000h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R41h	W	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R42h	W	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VL1[8:0]: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the first to 320th can be scrolled for the number of the raster-row. After 320th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL1[8:0]) is valid when VLE1 = "1" or VLE2 = "1". The raster-row display is fixed when VLE[2:1] = "00".

VL2[8:0]: Specify scroll length at the scroll display for vertical smooth scrolling at 2nd screen. The display-start raster-row (VL2[8:0]) is valid when VLE1 = "1" and VLE2 = "1".

Horizontal RAM address position (R44h) (POR = EF00h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
POR		1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0

HSA[7:0]/HEA[7:0]: Specify the start/end positions of the window address in the horizontal direction by an address unit. Data are written to the GDDRAM within the area determined by the addresses specified by HEA[7:0] and HSA[7:0]. These addresses must be set before the RAM write. In setting these bits, make sure that "00"h ≤ HSA[7:0] ≤ HEA[7:0] ≤ "EF"h.

Vertical RAM address position (R45h-R46h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R45h	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
	POR		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

VSA[8:0]/VEA[8:0]: Specify the start/end positions of the window address in the vertical direction by an address unit. Data are written to the GRAM within the area determined by the addresses specified by VEA[8:0] and VSA[8:0]. These addresses must be set before the RAM write. In setting these bits, make sure that "00"h ≤ VSA[8:0] ≤ VEA[8:0] ≤ "13F"h.

1st Screen driving position (R48h-R49h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R48h	W	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	W	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	POR		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

SS1[8:0]: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the set gate driver, i.e. the first driving Gate is G0 if SS1[8:0] = 00H

SE1[8:0]: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the set gate driver. For instance, when SS1[8:0] = "07"H and SE1[8:0] = "10"H are set, the LCD driving is performed from G7 to G16, and non-selection driving is performed for G1 to G6, G17, and others. Ensure that SS1[8:0] ≤ SE1[8:0] ≤ 13FH.

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2nd Screen driving position (R4Ah-R4Bh)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R4Ah	W	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	W	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	POR		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

SS2[8:0]: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the set gate driver. The second screen is driven when SPT = "1".

SE2[8:0]: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the set gate driver. For instance, when SPT = "1", SS2[8:0] = "20"H, and SE2[8:0] = "2F"H are set, the LCD driving is performed from G32 to G47. Ensure that SS1[8:0] ≤ SE1[8:0] ; SS2[8:0] ≤ SE2[8:0] ≤ 13FH.

RAM address set (R4Eh-R4Fh)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R4Eh	W	1	0	0	0	0	0	0	0	0	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	W	1	0	0	0	0	0	0	0	YAD8	YAD7	YAD6	YAD5	YAD4	YAD 3	YAD 2	YAD 1	YAD 0
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

XAD[7:0]: Make initial settings for the GDDRAM X address in the address counter (AC).
YAD[8:0]: Make initial settings for the GDDRAM Y address in the address counter (AC).

After GDDRAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and setting for a new GDDRAM address is not required in the address counter. Therefore, data are written consecutively without setting an address. The address counter is not automatically updated when data are read out from the GDDRAM. GDDRAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses.

Optimize display performance and crosstalk mininmization (R20+R26+R27+R2E+R2F)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R20h	W	1	1	0	1	1	0	0	0	0	1	1	1	0	0	0	1	1
R26h	W	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R27h	W	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
R2Eh	W	1	0	1	1	1	1	1	1	0	0	1	0	0	0	1	0	1
R2Fh	W	1	0	0	0	1	0	0	1	0	1	1	1	0	1	0	1	1

R20h is to adjust Internal Vcom strength
R26h is to adjust Internal Bandgap strength
R27h is to adjust Internal VCOMH/VCOML timing
R2Eh is to adjust VCOM charge sharing time
R2Fh is to adjust Ram speed

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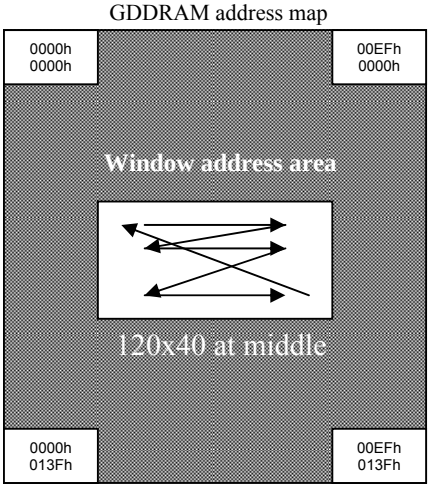
Window Address Function

The window address function enables writing display data sequentially in a window address area made in the internal GDDRAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and ID[1:0] bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the SSD1298 to write data including image data sequentially without taking the data wrap position into account. The window address area must be made within the GDDRAM address map area.

Condition:
00h ≤ HSA[7:0] ≤ HEA[7:0] ≤ EFh
00h ≤ VSA[8:0] ≤ VEA[8:0] ≤ 13Fh
AM and ID[1:0] refer to R11h

GDDRAM address map



Window address setting area:
HSA[7:0] = 3Bh; HEA[7:0] = B3h
VSA[8:0] = 8Bh; VEA[8:0] = B3h
AM = “0” and ID[1;]] = “11”

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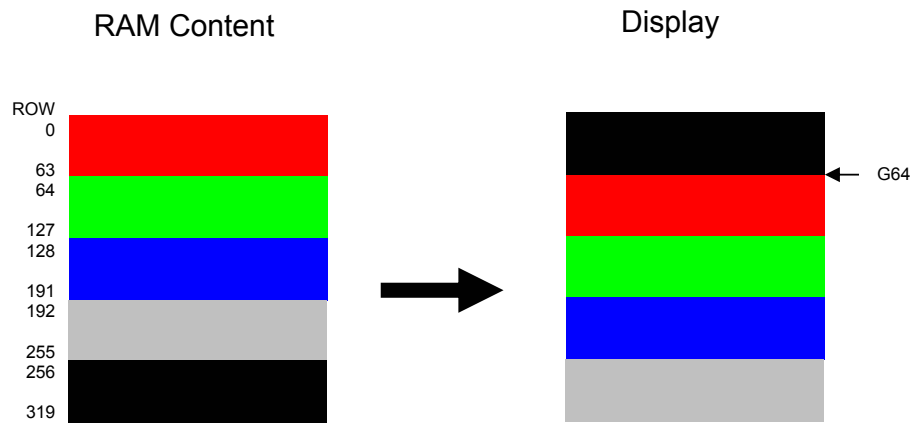
Partial Display and Scrolling Function

SSD1298 support schrolling and partial display function. The SSD2220 enables to selectively drive two screens at arbitrary positions with the screen-driving position registers (R48h to R4Bh). Only the lines required to display two screens at arbitrary positions are selectively driven.
The first screen driving position registers (R48 and R49) specifies the start line (SS18-10) and the end line (SE18-10) for displaying the first screen. The second screen driving position register (R4A) specifies the start line (SS28-20) and the end line (SE28-20) for displaying the second screen. The second screen control is effective when the SPT bit is set to 1. The total number of lines driven for displaying the first and second screens must be less than the number of lines to drive the LCD.

Scrolling Funtion: In Full screen display, schrolling could be enabled by setting VL1[8:0]

Example Register setting

Register	Value		Remark
R07h	0233h	MO=0, VLE2=0, VLE1=1, SPT=0	Enable schrolling by setting VLE1=1
R48h	0000h	SS1[8:0] = 0	
R49h	013Fh	SE1[8:0] = 319	
R4Ah	0000h	SS2[8:0] = 0	
R4Bh	013Fh	SE2[8:0] = 431	
R41h	0040h	VL1[8:0] = 64	Set scrolling amount
R42h	0000h	VL2[8:0] = 0	



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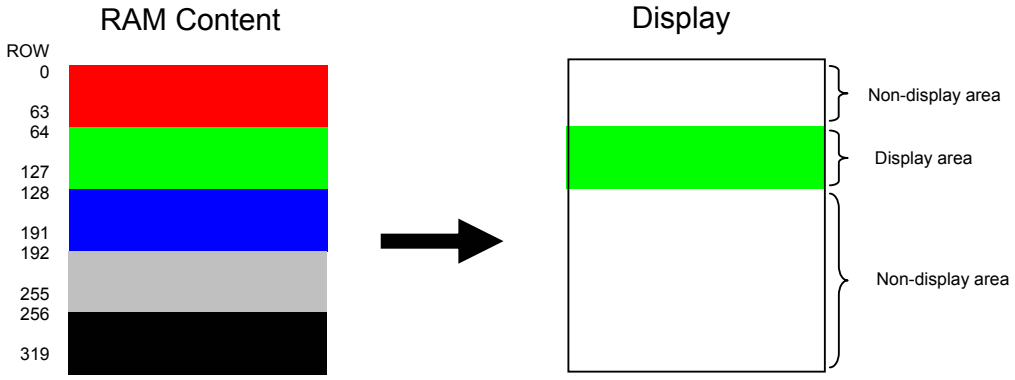
Partial display with one window:

Example Register setting

Register	Value		Remark
R07h	1833h	PT=11, VLE2=0, VLE1=0, SPT=0	Set PT=11 to set non-display to display data'1'
R48h	0040h	SS1[8:0] = 64	Define 1st display window
R49h	007Fh	SE1[8:0] = 127	
R4Ah	0000h	SS2[8:0] = 0	
R4Bh	013fh	SE2[8:0] = 319	
R41h	0000h	VL1[8:0] = 0	
R42h	0000h	VL2[8:0] = 0	



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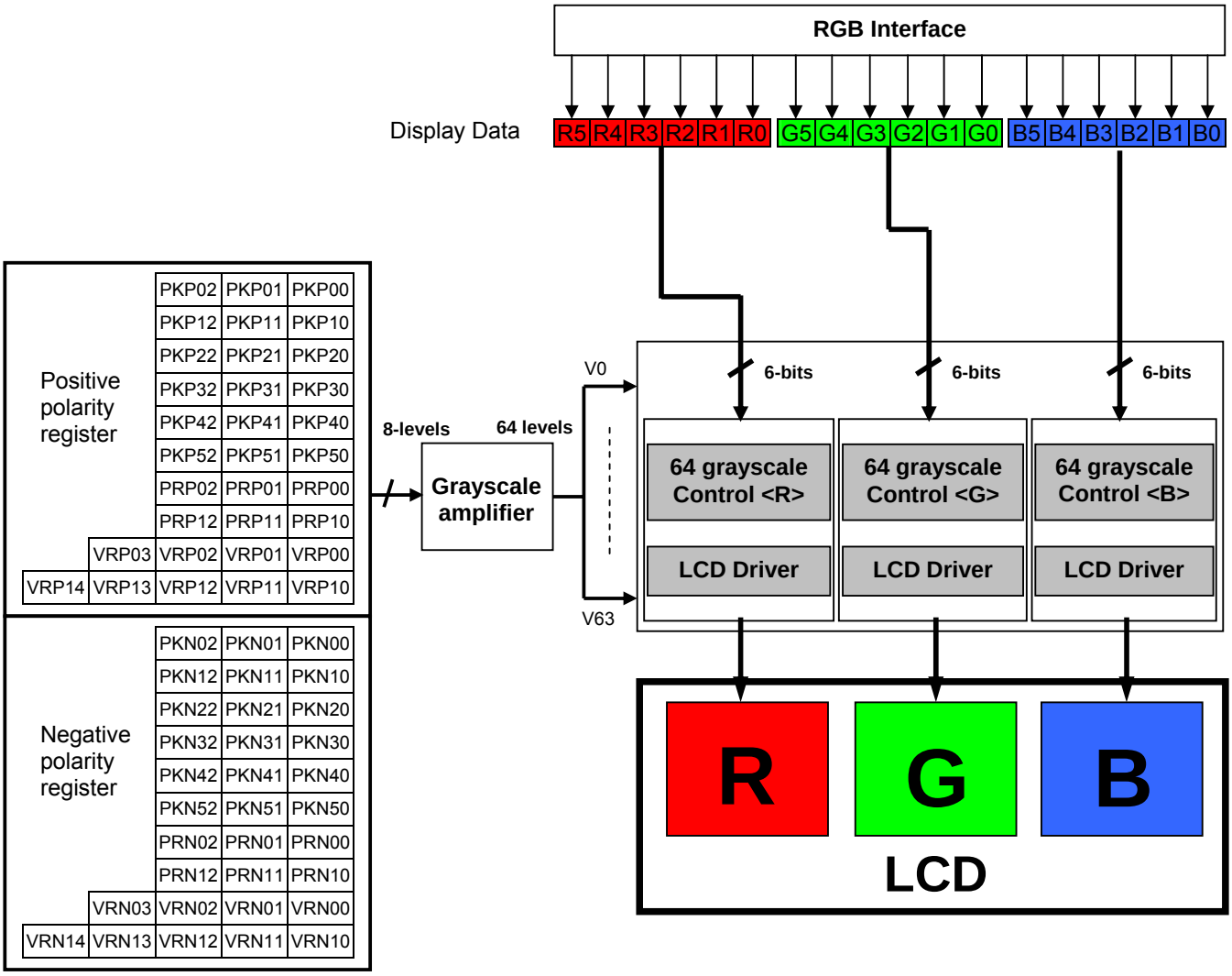
9 GAMMA ADJUSTMENT FUNCTION

The SSD1298 incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.



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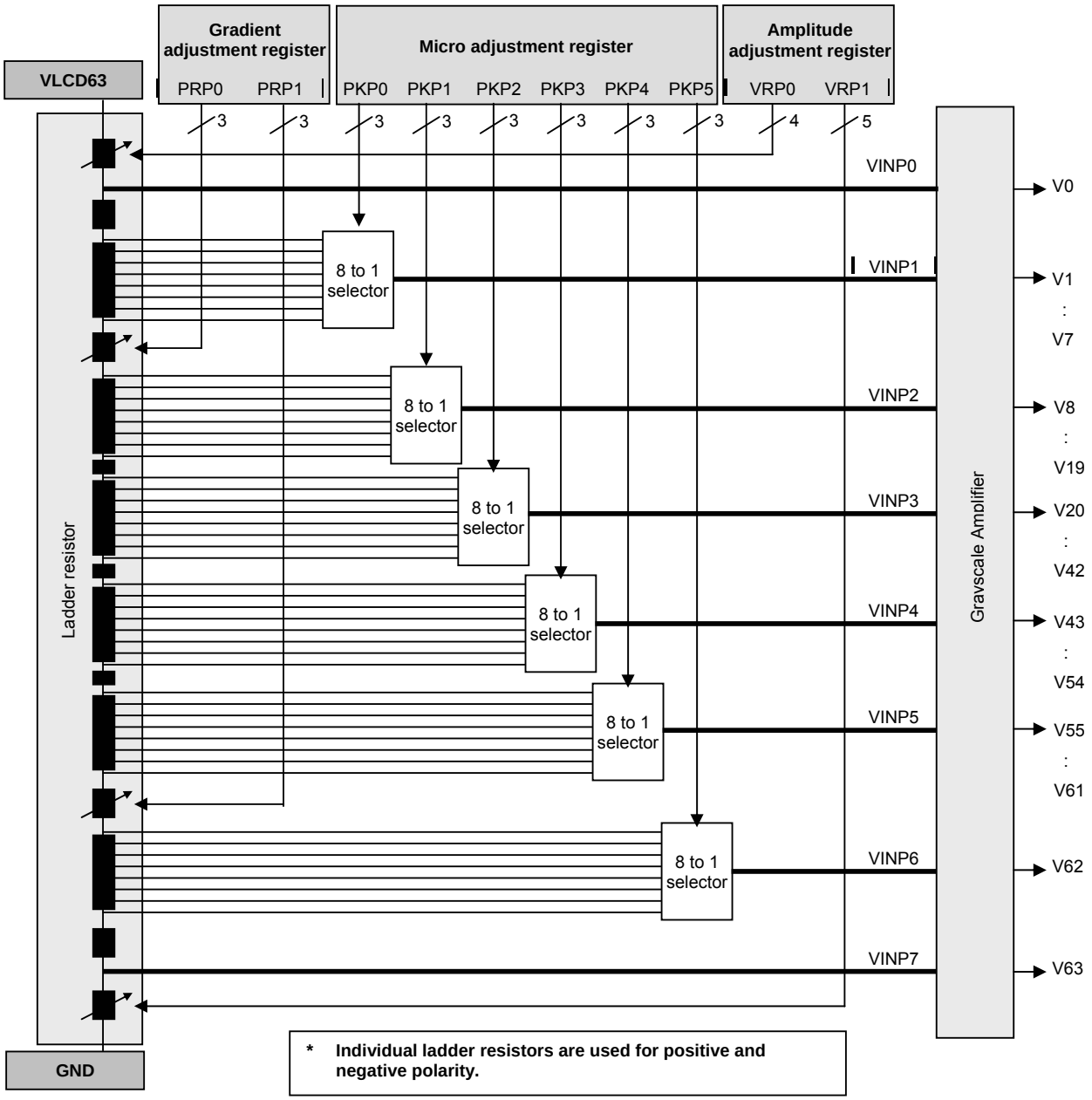
9.1 Structure of Grayscale Amplifier

Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.



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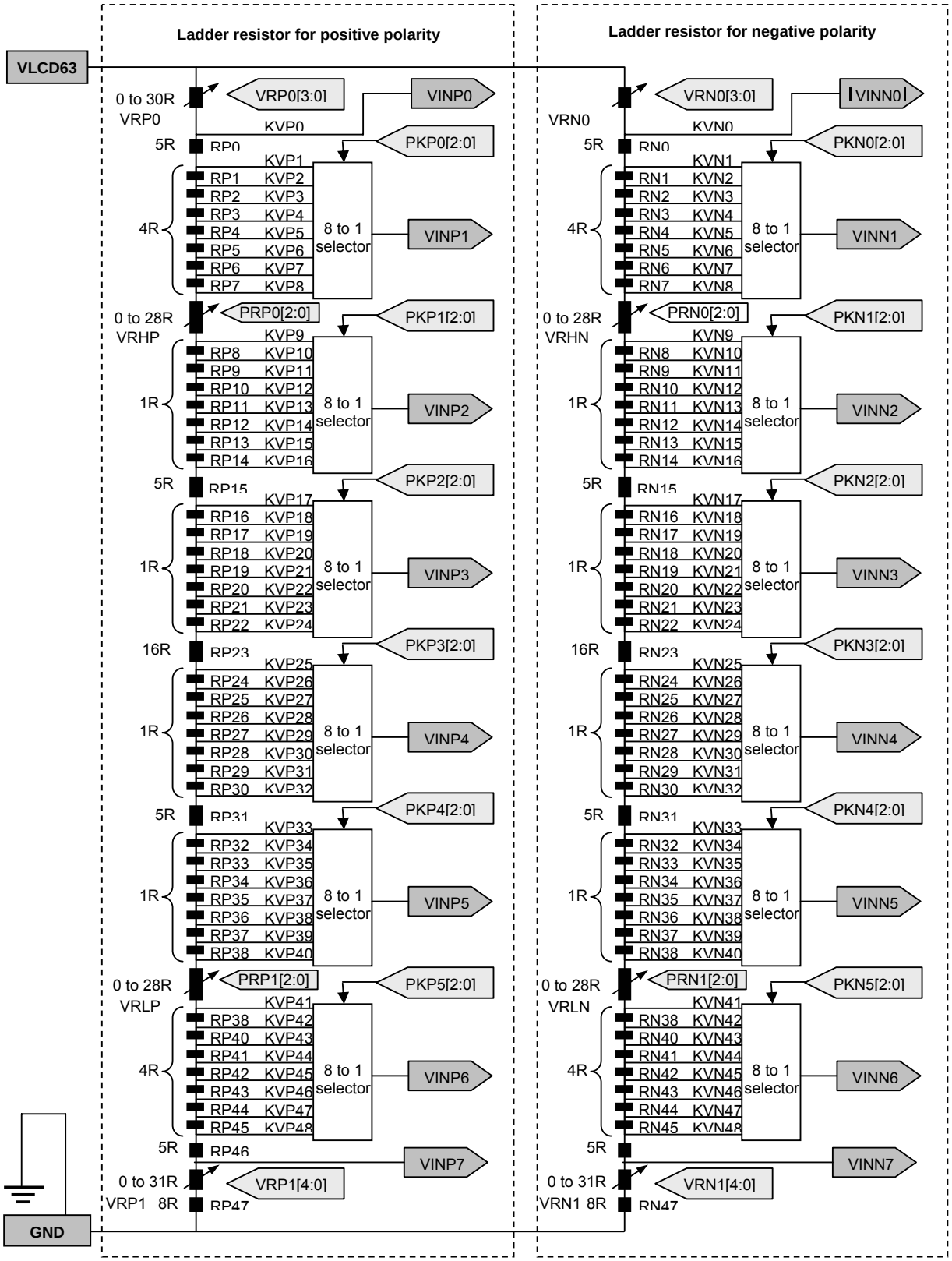

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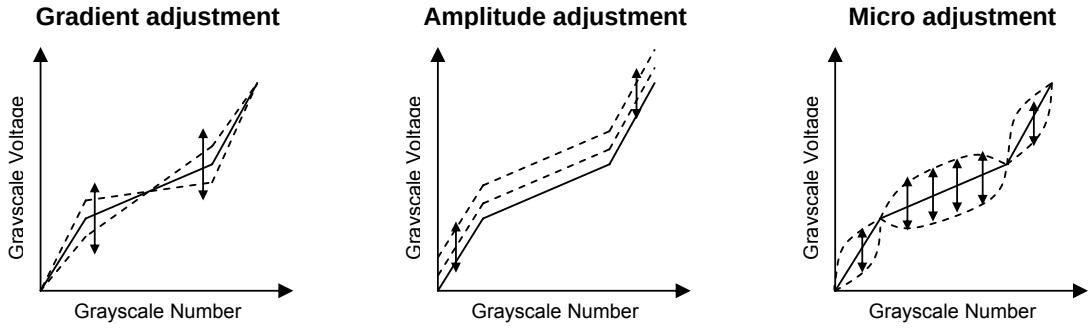
9.2 Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.



9.2.1 Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

9.2.2 Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

9.2.3 Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

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9.3 Ladder Resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

VRP(N)0	Resistance
0000	0R
0001	2R
0010	4R
: Step = 2R :	
1110	28R
1111	30R

VRP(N)1	Resistance
00000	0R
00001	1R
00010	2R
: Step = 1R :	
11110	30R
11111	31R

8 to 1 selecter

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Postive polarity							Negative polarity						
Registor PKP[2:0]	Selected voltage						Registor PKN[2:0]	Selected voltage					
	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6		VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Grayscale voltage	Formula	Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP(N)0	V22	V43+(V20-V43)*(21/23)	V44	V55+(V43-V55)*(22/24)
V1	VINP(N)1	V23	V43+(V20-V43)*(20/23)	V45	V55+(V43-V55)*(20/24)
V2	V8+(V1-V8)*(30/48)	V24	V43+(V20-V43)*(19/23)	V46	V55+(V43-V55)*(18/24)
V3	V8+(V1-V8)*(23/48)	V25	V43+(V20-V43)*(18/23)	V47	V55+(V43-V55)*(16/24)
V4	V8+(V1-V8)*(16/48)	V26	V43+(V20-V43)*(17/23)	V48	V55+(V43-V55)*(14/24)
V5	V8+(V1-V8)*(12/48)	V27	V43+(V20-V43)*(16/23)	V49	V55+(V43-V55)*(12/24)
V6	V8+(V1-V8)*(8/48)	V28	V43+(V20-V43)*(15/23)	V50	V55+(V43-V55)*(10/24)
V7	V8+(V1-V8)*(4/48)	V29	V43+(V20-V43)*(14/23)	V51	V55+(V43-V55)*(8/24)
V8	VINP(N)2	V30	V43+(V20-V43)*(13/23)	V52	V55+(V43-V55)*(6/24)
V9	V20+(V8-V20)*(22/24)	V31	V43+(V20-V43)*(12/23)	V53	V55+(V43-V55)*(4/24)
V10	V20+(V8-V20)*(20/24)	V32	V43+(V20-V43)*(11/23)	V54	V55+(V43-V55)*(2/24)
V11	V20+(V8-V20)*(18/24)	V33	V43+(V20-V43)*(10/23)	V55	VINP(N)5
V12	V20+(V8-V20)*(16/24)	V34	V43+(V20-V43)*(9/23)	V56	V62+(V55-V62)*(44/48)
V13	V20+(V8-V20)*(14/24)	V35	V43+(V20-V43)*(8/23)	V57	V62+(V55-V62)*(40/48)
V14	V20+(V8-V20)*(12/24)	V36	V43+(V20-V43)*(7/23)	V58	V62+(V55-V62)*(36/48)
V15	V20+(V8-V20)*(10/24)	V37	V43+(V20-V43)*(6/23)	V59	V62+(V55-V62)*(32/48)
V16	V20+(V8-V20)*(8/24)	V38	V43+(V20-V43)*(5/23)	V60	V62+(V55-V62)*(25/48)
V17	V20+(V8-V20)*(6/24)	V39	V43+(V20-V43)*(4/23)	V61	V62+(V55-V62)*(18/48)
V18	V20+(V8-V20)*(4/24)	V40	V43+(V20-V43)*(3/23)	V62	VINP(N)6
V19	V20+(V8-V20)*(2/24)	V41	V43+(V20-V43)*(2/23)	V63	VINP(N)7
V20	VINP(N)3	V42	V43+(V20-V43)*(1/23)		
V21	V43+(V20-V43)*(22/23)	V43	VINP(N)4		

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Reference voltage of positive polarity:

Reference	Formula	Micr0-adjusting rgister	Reference voltage
KVP0	VLCD63 - ΔV x VRP0 / SUMRP	--	VINP0
KVP1	VLCD63 - ΔV x (VRP0 + 5R) / SUMRP	PKP0[2:0] = “000”	VINP1
KVP2	VLCD63 - ΔV x (VRP0 + 9R) / SUMRP	PKP0[2:0] = “001”	
KVP3	VLCD63 - ΔV x (VRP0 + 13R) / SUMRP	PKP0[2:0] = “010”	
KVP4	VLCD63 - ΔV x (VRP0 + 17R) / SUMRP	PKP0[2:0] = “011”	
KVP5	VLCD63 - ΔV x (VRP0 + 21R) / SUMRP	PKP0[2:0] = “100”	
KVP6	VLCD63 - ΔV x (VRP0 + 25R) / SUMRP	PKP0[2:0] = “101”	
KVP7	VLCD63 - ΔV x (VRP0 + 29R) / SUMRP	PKP0[2:0] = “110”	
KVP8	VLCD63 - ΔV x (VRP0 + 33R) / SUMRP	PKP0[2:0] = “111”	
KVP9	VLCD63 - ΔV x (VRP0 + 33R + VRHP) / SUMRP	PKP1[2:0] = “000”	VINP2
KVP10	VLCD63 - ΔV x (VRP0 + 34R + VRHP) / SUMRP	PKP1[2:0] = “001”	
KVP11	VLCD63 - ΔV x (VRP0 + 35R + VRHP) / SUMRP	PKP1[2:0] = “010”	
KVP12	VLCD63 - ΔV x (VRP0 + 36R + VRHP) / SUMRP	PKP1[2:0] = “011”	
KVP13	VLCD63 - ΔV x (VRP0 + 37R + VRHP) / SUMRP	PKP1[2:0] = “100”	
KVP14	VLCD63 - ΔV x (VRP0 + 38R + VRHP) / SUMRP	PKP1[2:0] = “101”	
KVP15	VLCD63 - ΔV x (VRP0 + 39R + VRHP) / SUMRP	PKP1[2:0] = “110”	
KVP16	VLCD63 - ΔV x (VRP0 + 40R + VRHP) / SUMRP	PKP1[2:0] = “111”	
KVP17	VLCD63 - ΔV x (VRP0 + 45R + VRHP) / SUMRP	PKP2[2:0] = “000”	VINP3
KVP18	VLCD63 - ΔV x (VRP0 + 46R + VRHP) / SUMRP	PKP2[2:0] = “001”	
KVP19	VLCD63 - ΔV x (VRP0 + 47R + VRHP) / SUMRP	PKP2[2:0] = “010”	
KVP20	VLCD63 - ΔV x (VRP0 + 48R + VRHP) / SUMRP	PKP2[2:0] = “011”	
KVP21	VLCD63 - ΔV x (VRP0 + 49R + VRHP) / SUMRP	PKP2[2:0] = “100”	
KVP22	VLCD63 - ΔV x (VRP0 + 50R + VRHP) / SUMRP	PKP2[2:0] = “101”	
KVP23	VLCD63 - ΔV x (VRP0 + 51R + VRHP) / SUMRP	PKP2[2:0] = “110”	
KVP24	VLCD63 - ΔV x (VRP0 + 52R + VRHP) / SUMRP	PKP2[2:0] = “111”	
KVP25	VLCD63 - ΔV x (VRP0 + 68R + VRHP) / SUMRP	PKP3[2:0] = “000”	VINP4
KVP26	VLCD63 - ΔV x (VRP0 + 69R + VRHP) / SUMRP	PKP3[2:0] = “001”	
KVP27	VLCD63 - ΔV x (VRP0 + 70R + VRHP) / SUMRP	PKP3[2:0] = “010”	
KVP28	VLCD63 - ΔV x (VRP0 + 71R + VRHP) / SUMRP	PKP3[2:0] = “011”	
KVP29	VLCD63 - ΔV x (VRP0 + 72R + VRHP) / SUMRP	PKP3[2:0] = “100”	
KVP30	VLCD63 - ΔV x (VRP0 + 73R + VRHP) / SUMRP	PKP3[2:0] = “101”	
KVP31	VLCD63 - ΔV x (VRP0 + 74R + VRHP) / SUMRP	PKP3[2:0] = “110”	
KVP32	VLCD63 - ΔV x (VRP0 + 75R + VRHP) / SUMRP	PKP3[2:0] = “111”	
KVP33	VLCD63 - ΔV x (VRP0 + 80R + VRHP) / SUMRP	PKP4[2:0] = “000”	VINP5
KVP34	VLCD63 - ΔV x (VRP0 + 81R + VRHP) / SUMRP	PKP4[2:0] = “001”	
KVP35	VLCD63 - ΔV x (VRP0 + 82R + VRHP) / SUMRP	PKP4[2:0] = “010”	
KVP36	VLCD63 - ΔV x (VRP0 + 83R + VRHP) / SUMRP	PKP4[2:0] = “011”	
KVP37	VLCD63 - ΔV x (VRP0 + 84R + VRHP) / SUMRP	PKP4[2:0] = “100”	
KVP38	VLCD63 - ΔV x (VRP0 + 85R + VRHP) / SUMRP	PKP4[2:0] = “101”	
KVP39	VLCD63 - ΔV x (VRP0 + 86R + VRHP) / SUMRP	PKP4[2:0] = “110”	
KVP40	VLCD63 - ΔV x (VRP0 + 87R + VRHP) / SUMRP	PKP4[2:0] = “111”	
KVP41	VLCD63 - ΔV x (VRP0 + 87R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “000”	VINP6
KVP42	VLCD63 - ΔV x (VRP0 + 91R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “001”	
KVP43	VLCD63 - ΔV x (VRP0 + 95R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “010”	
KVP44	VLCD63 - ΔV x (VRP0 + 99R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “011”	
KVP45	VLCD63 - ΔV x (VRP0 + 103R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “100”	
KVP46	VLCD63 - ΔV x (VRP0 + 107R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “101”	
KVP47	VLCD63-ΔV x (VRP0 + 111R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “110”	
KVP48	VLCD63 - ΔV x (VRP0 + 115R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “111”	
KVP49	VLCD63 - ΔV x (VRP0 + 120R + VRHP + VRLP) / SUMRP	--	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1

ΔV: Voltage difference between VLCD63 and of GND.

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Reference voltage of negative polarity:

Reference	Formula	Micr0-adjusting rgister	Reference voltage
KVN0	VLCD63 - ΔV x VRN0 / SUMRN	--	VINN0
KVN1	VLCD63 - ΔV x (VRN0 + 5R) / SUMRN	PKN0[2:0] = “000”	VINN1
KVN2	VLCD63 - ΔV x (VRN0 + 9R) / SUMRN	PKN0[2:0] = “001”	
KVN3	VLCD63 - ΔV x (VRN0 + 13R) / SUMRN	PKN0[2:0] = “010”	
KVN4	VLCD63 - ΔV x (VRN0 + 17R) / SUMRN	PKN0[2:0] = “011”	
KVN5	VLCD63 - ΔV x (VRN0 + 21R) / SUMRN	PKN0[2:0] = “100”	
KVN6	VLCD63 - ΔV x (VRN0 + 25R) / SUMRN	PKN0[2:0] = “101”	
KVN7	VLCD63 - ΔV x (VRN0 + 29R) / SUMRN	PKN0[2:0] = “110”	
KVN8	VLCD63 - ΔV x (VRN0 + 33R) / SUMRN	PKN0[2:0] = “111”	
KVN9	VLCD63 - ΔV x (VRN0 + 33R + VRHN) / SUMRN	PKN1[2:0] = “000”	VINN2
KVN10	VLCD63 - ΔV x (VRN0 + 34R + VRHN) / SUMRN	PKN1[2:0] = “001”	
KVN11	VLCD63 - ΔV x (VRN0 + 35R + VRHN) / SUMRN	PKN1[2:0] = “010”	
KVN12	VLCD63 - ΔV x (VRN0 + 36R + VRHN) / SUMRN	PKN1[2:0] = “011”	
KVN13	VLCD63 - ΔV x (VRN0 + 37R + VRHN) / SUMRN	PKN1[2:0] = “100”	
KVN14	VLCD63 - ΔV x (VRN0 + 38R + VRHN) / SUMRN	PKN1[2:0] = “101”	
KVN15	VLCD63 - ΔV x (VRN0 + 39R + VRHN) / SUMRN	PKN1[2:0] = “110”	
KVN16	VLCD63 - ΔV x (VRN0 + 40R + VRHN) / SUMRN	PKN1[2:0] = “111”	
KVN17	VLCD63 - ΔV x (VRN0 + 45R + VRHN) / SUMRN	PKN2[2:0] = “000”	VINN3
KVN18	VLCD63 - ΔV x (VRN0 + 46R + VRHN) / SUMRN	PKN2[2:0] = “001”	
KVN19	VLCD63 - ΔV x (VRN0 + 47R + VRHN) / SUMRN	PKN2[2:0] = “010”	
KVN20	VLCD63 - ΔV x (VRN0 + 48R + VRHN) / SUMRN	PKN2[2:0] = “011”	
KVN21	VLCD63 - ΔV x (VRN0 + 49R + VRHN) / SUMRN	PKN2[2:0] = “100”	
KVN22	VLCD63 - ΔV x (VRN0 + 50R + VRHN) / SUMRN	PKN2[2:0] = “101”	
KVN23	VLCD63 - ΔV x (VRN0 + 51R + VRHN) / SUMRN	PKN2[2:0] = “110”	
KVN24	VLCD63 - ΔV x (VRN0 + 52R + VRHN) / SUMRN	PKN2[2:0] = “111”	
KVN25	VLCD63 - ΔV x (VRN0 + 68R + VRHN) / SUMRN	PKN3[2:0] = “000”	VINN4
KVN26	VLCD63 - ΔV x (VRN0 + 69R + VRHN) / SUMRN	PKN3[2:0] = “001”	
KVN27	VLCD63 - ΔV x (VRN0 + 70R + VRHN) / SUMRN	PKN3[2:0] = “010”	
KVN28	VLCD63 - ΔV x (VRN0 + 71R + VRHN) / SUMRN	PKN3[2:0] = “011”	
KVN29	VLCD63 - ΔV x (VRN0 + 72R + VRHN) / SUMRN	PKN3[2:0] = “100”	
KVN30	VLCD63 - ΔV x (VRN0 + 73R + VRHN) / SUMRN	PKN3[2:0] = “101”	
KVN31	VLCD63 - ΔV x (VRN0 + 74R + VRHN) / SUMRN	PKN3[2:0] = “110”	
KVN32	VLCD63 - ΔV x (VRN0 + 75R + VRHN) / SUMRN	PKN3[2:0] = “111”	
KVN33	VLCD63 - ΔV x (VRN0 + 80R + VRHN) / SUMRN	PKN4[2:0] = “000”	VINN5
KVN34	VLCD63 - ΔV x (VRN0 + 81R + VRHN) / SUMRN	PKN4[2:0] = “001”	
KVN35	VLCD63 - ΔV x (VRN0 + 82R + VRHN) / SUMRN	PKN4[2:0] = “010”	
KVN36	VLCD63 - ΔV x (VRN0 + 83R + VRHN) / SUMRN	PKN4[2:0] = “011”	
KVN37	VLCD63 - ΔV x (VRN0 + 84R + VRHN) / SUMRN	PKN4[2:0] = “100”	
KVN38	VLCD63 - ΔV x (VRN0 + 85R + VRHN) / SUMRN	PKN4[2:0] = “101”	
KVN39	VLCD63 - ΔV x (VRN0 + 86R + VRHN) / SUMRN	PKN4[2:0] = “110”	
KVN40	VLCD63 - ΔV x (VRN0 + 87R + VRHN) / SUMRN	PKN4[2:0] = “111”	
KVN41	VLCD63 - ΔV x (VRN0 + 87R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “000”	VINN6
KVN42	VLCD63 - ΔV x (VRN0 + 91R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “001”	
KVN43	VLCD63 - ΔV x (VRN0 + 95R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “010”	
KVN44	VLCD63 - ΔV x (VRN0 + 99R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “011”	
KVN45	VLCD63 - ΔV x (VRN0 + 103R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “100”	
KVN46	VLCD63 - ΔV x (VRN0 + 107R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “101”	
KVN47	VLCD63-ΔV x (VRN0 + 111R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “110”	
KVN48	VLCD63 - ΔV x (VRN0 + 115R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “111”	
KVN49	VLCD63 - ΔV x (VRN0 + 120R + VRHN + VRLN) / SUMRN	--	VINN7

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1

ΔV: Voltage difference between VLCD63 and of GND.

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10 MAXIMUM RATINGS

Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
VDDIO	Supply Voltage	-0.3 to +4.0	V
VCI	Input Voltage	VSS - 0.3 to 5.0	V
I	Current Drain Per Pin Excluding V_{DDIO} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, strong electric fields, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices. It is advised that proper precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI and Vout be constrained to the range VSS < VDDIO ≤ VCI < V_{OUT}. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 1.65 to 3.6V, T_A = -40 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.4	-	3.6	V
VCIR	Regulator power supply for logic device	Recommend Operating Voltage Possible Operating Voltage	2.5	-	3.6	V
VCI	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO whichever is higher	-	3.6	V
VGH	Gate driver High Output Voltage Booster efficiency	No panel loading; 4x or 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	88	90	-	%
		No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	82	84	-	%
VCIX2	VCIX2 primary booster efficiency	No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	83	85	-	%
VGH	Gate driver High Output Voltage		9	-	18	V
VGL	Gate driver Low Output Voltage		-15	-	-6	V
VcomH	Vcom High Output Voltage		V_{CI} + 0.5	-	5	V
VcomL	Vcom Low Output Voltage		-V_{CIM}+0.5	-	-1	V
VLCD63	Max. Source Voltage		-	-	6	V
ΔVLCD63	Source voltage variation		-2		2	%
V_{OH1}	Logic High Output Voltage	Iout=-100μA	0.9* VDDIO	-	VDDIO	V
V_{OL1}	Logic Low Output Voltage	Iout=100μA	0	-	0.1*VDDIO	V
V_{IH1}	Logic High Input voltage		0.8*VDDIO	-	VDDIO	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*VDDIO	V
I_{OH}	Logic High Output Current Source	Vout = V_{DDIO}-0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	μA

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I_{IL}/I_{IH}	Logic Input Current			-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance			-	5	7.5	pF
R_{SON}	Source drivers output resistance			-	1	-	kΩ
R_{GON}	Gate drivers output resistance			-	500	-	Ω
R_{CON}	Vcom output resistance			-	200	-	Ω
I_{dp}(262k)	Display current for 262k	Vddi1o = 1.8V, Vci = 2.8V. 5x/-5x booster ratio. Full color current consumption, without panel loading	Ivdd	-	150	500	uA
			Ivci	-	2.5	8	mA
I_{dp}(8 color)	Display current for 8 color mode	Current consumption for 8 color partial display, without panel loading	Ivdd	-	120	500	µA
			Ivci	-	1	5	mA
I_{slp}	Sleep mode current	Oscillator off, no source/gate output, Ram read write halt. Send command R10-0001 (sleep mode), R00-0000 (stop osc)	Ivdd	-	30	100	µA
			Ivci	-	40	200	µA

Remark: Ivci(total) = Ivci + Ivcir

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12 AC CHARACTERISTICS

Table 12-1 – Parallel 6800 Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	1000	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Data Setup Time	5	-	-	ns
t_{DHW}	Data Hold Time	5	-	-	ns
t_{ACC}	Data Access Time	250	-	-	ns
t_{OH}	Output Hold time	100	-	-	ns
$PWCS_L$	Pulse width /CS low (write cycle)	50	-	-	ns
$PWCS_H$	Pulse width /CS high (write cycle)	50	-	-	ns
$PWCS_L$	Pulse width /CS low (read cycle)	500	-	-	ns
$PWCS_H$	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

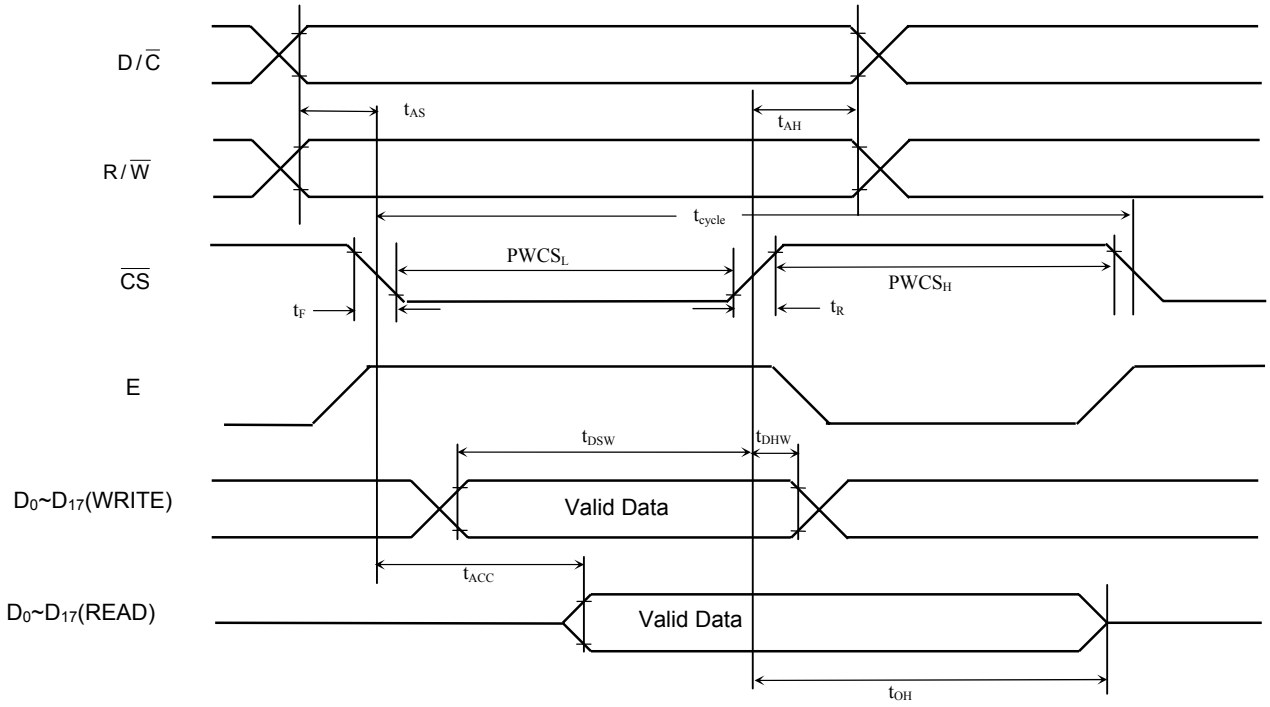

Figure 12-1 –Parallel 6800-series Interface Timing Characteristics

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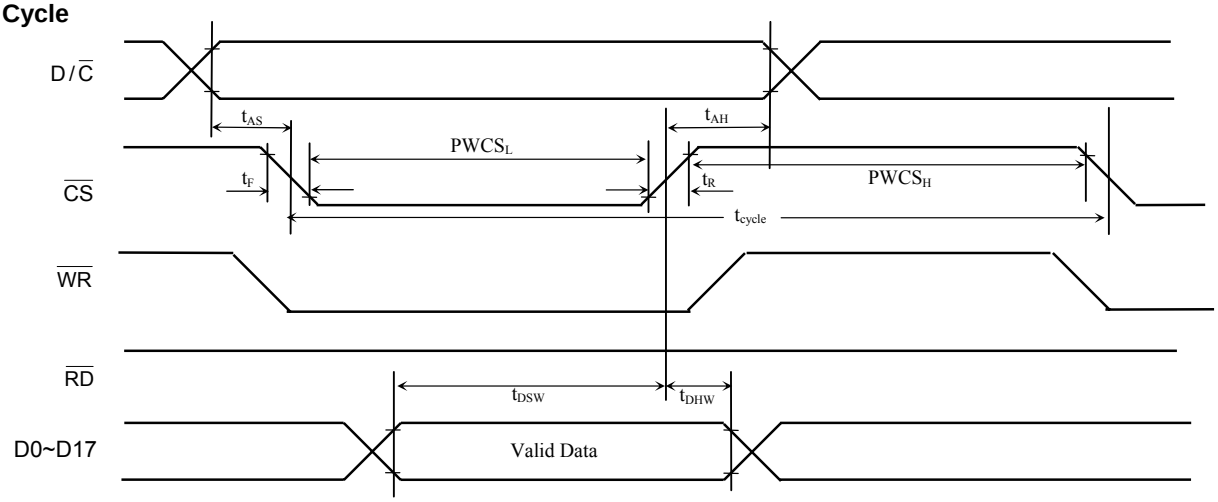
Table 12-2 – Parallel 8080 Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.65V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	1000	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Data Setup Time	5	-	-	ns
t_{DHW}	Data Hold Time	5	-	-	ns
t_{ACC}	Data Access Time	250	-	-	ns
t_{OH}	Output Hold time	100	-	-	ns
$PWCS_L$	Pulse Width /CS low (write cycle)	50	-	-	ns
$PWCS_H$	Pulse Width /CS high (write cycle)	50	-	-	ns
$PWCS_L$	Pulse Width /CS low (read cycle)	500	-	-	ns
$PWCS_H$	Pulse Width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Write Cycle



Read Cycle

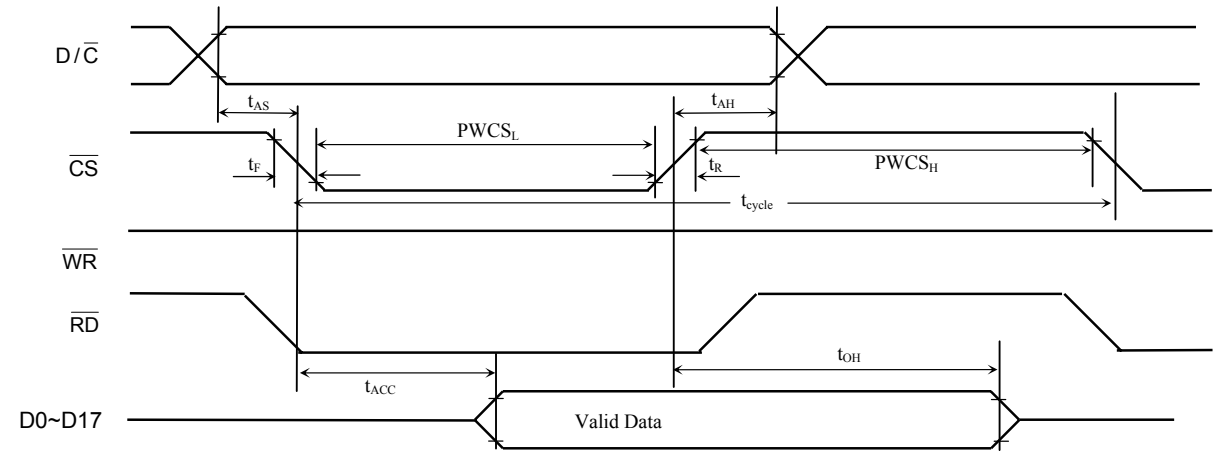


Figure 12-2 –Parallel 8080-series Interface Timing Characteristics

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Table 12-3 - Serial Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.65V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	13	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

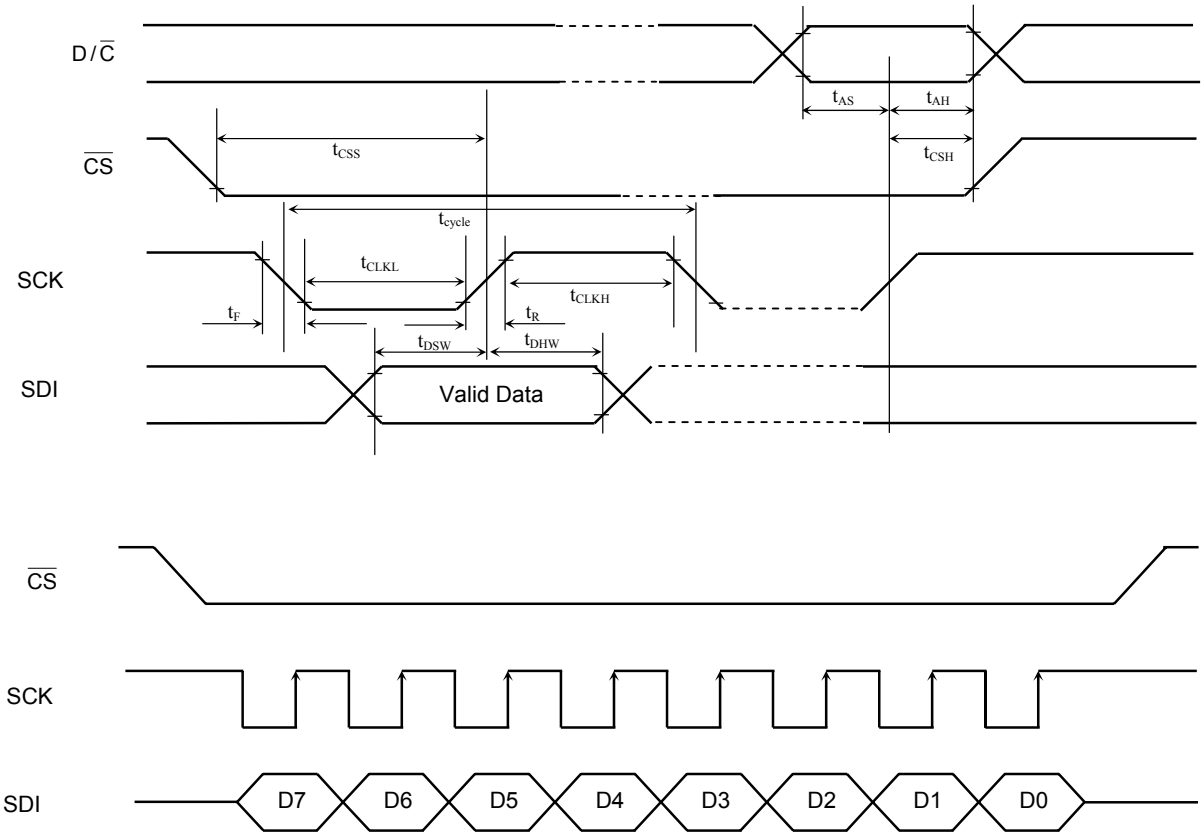

Figure 12-3 – 4 wire Serial Timing Characteristics

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Table 12-4 - RGB Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.65V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
f_{DOTCLK}	DOTCLK Frequency	-	2.64	3.95	MHz
t_{DOTCLK}	DOTCLK Period	253	379	-	ns
t_{VSYS}	Vertical Sync Setup Time	30	-	-	ns
t_{VSYH}	Vertical Sync Hold Time	30	-	-	ns
t_{HSYS}	Horizontal Sync Setup Time	30	-	-	ns
t_{HSYH}	Horizontal Sync Hold Time	30	-	-	ns
t_{HV}	Phase difference of Sync Signal Falling Edge	0	-	176	tDOT CLK
t_{CLK}	DOTCLK Low Period	126	-	-	ns
t_{CKH}	DOTCLK High Period	126	-	-	ns
t_{DS}	Data Setup Time	40	-	-	ns
t_{DH}	Data hold Time	40	-	-	ns
t_{RES}	Reset pulse width	10			ns

Note: External clock source must be provided to DOTCLK pin of SSD1298. The driver will not operate in absence of the clocking signal.

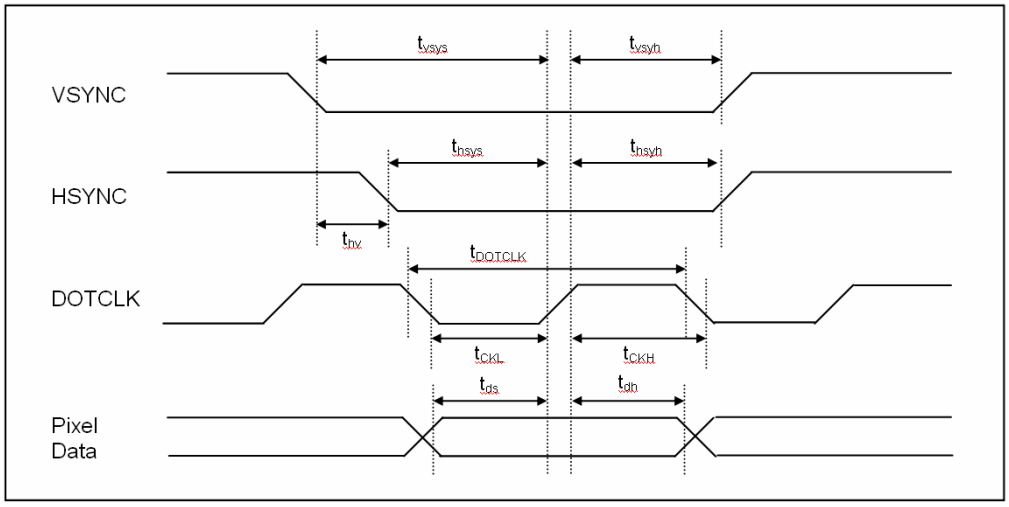

Figure 0-4 – RGB Timing Characteristics

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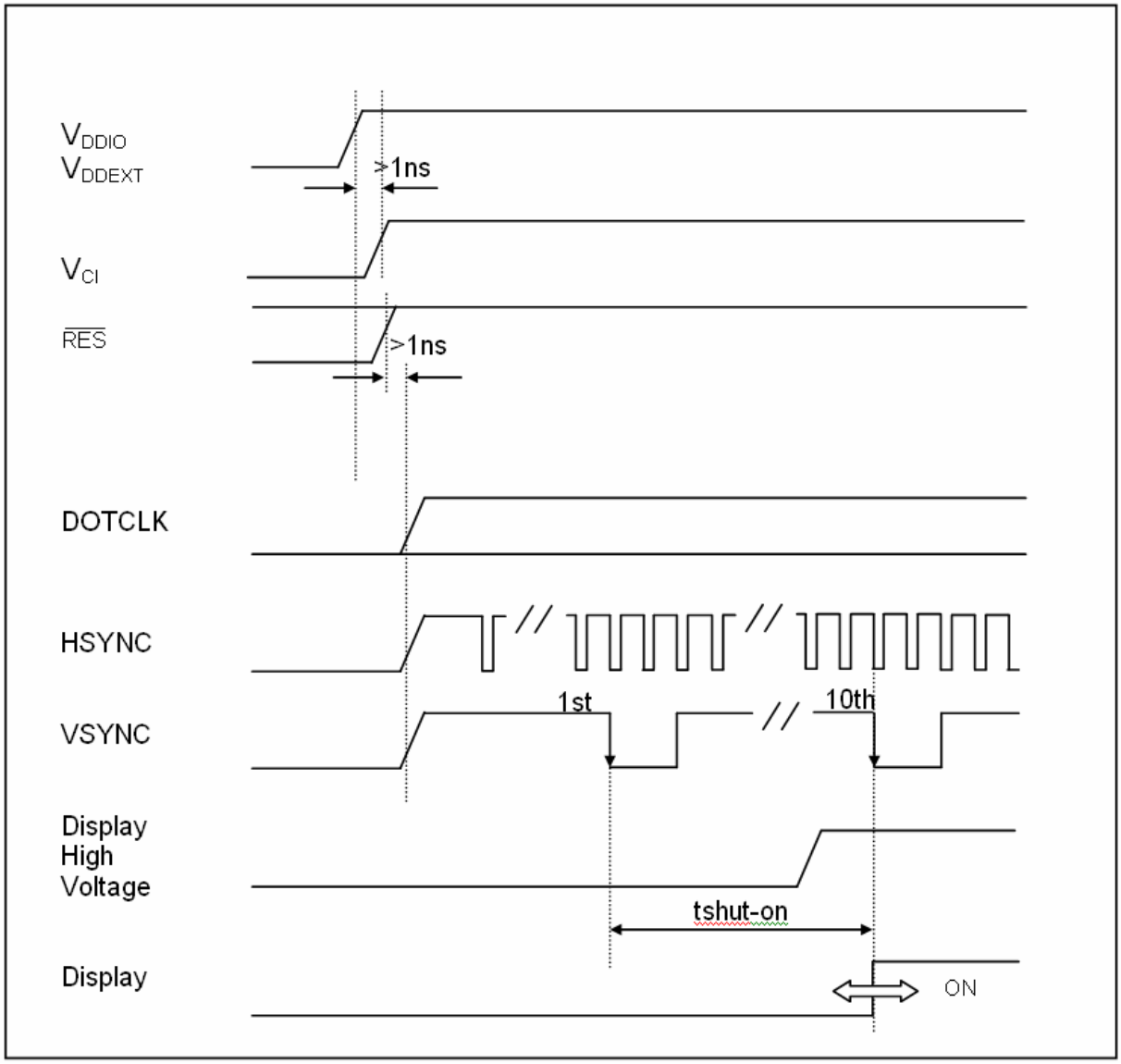

Figure 12-5 - Power Up Sequence

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GDDRAM ADDRESS

	RL=1	S0	S1	S2	S3	S4	S5	S6	S7	S8	…	S714	S715	S716	S717	S718	S719	
	RL=0	S719	S718	S717	S716	S715	S714	S713	S712	S711	…	S5	S4	S3	S2	S1	S0	
	BGR=0	R	G	B	R	G	B	R	G	B	…	R	G	B	R	G	B	Vertical address
	BGR=1	B	G	R	B	G	R	B	G	R	…	B	G	R	B	G	R	
TB=1	TB=0																	
G0	G319	0000H,0000H			0000H, 0001H			0000H, 0010H			…	0000H, 00EEH			0000H, 00EFH			0
G1	G318	0001H,0000H			0001H, 0001H			0001H, 0010H			…	0001H, 00EEH			0001H, 00EFH			1
G2	G317	0010H,0000H			0010H, 0001H			0010H, 0010H			…	0010H, 00EEH			0010H, 00EFH			2
G3	G316	0011H,0000H			0011H, 0001H			0011H, 0010H			…	0011H, 00EEH			0011H, 00EFH			3
G4	G315	0100H,0000H			0100H, 0001H			0100H, 0010H			…	0100H, 00EEH			0100H, 00EFH			4
. . .	. . .	. . .			. . .			. . .			. . .	. . .			. . .			. . .
G316	G3	013CH, 0000H			013CH, 0001H			013CH, 0010H			…	013CH, 00EEH			013CH, 00EFH			316
G317	G2	013DH, 0000H			013DH, 0001H			013DH, 0010H			…	013DH, 00EEH			013DH, 00EFH			317
G318	G1	013EH, 0000H			013EH, 0001H			013EH, 0010H			…	013EH, 00EEH			013EH, 00EFH			318
G319	G0	013FH, 0000H			013FH, 0001H			013FH, 0010H			…	013FH, 00EEH			013FH, 00EFH			319

Horizontal address	0	1	2	…	238	239

Remark : The address is in 00xxH,0yyyH format, where yyy is the vertical address and xx is the horizontal address

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13 INTERFACE MAPPING

13.1 Interface Setting

Table 13-1: Interface setting and data bus setting

PS3	PS2	PS1	PS0	Interface Mode	Data bus input	Data bus output
0	0	0	0	16-bit 6800 parallel interface	D[17:10], D[8:1]	D[17:10], D[8:1]
0	0	0	1	8-bit 6800 parallel interface	D[17:10]	D[8:1]
0	0	1	0	16-bit 8080 parallel interface	D[17:10], D[8:1]	D[17:10], D[8:1]
0	0	1	1	8-bit 8080 parallel interface	D[17:10]	D[8:1]
1	0	1	0	18-bits 8080 parallel interface	D[17:0]	D[17:0]
1	0	1	1	9-bits 8080 parallel interface	D[17:9]	D[8:0]
1	0	0	0	18-bits 6800 parallel interface	D[17:0]	D[17:0]
1	0	0	1	9-bits 6800 parallel interface	D[17:9]	D[8:0]

13.1.1 6800-series System Bus Interface

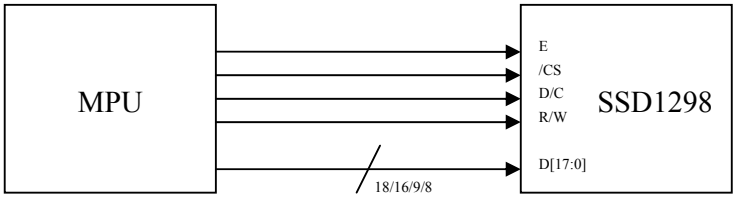

Table 13-2 – The Function of 6800-series parallel interface

PS3	PS2	PS1	PS0	Interface Mode	Data bus	R/W	E	D/C	/CS	Operation
0	0	0	0	16-bit 6800 parallel interface	D[17:10], D[8:1]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 16-bit display data
0	0	0	1	8-bit 6800 parallel interface	D[8:1] D[17:10]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 8-bit display data
1	0	0	0	18-bits 6800 parallel interface	D[17:0]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 18-bit display data
1	0	0	1	9-bits 6800 parallel interface	D[8:0] D[17:9]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 9-bit display data

* A dummy read is required before the first actual display data read

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13.1.2 8080-series System Bus Interface

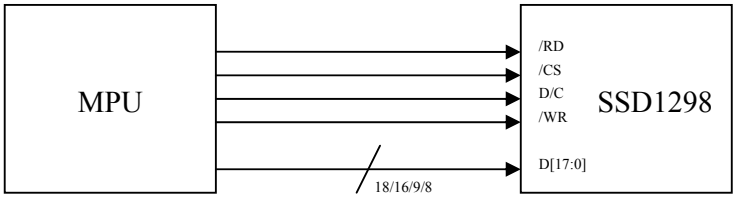

Table 13-3 – The Function of 8080-series parallel interface

PS3	PS2	PS1	PS0	Interface Mode	Data bus	/WR	/RD	D/C	/CS	Operation
0	0	1	0	16-bit 8080 parallel interface	D[17:10], D[8:1]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 16-bit display data
0	0	1	1	8-bit 8080 parallel interface	D[8:1]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
					D[17:10]	0	1	0	0	Write 8-bit command
						0	1	1	0	Write 8-bit display data
1	0	1	0	18-bit 8080 parallel interface	D[17:0]	0	1	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 18-bit display data
1	0	1	1	9-bit 8080 parallel interface	D[8:0]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
					D[17:9]	0	1	0	0	Write 8-bit command
						0	1	1	0	Write 9-bit display data

* A dummy read is required before the first actual display data read

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13.2 Mapping for Writing an Instruction

		Hardware pins																	
Interface	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x
16 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8		IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
9 bits	1st	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x									
	2nd	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x									
8 bits	1st	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8										
	2nd	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0										

Remark : x Don't care bits
Not connected pins

13.3 Mapping for Writing Pixel Data

			Hardware pins																
Interface	**Color mode**	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18 bits	**262k**		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits	**262k**	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	B4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x	
		3rd	G5	G4	G3	G2	G1	G0	x	x		B5	B4	B3	B2	B1	B0	x	x	
		1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	x	x	x	x	x	x	x	x		B5	B4	B3	B2	B1	B0	x	x	
		1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	B4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	
	65k		R4	R3	R2	R1	R0	G5	G4	G3		G2	G1	G0	B4	B3	B2	B1	B0	
9 bits	**262k**	1st	R5	R4	R3	R2	R1	R0	G5	G4	G3									
		2nd	G2	G1	G0	B5	B4	B3	B2	B1	B0									
8 bits	**262k**	1st	R5	R4	R3	R2	R1	R0	x	x										
		2nd	G5	G4	G3	G2	G1	G0	x	x										
		3rd	B5	B4	B3	B2	B1	B0	x	x										
	65k	1st	R4	R3	R2	R1	R0	G5	G4	G3										
		2nd	G2	G1	G0	B4	B3	B2	B1	B0										

Remark : x Don't care bits
Not connected pins

13.4 Mapping for Writing Pixel Data in generic mode

Interface	**Color mode**	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18-bit RGB	**262k**	-	RR5	RR4	RR3	RR2	RR1	RR0	GG5	GG4	GG3	GG2	GG1	GG0	BB5	BB4	BB3	BB2	BB1	BB0
16-bit RGB	**65k**	-	RR4	RR3	RR2	RR1	RR0	RR4	GG5	GG4	GG3	GG2	GG1	GG0	BB4	BB3	BB2	BB1	BB0	BB4
9-bit RGB	**262k**	1st	-	-	-	-	-	-	-	-	-	RR5	RR4	RR3	RR2	RR1	RR0	GG5	GG4	GG3
		2nd	-	-	-	-	-	-	-	-	-	BB5	BB4	BB3	BB2	BB1	BB0	GG2	GG1	GG0
6-bit RGB	**262k**	1st	-	-	-	-	-	-	-	-	-	RR5	RR4	RR3	RR2	RR1	RR0			
		2nd	-	-	-	-	-	-	-	-	-	GG5	GG4	GG3	GG2	GG1	GG0			
		3rd										BB5	BB4	BB3	BB2	BB1	BB0			

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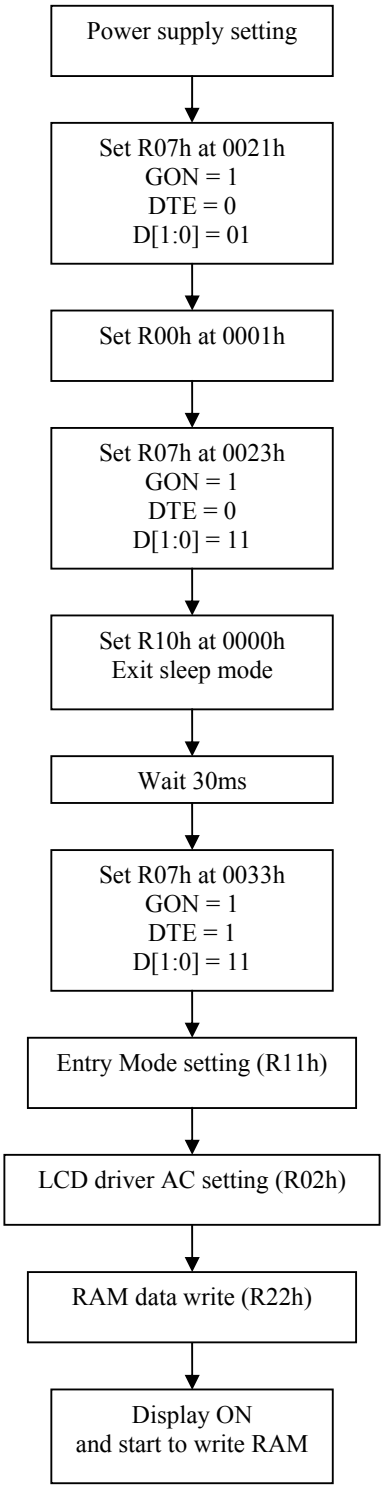
14 DISPLAY SETTING SEQUENCE

14.1 Display ON Sequence



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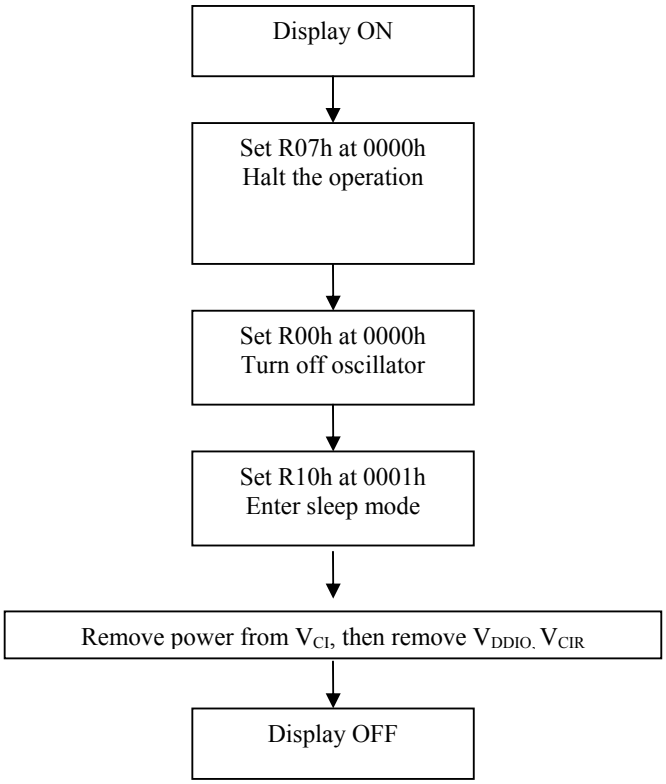
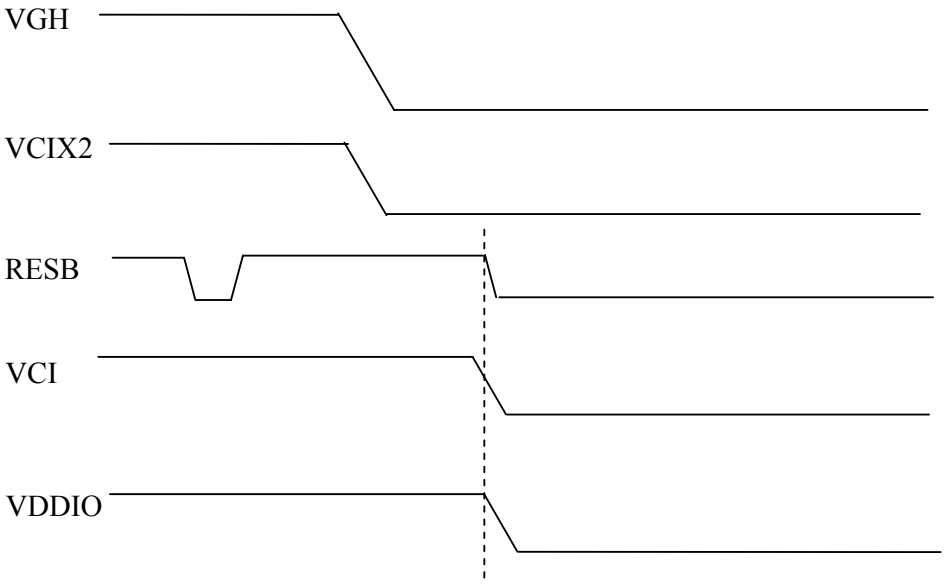
14.2 Display OFF Sequence





Note:
1. VDDIO should be the last to fall, or VCI/VDDIO could be power off at the same time
2. If OTP is active in the application, the MTP programming voltage should be turned off and capacitors at VGH and VCIX2 discharged before VCI/VDDIO are turned off.

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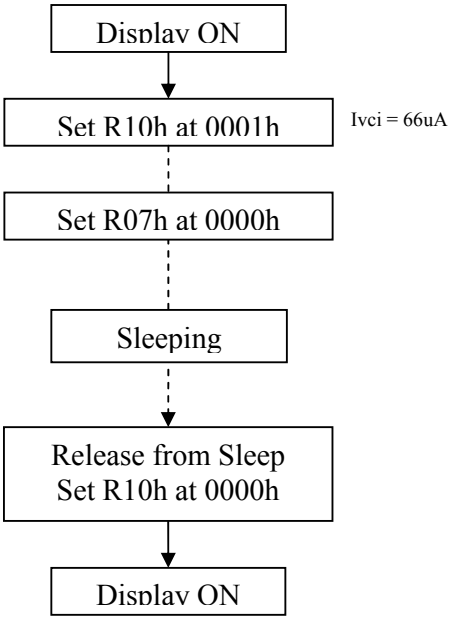
14.3 Sleep Mode Display Sequence



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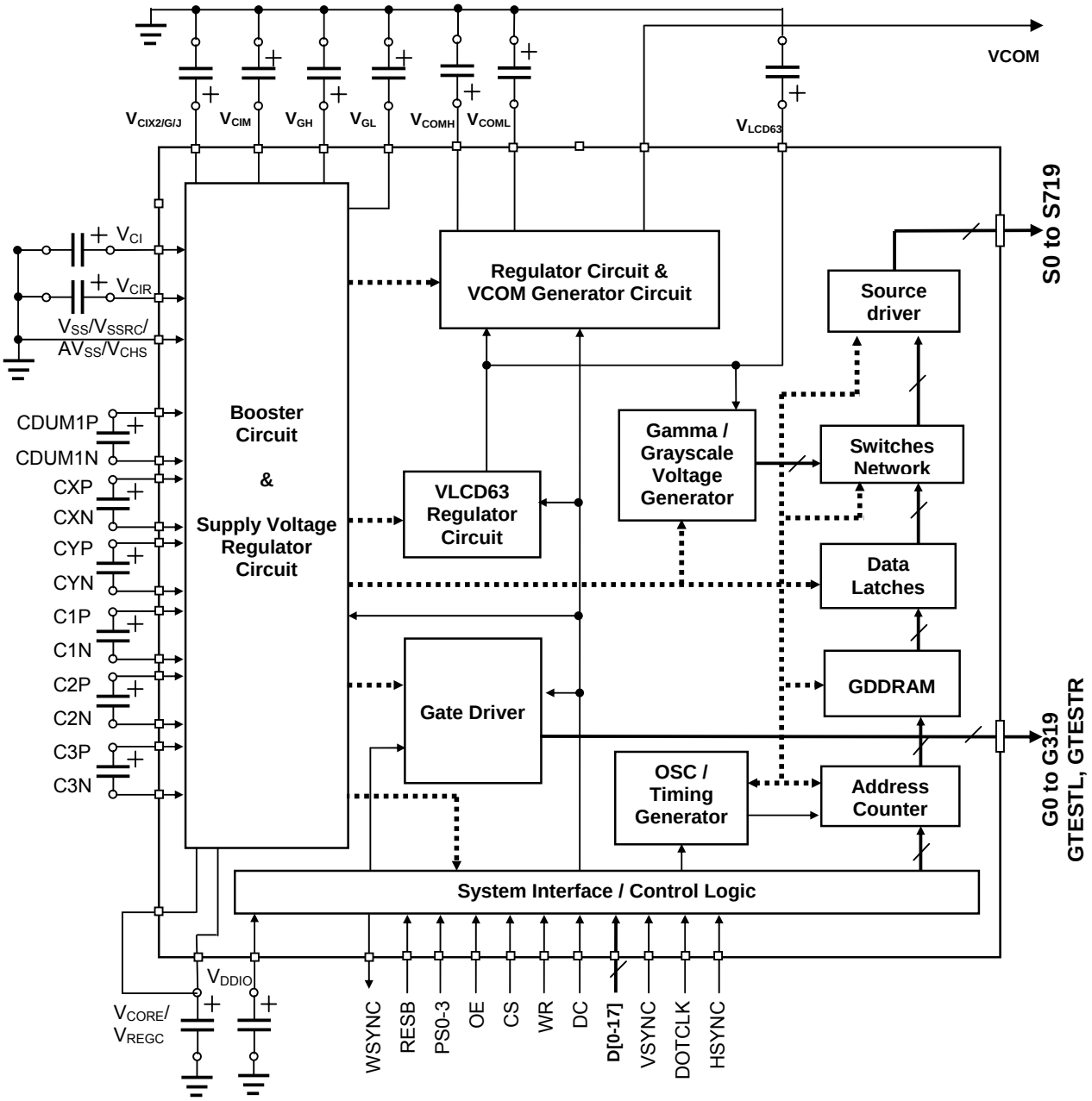
15 POWER SUPPLY BLOCK DIAGRAM



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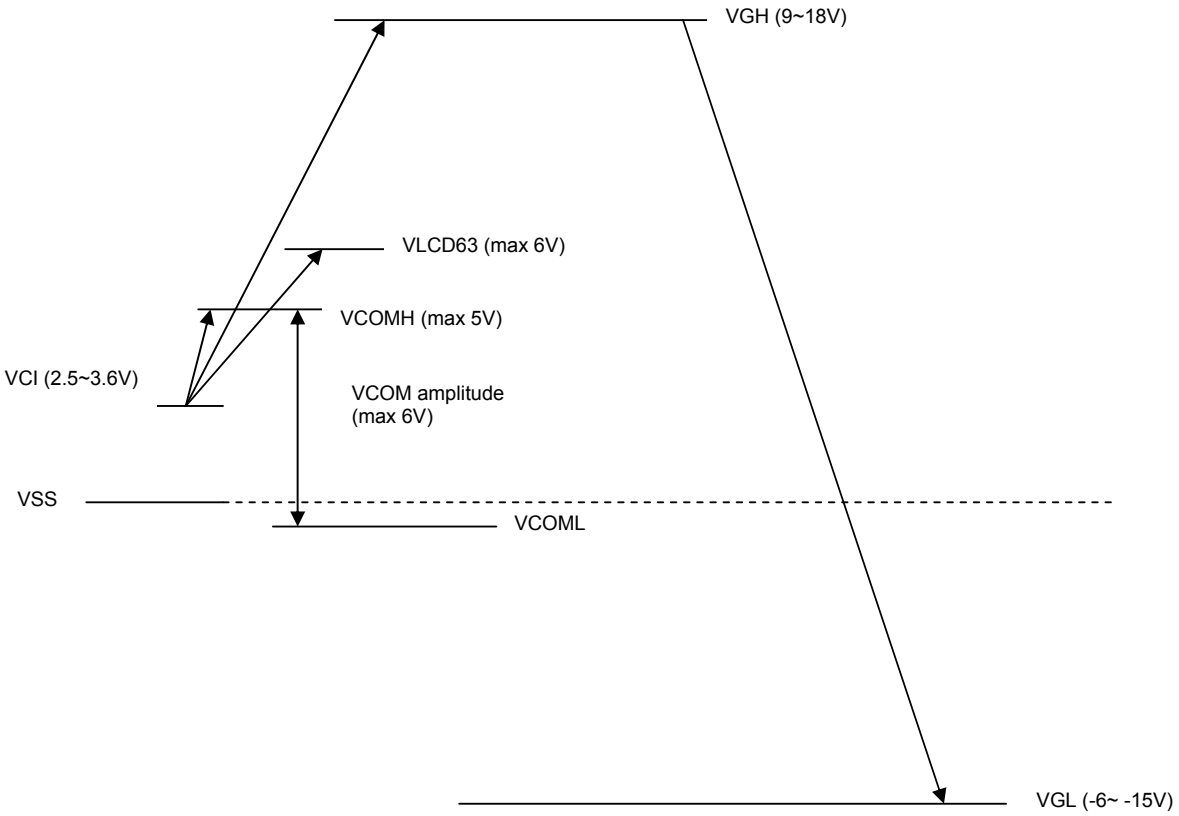
16 SSD1298 OUTPUT VOLTAGE RELATIONSHIP



Note: VGH-VGL<30V_{p-p}

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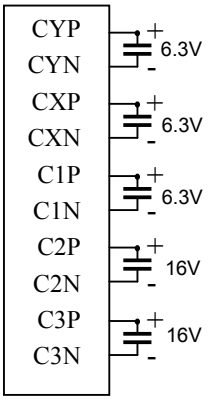
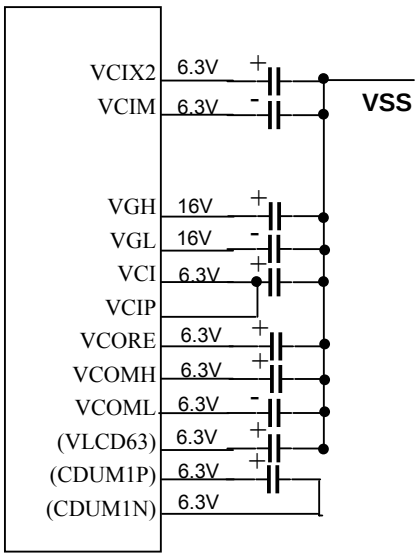
19Application Circuit

Figure 16-1: Booster Capacitors



All capacitors
0.1 ~ 0.22uF (0.22uF for better stability)

Figure 16-2 : Filtering and Charge Sharing Capacitors



Mandatory requirement on external components for SSD1298 is 13 capacitors.
VCIX2, VCIM, VGH, VGL, VCI, VCORE, VCOMH, VCOML
C1P/C1N, C2P/C2N, C3P/C3N, CYP/CYN, CXP/CXN

Remark:
Capacitor for VCIX2 = 2.2uF
VCI should be separated with VCIP at ITO layout to provide noise free path.
VSS should be separated with VCHS, AVSS and VSSRC at ITO layout to provide noise free path.
All other capacitors 1.0uF ~ 2.2uF (2.2uF is preferred for better display quality and power consumption.)

(Optional capacitors)
VLCD63, capacitors are for stability
Capacitors on CDUM1N/CDUM1P are for power saving.

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Figure 16-3 – Panel Connection Example

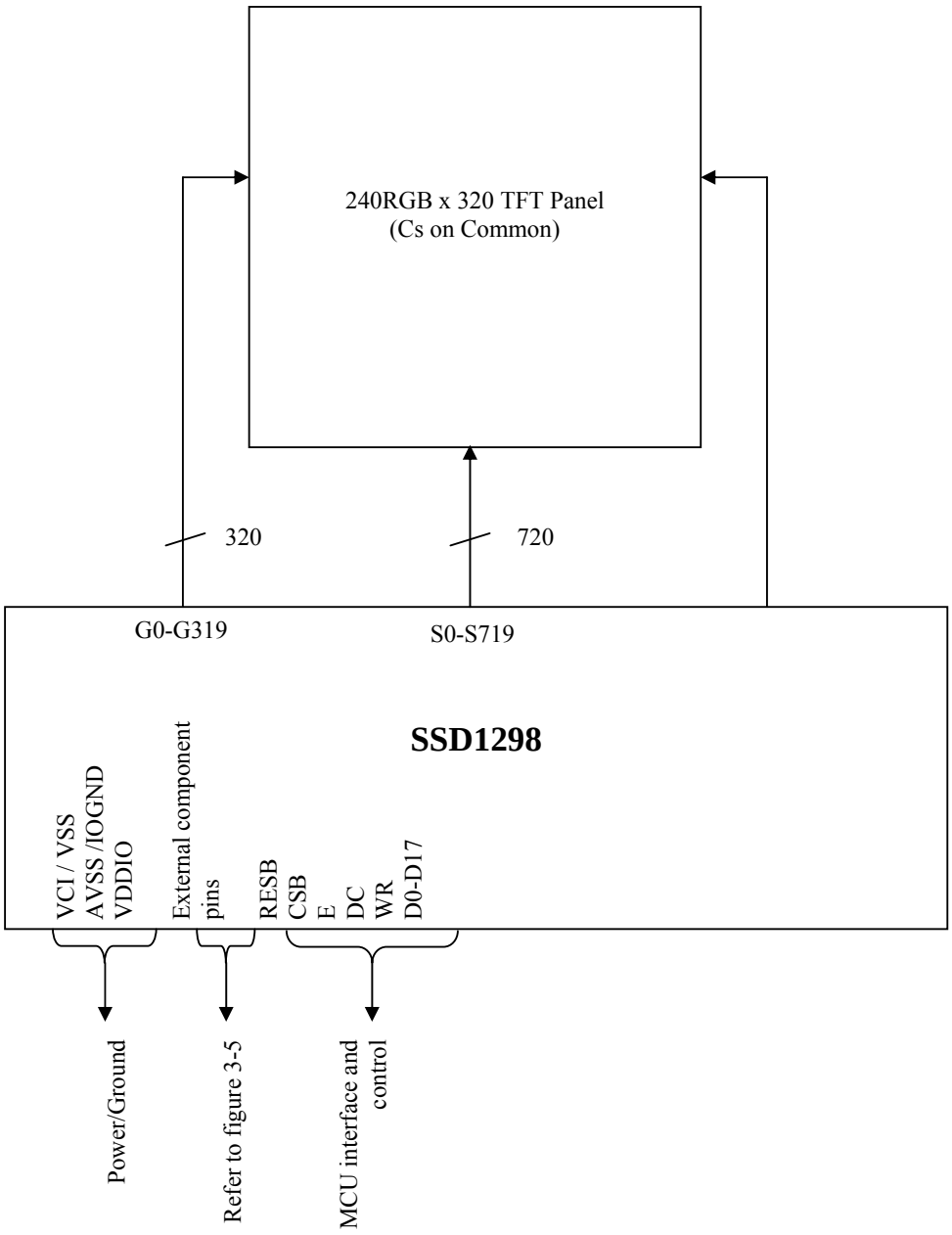

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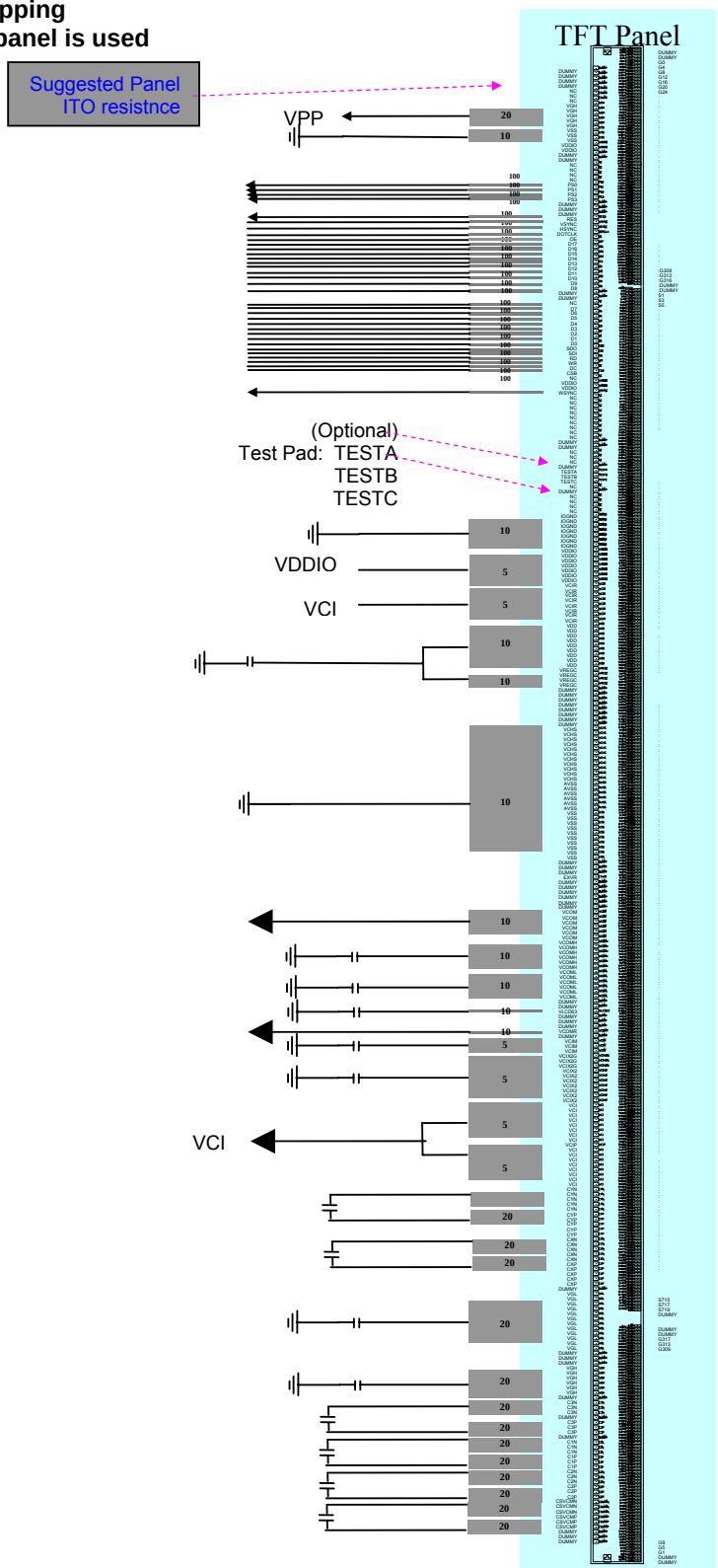
Figure 16-4 - ITO and FPC connection example

Operating conditions:

- **System 3.6V>System VDD>1.95V or1.65V>System VDD>1.4V**
- **Cs on common structure is used**
- **Color filter mapping**
- **Normal white panel is used**



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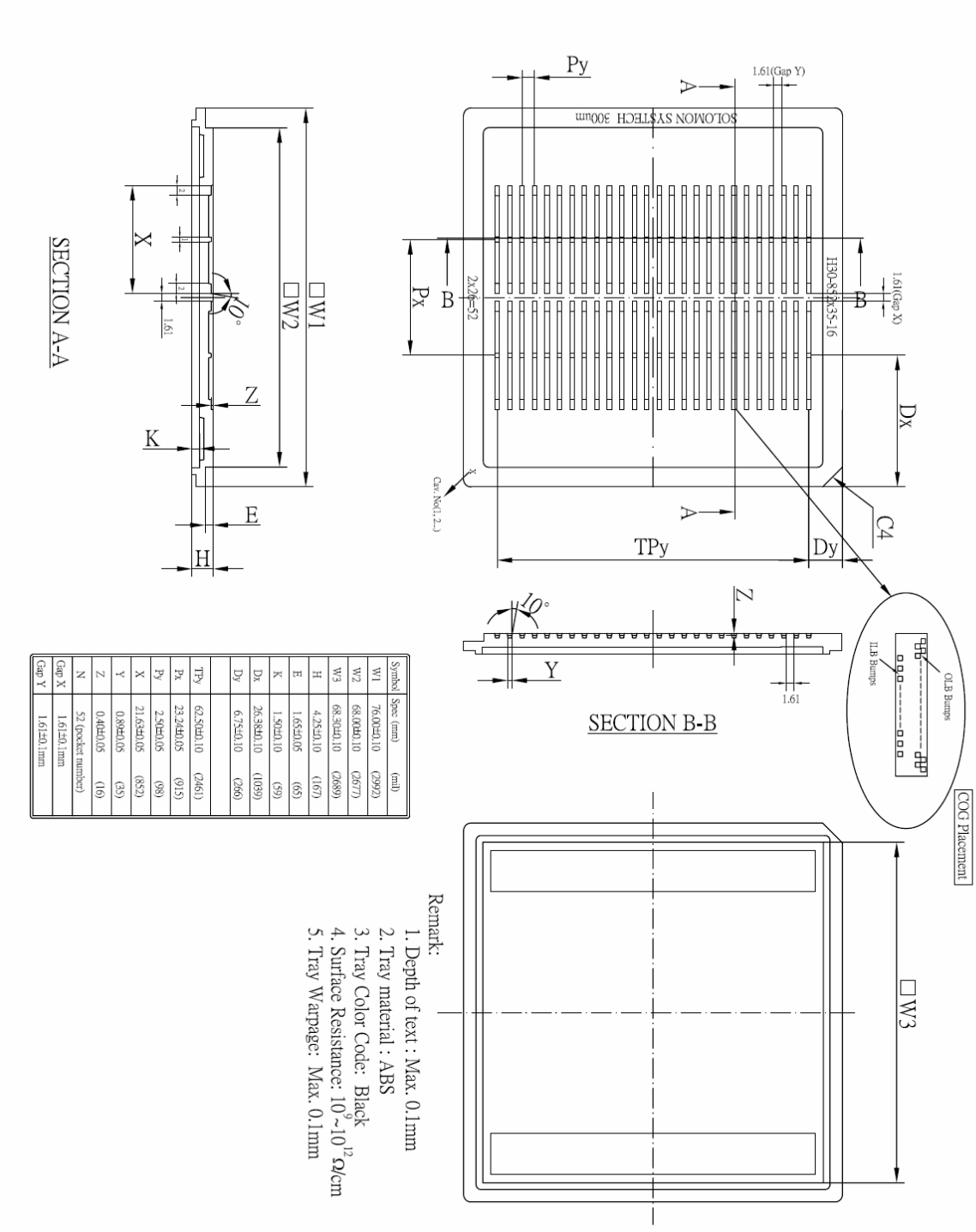
17 PACKAGE INFORMATION

17.1 DIE TRAY DIMENSIONS



Symbol	Spec (mm)	(mil)
W1	76.0±0.10	(2992)
W2	68.0±0.10	(2677)
W3	68.3±0.10	(2689)
H	4.25±0.10	(167)
E	1.65±0.05	(65)
K	1.50±0.10	(59)
Dx	26.38±0.10	(1039)
Dy	6.75±0.10	(266)
TPy	62.50±0.10	(2461)
Px	23.24±0.05	(915)
Py	2.50±0.05	(98)
X	21.63±0.05	(852)
Y	0.89±0.05	(35)
Z	0.40±0.05	(16)
N	52 (pocket number)	
Gap X	1.61±0.1mm	
Gap Y	1.61±0.1mm	

Remark:

1. Depth of text : Max. 0.1mm
2. Tray material : ABS
3. Tray Color Code: Black
4. Surface Resistance: 10^{9}~10^{12} Ω/cm
5. Tray Warpage: Max. 0.1mm

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