Features

- Precision supply-voltage monitor
  - 4.63V (STC706L/705, 813L, 708L/707)
  - 4.38V (STC706M/706, 813M, 708M/708)
  - 3.08V (STC706T, 813T, 708T)
  - 2.93V (STC706S, 813S, 708S)
  - 2.63V (STC706R, 813R/706P, 708R)
  - 2.32V (STC706Z, 813Z, 708Z)
  - 2.20V (STC706Y, 813Y, 708Y)
- 200ms reset pulse width
- Debounced TTL/CMOS-compatible manual-reset input
- Independent watchdog timer 1.6sec time-out (not available for STC707/708/708T/708S/R/Z/Y)
- Reset output signal:
  - Active-low only (STC705/706/706T/S/R/Z/Y)
  - Active-high only (STC813L/M/T/S/R/706P)
  - Active-high and active-low (707/708/708T/S/R)
- Voltage monitor for power-fail or low battery warning
- Guaranteed $\overline{\text{RESET}}$/RESET valid at V_{CC} = 1.2V

Introduction

The STC706X/813X/708X family microprocessor (µP) supervisory circuits are targeted to improve reliability and accuracy of power-supply circuitry in µP systems. These devices reduce the complexity and number of components required to monitor power-supply and battery functions.

The main functions are:

1. Asserting reset output during power-µp, power-down and brownout conditions for µP system;
2. Detecting power failure or low-battery conditions with a 1.25V threshold detector;
3. Watchdog functions (not for STC708x).

Applications

- Power-supply circuitry in µP systems

Contents

Block Diagram

Figure 1. Block Diagram of STC706X/707, STC813X/706P

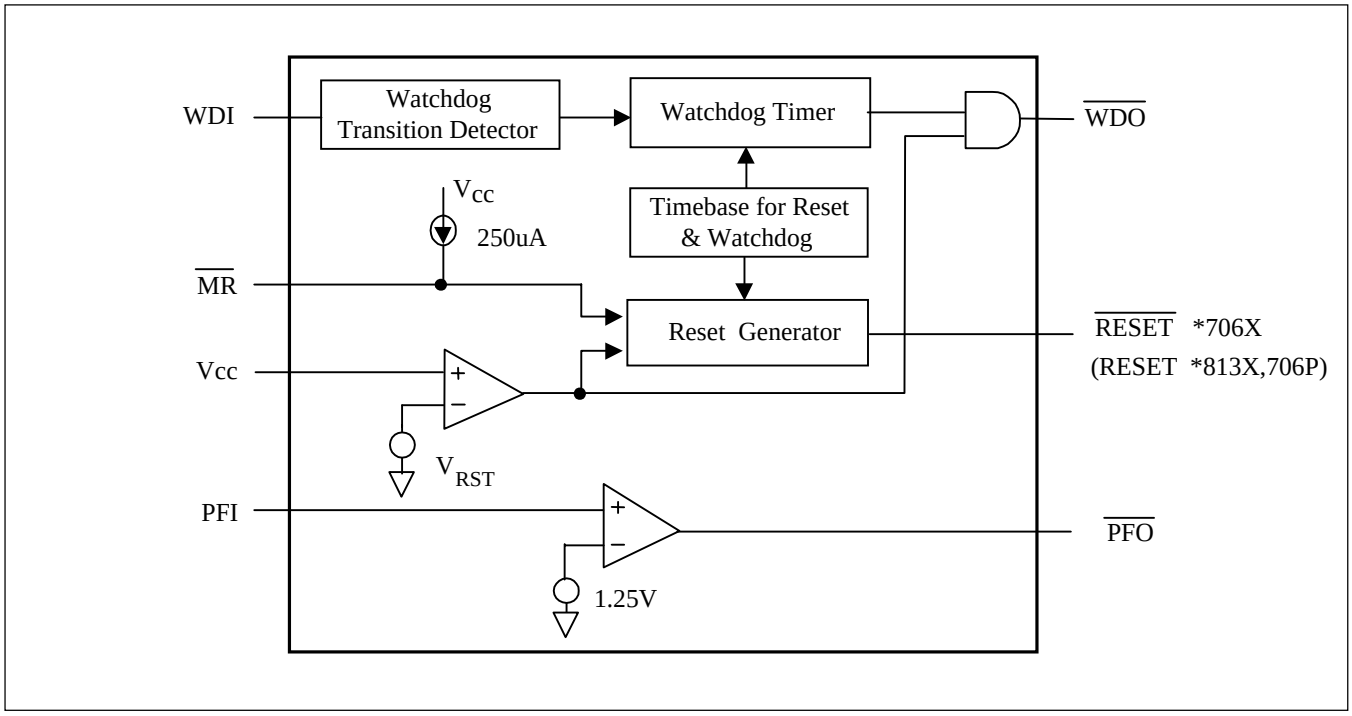
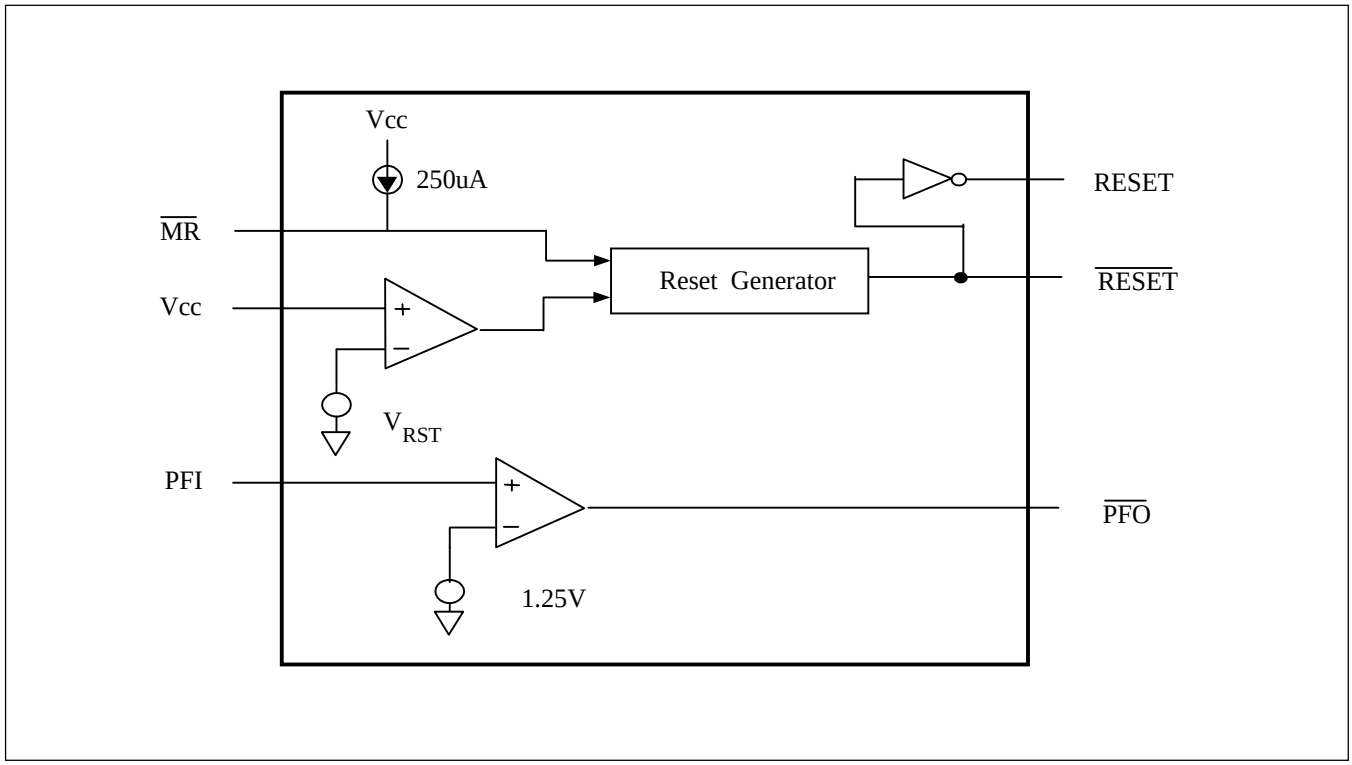


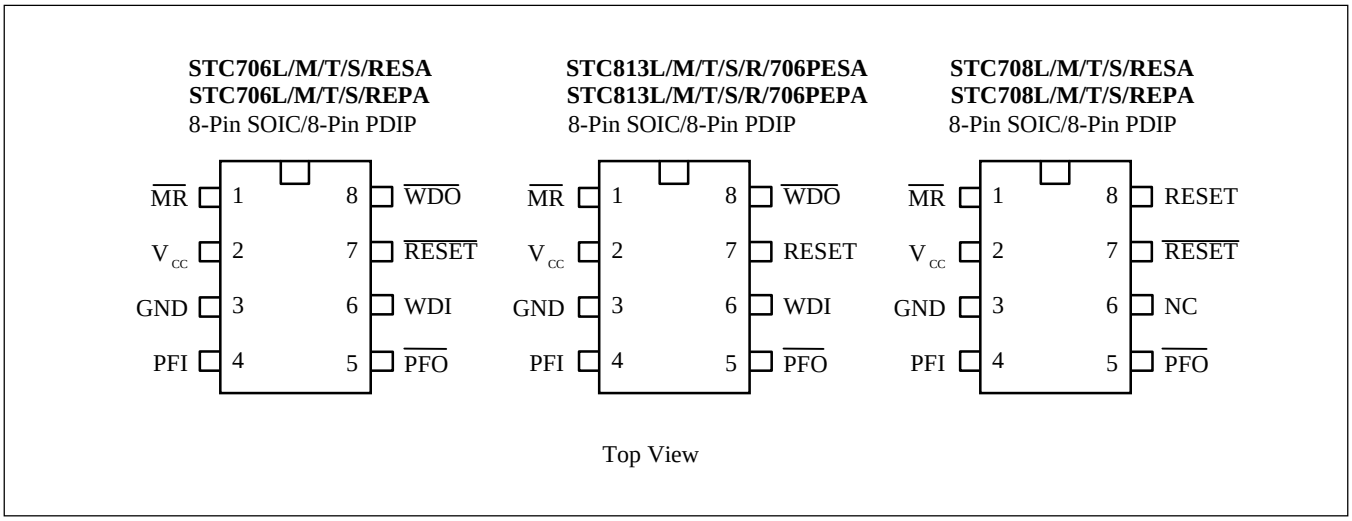
Figure 2. Block Diagram of STC708X / 707



Pin Information

Pin Configuration

Figure 3. Pin Configuration



Pin Description

Table 1. Pin Description

Pin Name	Type	Description
$\overline{MR}$	I	**Manual-Reset:** triggers a reset pulse when pulled below 0.8V, active low. It has an internal 250µA pull-up current and be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
Vcc	Power	**Power Supply**
GND	Ground	**Ground Reference** for all signals
PFI	I	**Power-Fail Voltage Monitor Input**: When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or Vcc when not used.
$\overline{PFO}$	O	**Power-Fail Output:** it gets low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
WDI	I	**Watchdog Input**: If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and $\overline{WDO}$ goes low. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted. WDI is three-stated, or WDI sees a rising or falling edge.
NC		No Connect
$\overline{RESET}$	O	**Reset Output pulses:** low for 200ms when triggered, and stays low whenever Vcc is below the reset threshold. It remains low for 200ms after Vcc rises above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
$\overline{WDO}$	O	**Watchdog Output**: pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions. Whenever Vcc is below the reset threshold, $\overline{WDO}$ stays low; however, unlike $\overline{RESET}$, $\overline{WDO}$ does not have minimum pulse width. As soon as Vcc rises above the reset threshold, $\overline{WDO}$ goes high with no delay.
RESET	O	**The inverse of $\overline{RESET}$**: active high. Whenever $\overline{RESET}$ is high, RESET is low.

Functional Description

The STCxxx family can assert reset output during power-up, power-down and brownout conditions for uP system, detect power failure or low-battery conditions with a 1.25V threshold detector and have watchdog functions. Refer to Table 2 for their individual features. The typical application see Figure 4.

Reset Output

The supervisory circuits can assert reset for a microprocessor during power-up, power-down and brownout to prevent code execution errors.

On power-up, once V_{CC} reaches about 1.2V, $\overline{RESET}$ is a guaranteed logic low of 0.4V or less. As V_{CC} rises, $\overline{RESET}$ stays low. When V_{CC} rises above the reset threshold, an internal timer releases $\overline{RESET}$ after about 200ms. $\overline{RESET}$ pulses low whenever V_{CC} drops below the reset threshold (brownout condition). If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms.

On power-down, once V_{CC} falls below the reset threshold, $\overline{RESET}$ stays low and is guaranteed to be 0.4V or less until Vcc drops below 1V.

The STC813x and STC706P active-high RESET output is simply the complement of the $\overline{RESET}$ output, and is guaranteed to be valid with V_{CC} down to 1.2V. Some µPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Timer

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec and WDI is not in high impedance, $\overline{WDO}$ goes low. As long as $\overline{RESET}$ is asserted or the WDI input is in high impedance, the watchdog timer will stay cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, $\overline{WDO}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{WDO}$ will go low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but $\overline{RESET}$ goes low simultaneously, and thus overrides the NMI interrupt. If WDI is left unconnected, $\overline{WDO}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{WDO}$ goes low only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

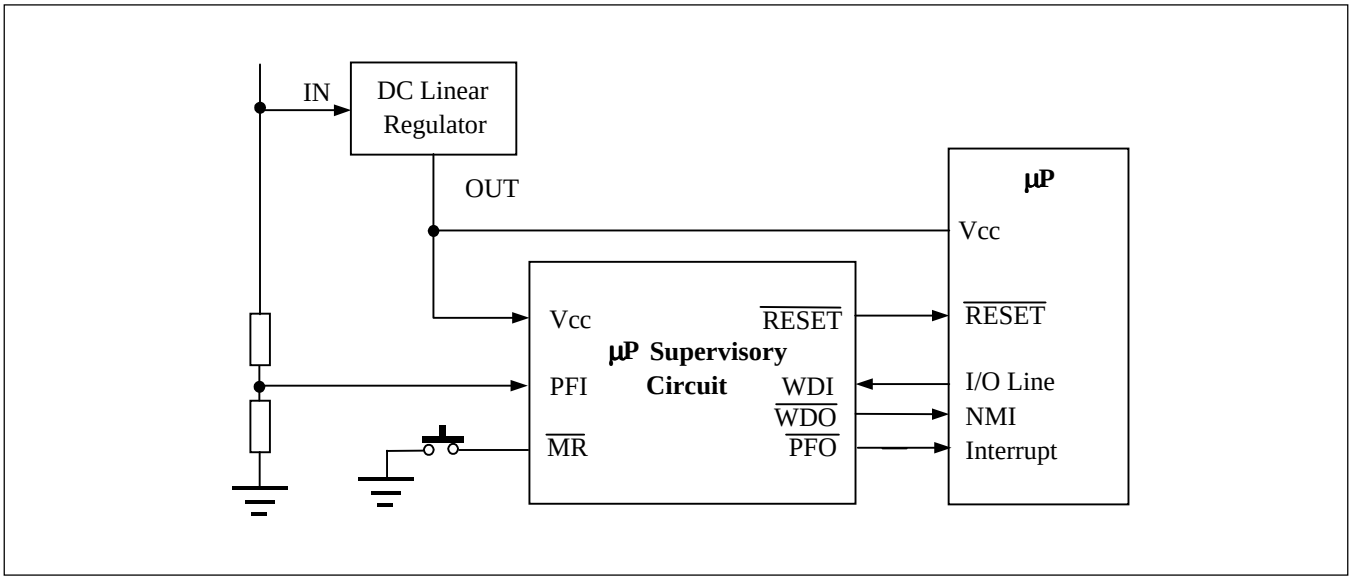
Manual Reset

The manual-reset input ($\overline{MR}$) allows reset to be triggered by a push-button switch. The switch is effectively debounced by the 140ms minimum reset pulse width. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by any logic reset output.

Power-Fail Comparator

The power-fail comparator will send out a Low signal once detects a voltage lowered than 1.25V. It can be used for various purposes because its output and non-inverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

Figure 4. Typical Application Circuit



Function Reference Table

Table 2. Function Table of PT7A75xx Family

Part No.	Reset Threshold	Reset Active Low or High	Nom. Reset Time (ms), t_{RS}	Nom. Watch dog Time (sec), t_{WD}	Power Fail Comp.	Manual Reset Input
STC706L/705	4.63V	LOW	200	1.6	1.25V detector	Yes
STC813L	4.63V	HIGH	200	1.6	1.25V detector	Yes
STC708L/707	4.63V	LOW, HIGH	200	unavailable	1.25V detector	Yes
STC706M/706	4.38V	LOW	200	1.6	1.25V detector	Yes
STC813M	4.38V	HIGH	200	1.6	1.25V detector	Yes
STC708M/708	4.38V	LOW, HIGH	200	unavailable	1.25V detector	Yes
STC706T	3.08V	LOW	200	1.6	1.25V detector	Yes
STC813T	3.08V	HIGH	200	1.6	1.25V detector	Yes
STC708T	3.08V	LOW, HIGH	200	unavailable	1.25V detector	Yes
STC706S	2.93V	LOW	200	1.6	1.25V detector	Yes
STC813S	2.93V	HIGH	200	1.6	1.25V detector	Yes
STC708S	2.93V	LOW, HIGH	200	unavailable	1.25V detector	Yes
STC706R	2.63V	LOW	200	1.6	1.25V detector	Yes
STC813R/706P	2.63V	HIGH	200	1.6	1.25V detector	Yes
STC708R	2.63V	LOW, HIGH	200	unavailable	1.25V detector	Yes
STC706Z	2.32V	LOW	200	1.6	1.25V detector	Yes
STC813Z	2.32V	HIGH	200	1.6	1.25V detector	Yes
STC708Z	2.32V	LOW, HIGH	200	unavailable	1.25V detector	Yes
STC706Y	2.20V	LOW	200	1.6	1.25V detector	Yes
STC813Y	2.20V	HIGH	200	1.6	1.25V detector	Yes
STC708Y	2.20V	LOW, HIGH	200	unavailable	1.25V detector	Yes

Mechanical Information

Figure 7. 8-Pin SOIC